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An Enhanced Algorithm for Wavelength Division Multiplexed Loop Buffer Memory Based Optical Packet Router

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Abstract: *To resolve the conflict during contention, packets are needed to be buffered. Data centers are the core of the networking. The users connect to ToR switches by various network topologies. Topology designs and applications running on data centers decide the traffic characteristics. Due to cloud computing environment in many data center switches distinctive varieties of applications runs. Thus, traffic characteristics vary on various data center switches. This paper discusses the random traffic model for data arrival on Top of Rack (ToR) switches and details of traffic shaping techniques are discussed. Finally the blocking performance of the ToR switches is measured to characterize the traffic shaping techniques.*

The loop buffer module used in this switch architecture is a new approach towards WDM buffering of packets. The mathematical modeling is done to validate the results obtained from simulation.

Keywords: AWG, BER, Cost Analysis, SOA, OPS; TWA.

Introduction

In optical transport networks, the current approach is to use optical switches to set up light paths. These all-optical switches are circuit switches and transparent to information carried over light path. Another alternative strategy could be to deploy all-optical packet switches and use packet switching in optical layer for data trans- port. Since the data is generated by electronic sources, only motivation to build the all-optical packet switch is when ingress routers aggregate the large number of pack- ets optically for very high bit rate payload.

This aggregated payload can be attached with low bit rate header and pushed into core optical network. The all-optical packet switches will convert the header of the packet to electrical form and keep the payload in optical form. The rise of cloud computing and other emerging web applications has created the need for more powerful warehouse-scale data centers. These data centers comprise hundreds of thousands of servers that need to communicate with each other via high performance and low latency interconnection networks.

With the rapid growth in Internet applications, data centers have witnessed demands for more and more storage, computation power, and communication bandwidth. In the present day's telecommunication environment, hundreds of thousands of servers are very common in heavy data center systems. In the recent survey report given by Cisco (Cisco Global Cloud, 2011), the yearly worldwide data center traffic is expected to reach several zetta bytes by the end of 2017. The data traffic, which is generated between the data centers and within the data center, is expected to grow extensively.

These features, discussed above, make optical networks the best available solution for the challenges faced by data center networks The header information can be used to route the packet. Once the packet reaches egress node, the aggregated packets can be separated using

optical demultiplexing techniques and passed onto the client network. Many optical packet switching (OPS) architectures have already been proposed in literature (Tucker and Zhong 1999; Dittmanm et al. 2003).

WDM technology had been incorporated (Dan- ielsen et al. 1997) to improve their performance. The limitations of the electronic switches results in the need of optical cloud networks. The real issue engaged with the optical cloud system is the switch/router structure which can perform exchanging operations efficiently at the high information rates. These can be named 'all'- optical cloud or photonic switches. On the whole optical cloud mode, the propagation and the handling of information is thought to be in optical cloud domain. As of now, optical cloud computing switch is not innovatively practical because of the absence of optical cloud RAMs

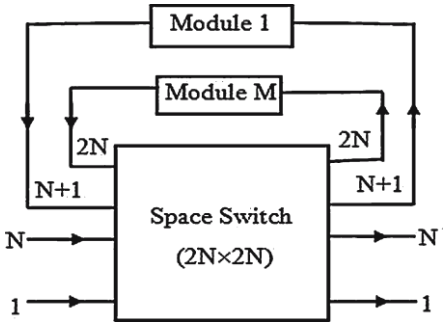

Figure 1 Optical packets switch architecture: modules (1 to M) represent optical loop buffer memories

loss probability and delay are presented in Sect. 5. Mathematical analysis is done in Sect. 6 and its results are compared with simulation results in Sect. 7 to validate the simulation analysis. Finally, Sect. 8 concludes the work.

Description of Router Architecture

The proposed architecture of optical packet switch is shown in Fig. 1. The core of this architecture is a nonblocking space switch of dimension $2N \times 2N$. The lower N ports (indexed 1 to N) of the core switch are used as switch inputs/outputs and the upper N ports (indexed $N+1$ to $2N$) are used for buffering the packets in the optical loop buffer modules (Fig. 2). Under this condition, the maximum numbers of allowed buffer modules are $m = N/D$, where D is the number of input/output at each loop buffer module. This D and hence m depend upon desired packet loss probability. If the switch is designed for M modules ($M \geq m$), then rest of the upper half ports (i.e., $N - MD$) will be left free and the switch fabric of size $(N + MD) \times (N + MD)$ is used. Hence, the effective size of core switch is $(N + MD) \times (N + MD)$ where N is the actual number of inputs. The length of delay line as well as the slot duration has been assumed of one packet length. Newly arriving packets and already stored packets may also contend for the same output. In such case, one of the contending packets is directed to the output port and remaining packets are kept in buffer according to the scheduling algorithm given in Sect. 4. When contending packets can neither be directed to assigned output port nor stored in buffer, it is dropped and assumed to be lost.

Each buffer module (Fig. 2) consists of D tunable wavelength converters (TWC) at its input, a recirculating loop buffer, and D fixed filters (FF) at its output (Verma et al. 2002; Shukla et al. 2004). The path followed by a packet while circulating inside the loop, consists of 3 dB coupler, DEMUX, TWC, combiner, erbium-doped fiber ampli- fier (EDFA), isolator and again the same 3 dB coupler. The number of TWC and the size of DEMUX and combiner inside the loop depend upon the required buffer capacity (B) and hence, these are considered equal to B. Thus, the total number of TWCs and FF used in the buffer module will be ($B + D$) and D

respectively. EDFA is placed inside the loop to compensate the power loss through the loop buffer during circulations.

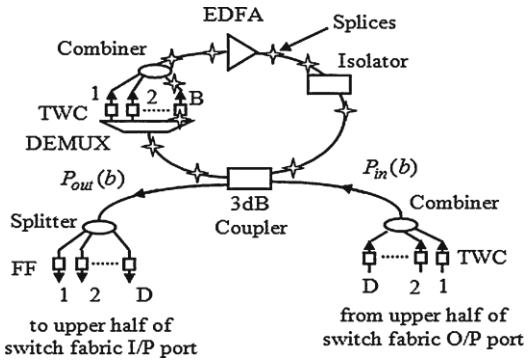

Figure 2 Optical loop buffer memory module

Each buffer module uses (B D) wavelengths where B is the number of buffer wavelengths used to store the packets in buffer modules, and D is the number of wavelengths used for reading out the packets from the buffer modules. Packets from all the D inputs use WDM technology to share the recirculating loop buffer. The number of buffer wavelengths (B) inside the memory module depends on the switch design, desired traffic throughput, packet loss probability and size of the switch (Shun et al. 2003). The allocation of the packets to the loop buffer depends on the routing and priority algorithm for the switch. The packets to be buffered are converted to the wavelengths available in the buffer; if buffer is full then packets are dropped. When a packet is forwarded for buffering, the respective TWC at the input of the available buffer module is tuned to any one of the B loop buffer wavelengths, which is free to accept the packet. As long as a packet remains in the buffer, the TWC inside that mod- ule, corresponding to the wavelength assigned to this packet, will remain transparent till it is desired to read out the packet or to have dynamic wavelength re-allocation. For reading out a packet when output contention is resolved, the corresponding TWC is tuned to the wavelength of appropriate output port fixed filters (FF). The packet is then broadcasted towards FFs and received by the intended one. Then, these pack- ets can be directed to the destined output port through the space switch fabric. We have assumed an electronic control unit (not shown in the figures) which tunes var- ious components of the loop buffer as well as controls the whole switch. The similar type of electronic controlling technique is already described in Fow-Sen Choa et al. (2005). The control of packet buffering is also done by this controller according to the scheduling algorithm proposed in Sect. 4. We have used the SOA based TWC which is proposed and fabricated in Fow-Sen Choa et al. (2005) and it is operated on the *nano-second* scale. The space switches are considered as SOA based electro-optical switch. The switching speed of this device is also of the order of *nano-second* while the insertion loss will be 0.5 dB per stage. The crosstalk is low (30 dB) and is negleeted in the calculation (Mynbaev and Scheiner 2001). Thus, the tuning speed of TWCs and the switching speed of space switch, do not put any constraint on the switching operation.

Half of the power is passed directly to the FFs. But, these FFs are chosen to receive the wavelength of range D only, so it will discard the wavelength coming directly (not from the loop) because the range of those wavelengths correspond to B. While reading-out a packet from the loop, the corresponding TWCs inside the loop tune that packet to any of the D wavelength and then the packet passes through 3 dB coupler. Again, half of the power of this packet will be passed towards the FFs and another half power will enter to the loop. But this time, the half power entering to the loop, is discarded by the DEMUX because the passing wavelength range of DEM- UX is chosen equal to B. This will remove the assignment of the buffer wavelength. Henceforth, the wavelength will become free and can be assigned to another packet.

We have analyzed the switch for limitation on buffering due to degradation as a result of accumulated noise. Further study of packet loss probability and average delay, for a given scheduling policy and switching parameters, has also been done.

Literature Survey

In Optical Cloud Packet Switching (OPS) various work is proposed in past, a brief review of the work detailed in this section.

Barry and Pierre (1995) developed a traffic model for circuit-switched all-optical cloud networks to evaluate the blocking probability with and without wavelength conversion this paper develops an idea to evaluate the packet loss rate in optical cloud networks. Singh *et al.* (2007) examined the routing wavelength assignment problem in optical cloud network without wavelength conversion as due to wavelength continuity problems.

Maite *et al.* (2009) presented a new heuristic offline wavelength assignment mechanism. In this work, QOS is also discussed by considering both BER and latency. This paper discusses two algorithms for the wavelength assignments such that QOS can be maintained.

He *et al.* (2011) proposed that the quality of an optical cloud signal degrades due to physical layer impairments as it propagates down the length. As a result, the signal quality at the receiver of a light path may not be sufficiently high, leading to increased call blocking. Suggested a model for WDM optical cloud networks and also proposed an algorithm based on most used wavelength assignment for minimizing the blocking probability. These results are then compared with the conventional wavelength assignment algorithms such as first fit, random fit and most used wavelength assignment algorithms given a mathematical model for reducing the blocking probability of the WDM optical cloud network. Their proposed model has low implementation complexity and its computation is quite efficient. This model is also used to evaluate the blocking performance of NSFNet topology and used to improve its performance.

Wang and Wen (2012) have proposed two light path-level active rerouting algorithms, which are the least resources rerouting algorithms and the load balanced rerouting algorithms. Simulation results show that the proposed load-balanced active rerouting algorithm yields much lower connection blocking probability than the least resources rerouting algorithms. This result shows that the performance of the networks can be significantly improved. In the above mentioned papers, the researcher looked into the routing algorithms, and minimizing the blocking probability with and without wavelength conversion.

Josep *et al.* (2012) in this work, accumulation of physical layer impairments on the signal along optical cloud transparent paths is discussed, therefore limiting the system reach and the overall network performance. Such challenges require the use of cross-layer approaches, which involve dynamic interactions between the physical layer and the network layer to enable the compensation for mismatching of requirements and resources. He provides an overview of such challenges, reporting comparative analysis with a selection of existing solutions and to cast a glance at the open issues for future research.

Marino *et al.* (2013) transparent optical cloud networks are the enabling infrastructure for converged multi-granular networks in the Future Internet. The cross-layer planning of these networks considers physical impairments in the network layer design. This is complicated by the diversity of modulation formats, transmission rates, amplification and compensation equipment, or deployed fibre links. Thereby, the concept of Quality of Transmission (QOT) attempts to embrace the effects of the physical layer impairments, to introduce them in a multicriterium optimization and planning process. This paper contributes in this field by the proposal and comparative evaluation of two novel offline impairment aware planning algorithms for transparent optical cloud networks, which share a common QoT evaluation function.

Research Gap and Research Problem

A design for optical cloud node will be presented. The physical layer impairments will be discussed and a mathematical framework be presented to estimate the BER performance of the optical cloud node. The physical layer analysis would concentrate on how packet size and bit rate affect the performance of the switch. The power dissipation analysis will also be performed to visualize the power requirement in as a switch. At the network layer packet loss performance would be evaluated.

The proposed switch is analyzed in terms of loss, power and noise by using the model shown in Fig. 2. The values of various parameters used in the following analysis, are reported in Table **Loss analysis**

For the convenience of calculation, the loss in this architecture has been divided into three parts.

1. The input section of the buffer module consists of TWC and combiner. Hence, loss from switch input up to the loop buffer input, termed as *Insertion loss* (A_{ins}), is given as

$$A_{ins} = L_{SF} L_{TWC} L_{Com} \quad (1)$$

2. Loss through the loop buffer is termed as *Recirculation loss* (A_{Re}). This has been obtained by breaking the loop in two parts for the ease of calculation. These are defined as below,

$$A_1 = L_{3dB} L_{DEMUX} L_{TWC} L_{Com} 6 L_S L_{F1} \quad (2)$$

$$A_2 = L_{ISO} 4 L_S L_{F2} \quad (3)$$

where, A_1 is loss of the buffer from entry port of loop buffer up to input of EDFA, and A_2 is loss after EDFA up to 3 dB coupler. Other variables are defined with relevant vaues in Table 1. Total loss of the loop buffer after one circulation, can be given as

$$A_{L_K} = (A_1 A_2).$$

Hence, after K circulations the recirculation loss will be

$$A_{Re} = (A_L).$$

All the losses in this model are fractional losses of power i.e., output/input (Watts/Watts).

3. The output section of the buffer module consists of splitter and FF. Hence, loss from the loop buffer output up to the switch output, termed as *Extraction loss* (A_{ext}), is given as,

$$A_{ext} = L_{SP} L_{FF} L_{SF} \quad (4)$$

Thus, total loss through the switch architecture is

$$A = A_{ins} A_{Re} L_{3dB} A_{ext} \quad (5)$$

Power Analysis

The TWC is a noisy device i.e., it adds noise to the incoming signal whenever it per- forms tuning for wavelength conversion while it will not introduce any noise when it is transparent (no tuning). But, sometimes it is considered as noiseless device for the performance observation because the introduction of noise may be compensated by the regeneration of the

signal in the TWC (Mamyshev 2004). So, we have done the analysis in two ways considering: (i) TWC as the noiseless device and (ii) TWC as the noisy device.

TWC as the noiseless device,

If we follow the above model (Fig. 2) then the power of bit '1' and bit '0' [$P_{in}(1)$ and $P_{in}(0)$] entering through the input of loop buffer, are

$$P_{in}(1) = P_{av}A_{ins}^{-\frac{2\varepsilon}{\Sigma}} \text{ and } P_{in}(0) = P_{av}A_{ins}^{-\frac{2}{\Sigma}} \quad (6)$$

P_{av} is average signal power at the switch input and 'ε' is the extinction ratio, defined as ε $P(1)/P(0)$. Thus the signal power, just before the 3 dB coupler after one circulation, is given by

$$A_L P_{in}(b)G + (G-1)n_{sp}h\upsilon B_o A_2 \quad (7)$$

where, $b = 1$ for bit '1' and $b = 0$ for bit '0'. In the Eq. (7), first term represents the sig- nal power and second term represents amplified spontaneous emission (ASE) noise power (Olsson 1989). A_L is loss of the loop in one circulation, G is the gain of Erbium Doped Fiber Amplifier (EDFA) and B_o is the optical bandwidth.

Thus, the power for the bit 'b' after K circulations, just before the 3 dB coupler, is

$$P_K(b) = (A_L)^K P_{in}(b)G^K + (G-1)n_{sp}h\upsilon B_o A_2 F \quad (8)$$

In Buffer,

$$P_{out}(b) = P_K(b)L_{3dB}1) \quad (9)$$

Here $I(1) = RP(1)$ and $I(0) = RP(0)$ are photocurrent, sampled by receiver during bit '1' and bit '0' respectively, and R is responsively of the photo detector.

Data Analysis

For the calculation of gain of the EDFA, we used the model given in Giles and Desurvire (1991). The number of channels passing through EDFA will vary during different time slot. This will change the gain of EDFA. Hence, we have assumed automatic gain control scheme (AGC), where gain of the EDFA will remain constant irrespective of the number of channels passing through it (Naik and Singh 2002; Richards et al. 1997). Since, we are using loop buffer module of capacity B with its various combination (i.e., $B = 4$, 8 and 16), hence the size as well as gain of the EDFA will also be changed in order to maintain the condition of $A_L G = 1$ inside the loop. The gain of EDFA for different buffer space has been computed by considering the loss through each component of loop while the corresponding doped fiber length has been taken from Giles and Desurvire (1991) and is shown in Table 2.

The length of the loop is equal to the packet duration and is given by Lcb/nR_b, where c is the speed of light, b is number of bits, n is the refractive index of fiber and R_b is the bit rate. We have assumed equal length packets of 53 bytes alongwith 1 byte period of guard time on each side and $n = 1.55$. The length is plotted against bit rate in Fig. 3. Here, the minimum loop length should be equal to the length of EDFA, required to provide the sufficient gain. We can observe in Table 2 that the minimum length of fiber is 10m which is needed to maintain the gain of 16.85 dB at $B = 4$.

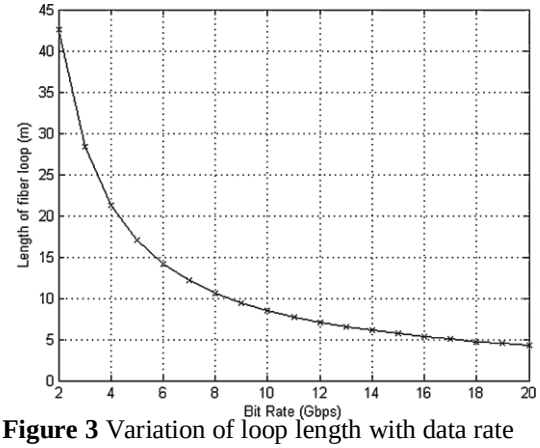

Figure 3 Variation of loop length with data rate

Obvious from Fig. 3 that the maximum bit rate which can be used, is 8 Gbps for 10 m length of fiber. Similarly for $G = 26.65$ dB at $B = 16$, the required minimum fiber length is 14 m and thus, the corresponding maximum bit rate will be 6 Gbps. If we consider a bit rate of 5 Gbps, the required loop length will be 17.04 m. Thus for $B = 4$, since the EDFA length should be 10 m, the required fiber length will be 7.04 m to form the complete loop of 17.04 m.

The wavelength selection have been done by following the ITU grid and the cho- sen range of wavelength is from 1550.12 to 1552.52 nm with a spacing of 0.8 nm ($Of = 100$ GHz). For the minimization of crosstalk, channel spacing should be greater than 6 times of the bit rate (Shun et al. 2003); Kartalopoulos 2000) (i.e., $Of \geq 6R_b$). Since, in this paper, the channel spacing (Of) is considered equal to 100 GHz and $R_b = 5$ Gbps. Hence, we can ignore the effect of crosstalk because it satisfies the above mentioned condition i.e., $6R_b = 30$ Gbps and $Of > 6R_b$.

We have obtained (Table 3) the number of maximum allowed circulations (C) at different power levels (in mW) with various combinations of switch size (N) and number of buffer wavelength (B) considering TWC as the noiseless device. The number of circulations C, is the largest value of K (circulations count) for which, BER 10^{-9}. It was found in the computed results (Table 4) that if we increase B beyond D, then the number of maximum allowed circulations decreases which in turn, may degrades the performance of large switch drastically. Hence, the maximum number of possible wavelength in any of the buffer module is considered as 4 because, for larger value of B (i.e., 8 and 16), the number of allowed circulations is zero at lower power and not much accountable at larger power. We have also calculated the number of maximum allowed circulations considering the TWC as the noisy device and the data is given in Table 5. If we compare these data with that one given in Table 3, then we can observe that there is not much effect of TWC noise on the number of maximum allowed circulation. So, the results for loss probability will be nearly same for both the cases.

Scheduling algorithm

The buffering in the modules is done using the following scheduling algorithm:-

1. The TWCs placed at the inputs of the loop buffer (Fig. 2), can be tuned to any of the B wavelengths and the TWCs inside the loop can be tuned.

Table 1 Maximum number of allowed Circulation (C) for various size (2N) of core switch and buffer

$2N$	B	C at P =1	C at P =2	C at P =5	C at P = 10
32	4	2	4	12	25
64	4	1	3	10	20
128	4	1	2	7	16
256	4	0	2	6	12
512	4	0	1	4	10
1024	4	0	1	3	7

Table 2 Maximum number of allowed Circulation (C) for switch of size N = 16 and for different values of D & B at different power levels (P, mW)

$2N$	B	C at P =1	C at P =2	C at P =5	C at P = 10
32	4	2	5	13	26
64	4	2	4	10	20
128	4	1	3	8	16
256	4	1	2	6	13
512	4	1	2	5	10
1024	4	0	1	4	8
32	8	0	1	3	7

($B \neq D$) wavelengths. Further it is assumed that TWC's can be tuned almost instant- tenuously.

2. If there are total i packets buffered in all the modules for the output j, then one of them will be send to the output via switch fabric. If in that slot, there are one or more packets also present at the inputs of switch destined for the output j, then these packets will be stored in the loop buffer to the extent allowed by the rules 4 to 5.

3. Considering the case when there is no packet in the buffer for the output j, but n of N input lines have packets for that output. Then, one of these n packets is directly sent to output j by configuring the switch fabric. The remaining $(n-1)$ packets will be stored in the buffer module to the extent allowed by the rules 4 to 5.

4. Number of packets x_j for the output j, stored in all the buffer modules, should never be greater than $\min(MB, C)$ i.e., $x_j \leq \min(MB, C)$, $1 \leq j \leq N$

5. Total amount of buffered packets for all the outputs, cannot be larger than the maximum buffering capacity MB i.e., $\sum x_j \leq MB$, $1 \leq j \leq N$

6. The buffers in the loop are such that simultaneous read and write is allowed in the same slot for the same wavelength.

7. The contending packets will try to occupy the lowest numbered (1 to M) available module (Fig. 1).

8. During any time slot, priority will be given to the packets stored in the loop buffer modules than the packets at the switch input. Essentially for switch output, FIFO discipline will be maintained.

9. If there are total q packets in all modules for any output r, then oldest of q con- tending packets will leave first for the switch output.

10. Packet for different output will leave the switch at the same time, from their modules.

11. If any of the incoming packets will not be able to pass through the switch due to the maximum buffer capacity limitation, then it will be dropped.

12. Packet will be stored in each module following the constraints specified in 4 to 5. There can be many strategies for storing the packets. Simplest is to find the lowest number memory module, which is empty, and store the packet in it subjected to the constraints specified in 4 to 5. We are considering this algorithm in this paper. Another alternative approach could be to find out the module with minimum number of packets and store the packet on a wavelength such that wavelength spacing for stored packet in the loop buffer is maximized. This will reduce impact of crosstalk due to imperfect filtering characteristics of various devices.

Simulation Analysis and Results

Using the above algorithm, the simulated results for '*packet loss probability*' and '*average packet delay*' are obtained under various loading conditions. The optimiza- tion of switch performance is done considering different number of buffer modules (*M*), and the number of maximum allowed circulations (*C*) at different power levels. Figures 4–6 show results for the switch of size $2N = 32$ with $B \ D \ 4$ and $M \ N/D$. As defined earlier, 16 of 32 are the actual inputs and other 16 are used to connect different number of buffer module. It has been observed that as the number of buffer module (*M*) increase, packet loss probability decreases. We can observe in Fig. 4 that, as the signal power increases, the probability of packet loss decreases due to the increment in *C* with power. But, this increment in power level beyond a value does not give any further advantage as packet loss probability is same for $P = 5$ and 10 mW. This happens because at higher power, packet can be buffered for more time (Table 3) but due to the limitation on maximum buffer space, higher values of *C* will have same effect as with lower one.

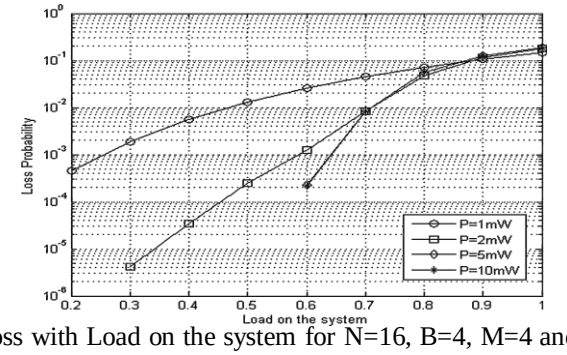

Figure 4 Probability of packet loss with Load on the system for N=16, B=4, M=4 and different values of signal power (P)

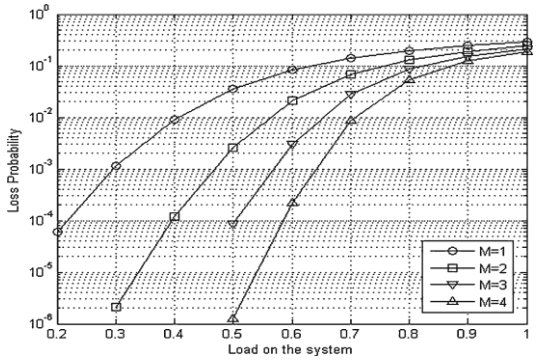

Figure 5 Probability of packet loss with Load on the system for N =16, B=4, P= 5 mW and different values of number of buffer modules (M)

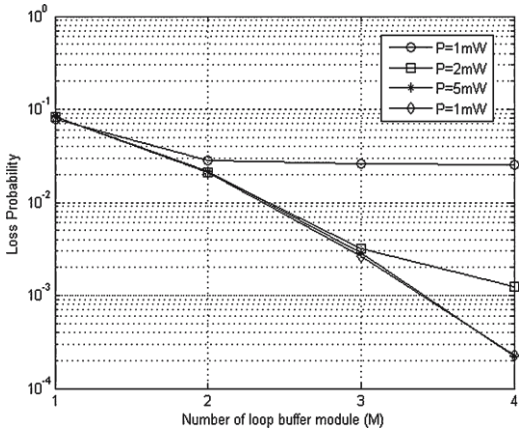

Figure 6 Probability of packet loss with number of buffer module (M) for N=16, B =4, Load = 0.6 and different values of signal power (P)

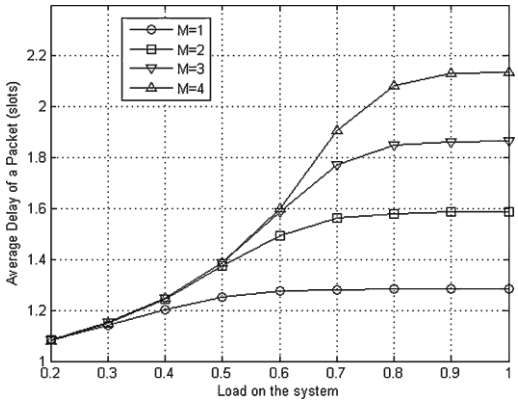

Figure 7 Average Delay with Load on the system for N=16, B=4, M=4 and different values of signal power (P).

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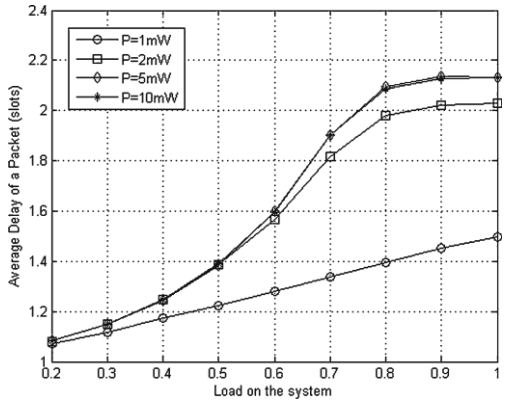

Figure 8 Average Delay with Load on the system for N=16, B=4, P=5 mW and different numbers of module (M)

The delay performance for this switch ($2N = 32$) is shown in Figs.3, 4. The aver- age delay increases with the number of modules. But, it remains same for $P = 5$ and 10 mW because for $N = 16$, we are using maximum number of modules (i.e., $M = 4$) which provide 16 buffer

spaces for any particular output. This indicate that in case of P = 10 mW, although the packet can be stored for 26 slots (Table 3), but due to limited maximum buffer space of 16, the packet cannot be circulated more than 16 slots. Hence the results for case of P = 10 mW will be nearly same as P =5 mW, since C = 13 for P = 5 mW. Hence, the optimized result for $2N$ = 32, are achieved at D B 4, P = 5 mW and M = 4. We have obtained similar trend in results for this architecture with larger size i.e., N = 32, 64 etc.

The results shown till now, is based on the assumption that the TWC is a noise- less device. We have also done the performance analysis of this switch architecture considering the TWC noise. We have found C = 2, 5, 13 & 26 at P = 1, 2, 5 & 10 mW and N = 16 for the noiseless case of TWC (Table 3) while C = 2, 4, 12 & 25 for the noisy TWC (Table 5). There is not much difference among the number of maximum allowed circulations at various power levels. The comparative results for packet loss probability and average delay for N = 16 at different power levels, are shown in Figs. 10 and 11, respectively. We observed that the results at all power levels are overlapping except the case of P = 2 mW where, the loss probability is better and the average delay is more for the case of noiseless TWC. This will happen because, the case of C =4 for noisy TWC may rejects some more packets when the total capacity is 16 (=M B) as compared to the case of C = 5 for noiseless TWC.

Mathematical Analysis

The packets are assumed to be randomly arriving with uniform rate between all source destination pairs. Depending upon the number of packets arriving and busy output port, various buffer states are attained. The state of the buffer is described by a vector 'b' of positive integers and of length N i.e., b $(b_1, b_2, \ldots, b_N)$ where 'b_i' (1 i N) represents the buffer state element for the ith output. Each such element can store packets ranging from 0 to min(MB,C). The sum of packets in any of the buffer state b, will be less than or equal to MB i.e., Σb_i MB. As defined earlier, M is the number of module used in the architecture, B represents the total buffering capacity of each module, and C is the circulation limit allowed for any packet. Thus, min(MB,C) will be used as the maximum buffering capacity for individual output.

Comparison of Mathematical and Simulation Analysis

We have verified our simulation results with the computational one given in Singh et al. (2003) where results are shown for large range of individual as well as total buffer length. To verify this, we have considered N= 4, M= 1, B = 4, in the switch archi- tecture presented here. For this configuration, the architectural logic will be nearly similar to the one given in Singh et al. (2003). In the proposed architecture, we have considered the circulation limit (C) for packets stored in the buffer which will in turn, limit the individual buffer capacity. We have shown the value of C for large switch shown in Fig.2 Comparative results for simulation with mathematical analysis ($N \geq 16$) in Table 3, and it indicate that the C will be larger than MB for N = 4, M =1, B= 4. Thus, there will not be any limit on the number of maximum allowed circulations because the net individual buffer capacity will be min(MB,C). Hence, for verification of the simulation results in the presence of circulation limit, we have considered a hypothetical value of C 2 for N 4 and compared the obtained result with the one given in Singh et al. (2003). The comparative results are shown in Fig. 12 and it is found that the variation of packet loss probability obtained from simulation method, strictly follows the mathematical analysis.

Conclusion

We have presented the architecture of an optical packet switch with feedback shared buffering using WDM loop buffer modules. The application of modular structure reduces the need for large range of wavelengths because the same set of wavelength is used in all the

buffer modules. One of the major advantages is that multiple loop buffer modules act together as one single fully shared buffer. Due to reuse of wave- length range, the bandwidth of certain component e.g., EDFA and TWC, does not restrain the total size of the buffers.

The power required for the correct operation of switch A1 is 300 nW, while in switch A2, the power requirement is 9µW, so the performance of switch A1 is much better in terms of power requirement:-

1. Each of the switches presented in the paper uses nearly the same type of components. The requirements of optical components are high in switch A2 as compared to switch A1.

2. As the cost of the optical components is too high, a detailed cost analysis of each switch is presented in the paper and the obtained results show that at "*a=1*" and "*b=1*," the cost of switch A1 is 2,632 units, while the cost of switch A2 is 3,280 units, so the design of switch A1 is more cost effective.

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