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A

A

# VTSG-104 Schematic

## VTSG-104

B

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C

Telecommunication Industry Development Park  
2019.06

D

D

Project Name : VTSG-104.PrjPcb			
Title : Cover Page			
Size : A4	Drawer : Kim Ung		
Revision : 001	Checker : *		
File Name : 001_CoverPage.SchDoc			1 / 20
		2020.04.20	

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## Revision Table

A

No

## History

Human

Page

Date

1

Alpha Version

Kim Ung



2019.06.05

No

## History

Human

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Date \_\_\_\_\_

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Project Name : VTSG-104.PrjPcb		
Title : Revision		
Size : A4	Drawer : Kim Ung	
Revision : 001	Checker : *	
File Name : 002_RevisionTable.SchDoc		2 / 20 2020.04.20

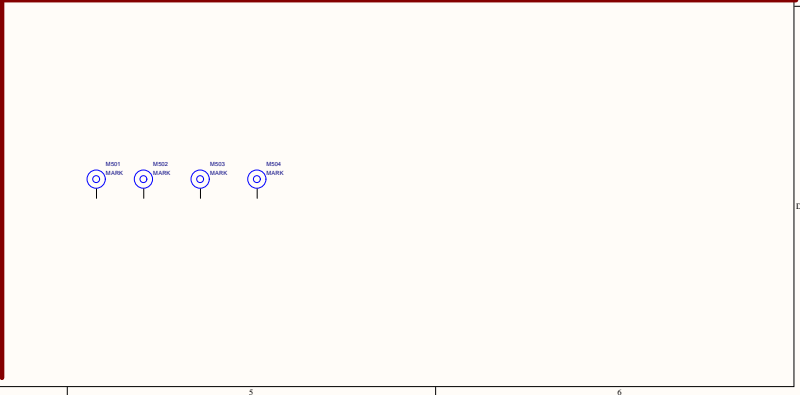
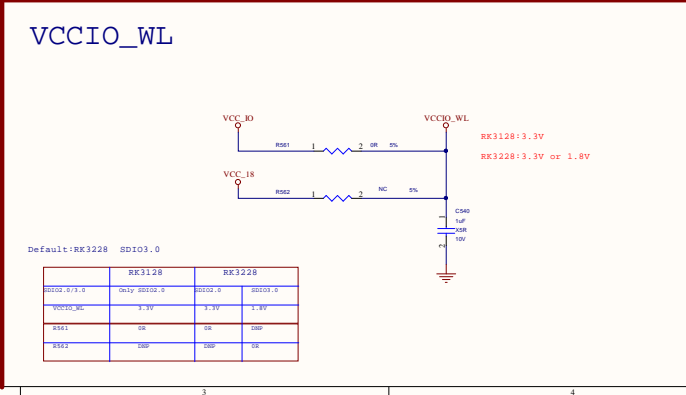
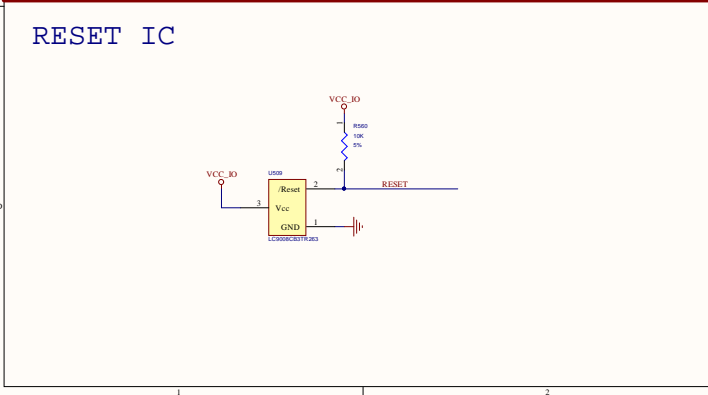
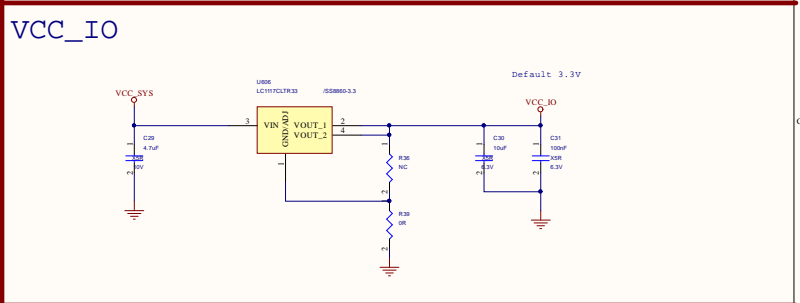
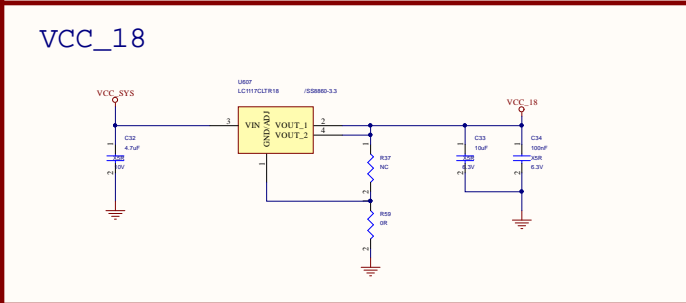
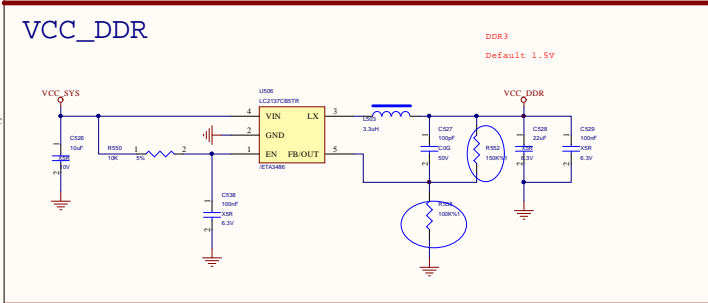
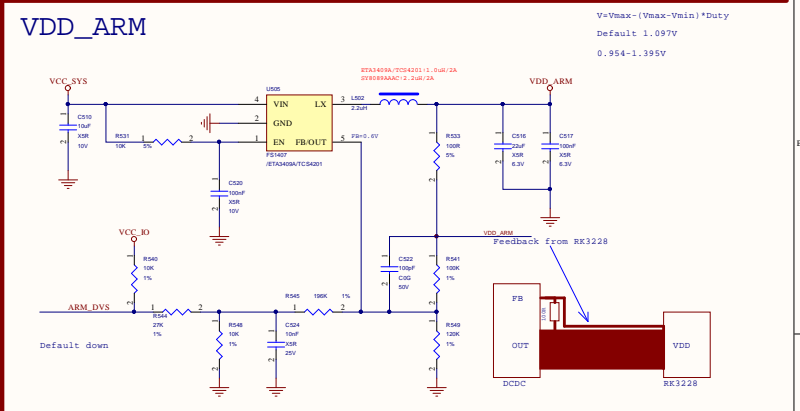
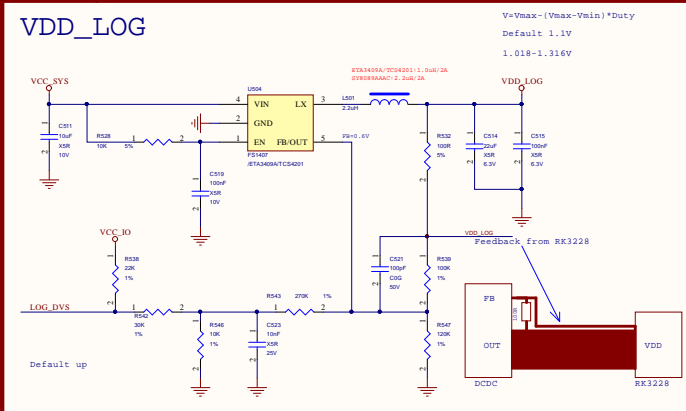
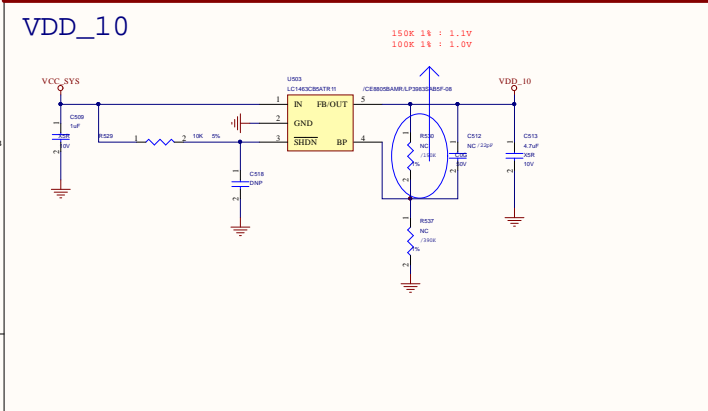
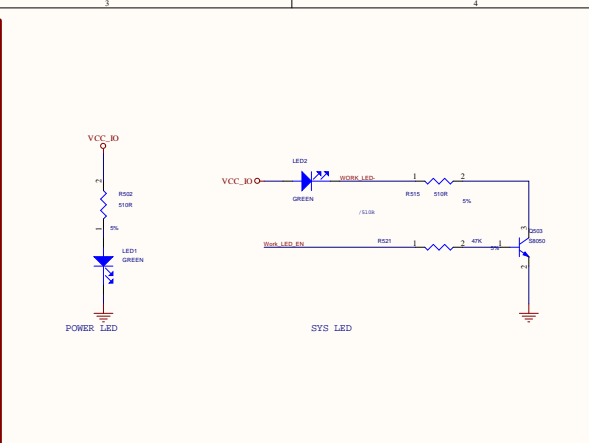
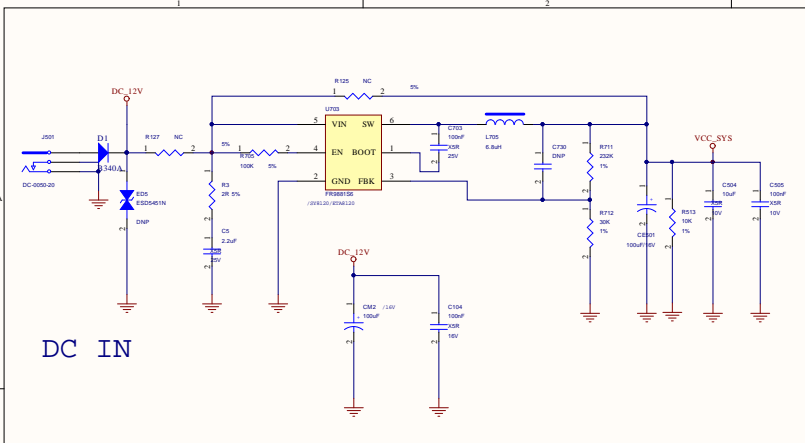


2020.04.20

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U1000K

ARM Core Power

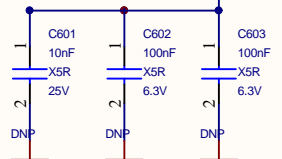
AVDD1  
AVDD2  
AVDD3  
AVDD4  
AVDD5

GPU/Logic Power

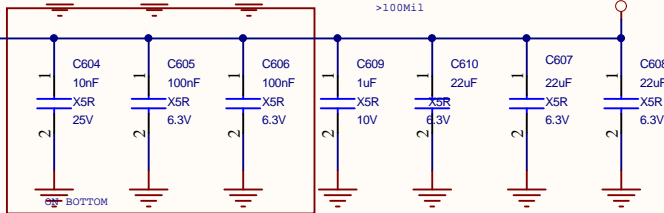
CVDD1  
CVDD2  
CVDD3  
CVDD4  
CVDD5  
CVDD6

RK3228A

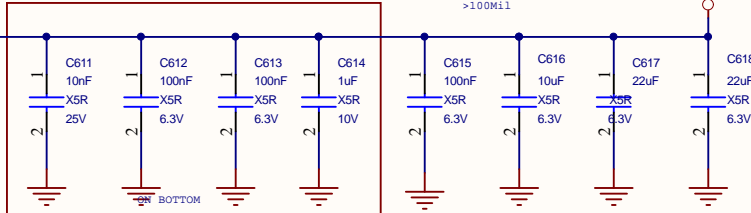
VDD\_ARM



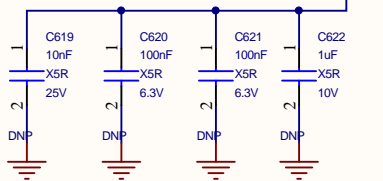
VDD\_ARM



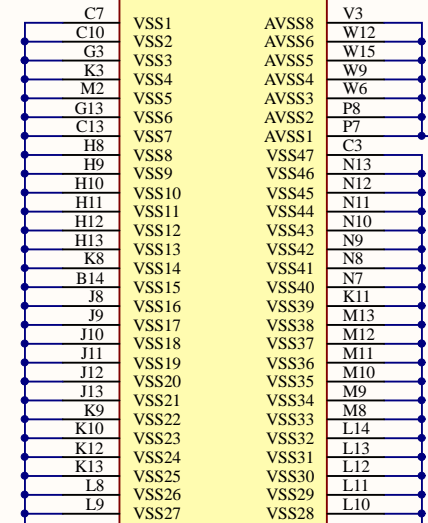
VDD\_LOG



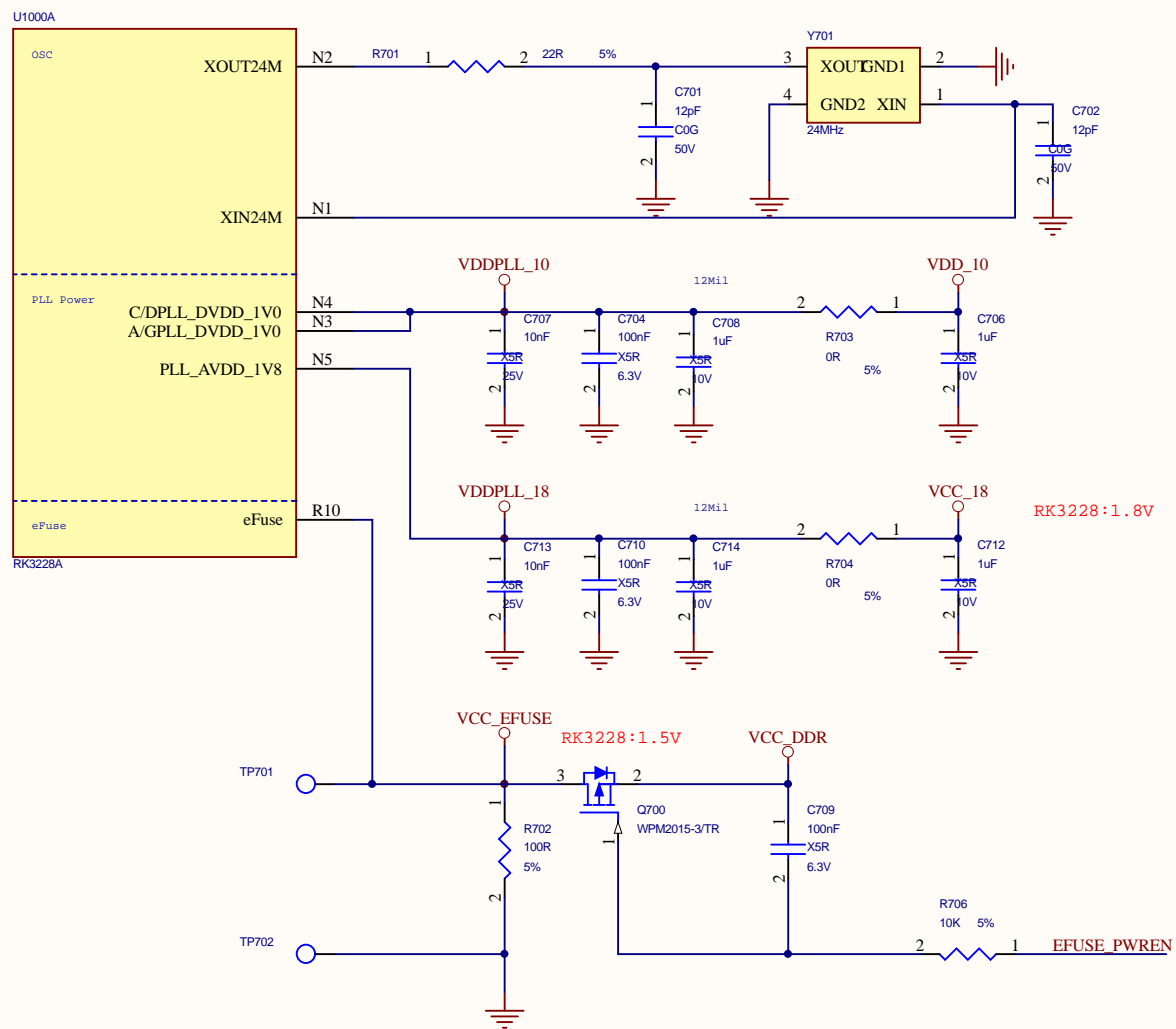
VDD\_LOG



U1000L



RK3228A







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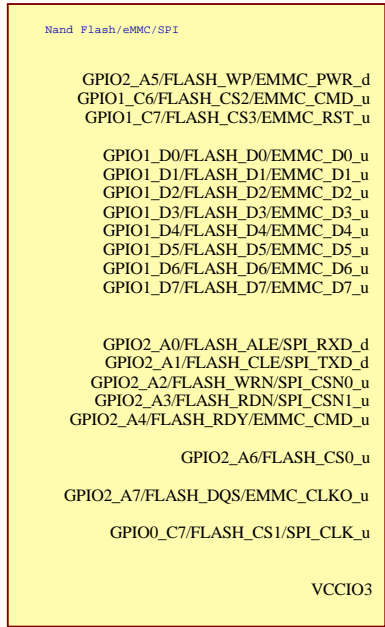
A

B

C

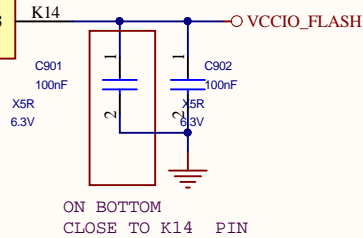
D

U1000D

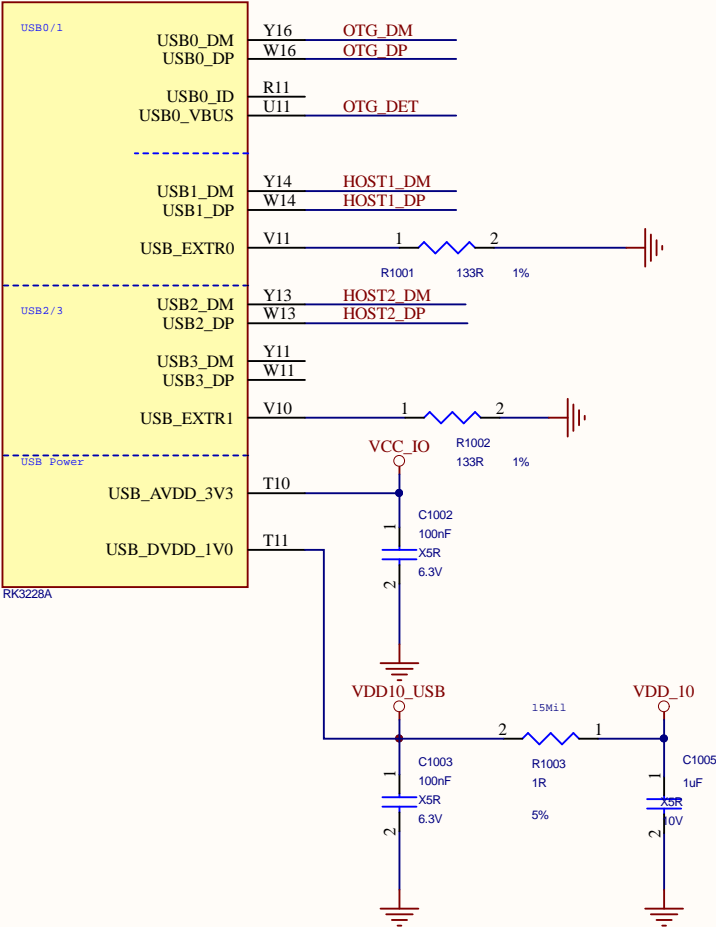


RK3228A

V19	FLASH_WP/EMMC_PWREN
U19	FLASH_CS2/EMMC_CMD
P19	FLASH_CS3/EMMC_RST
P16	FLASH_D0
U20	FLASH_D1
T19	FLASH_D2
T20	FLASH_D3
P18	FLASH_D4
R19	FLASH_D5
N15	FLASH_D6
P17	FLASH_D7
N16	FLASH_ALE
N17	FLASH_CLE
P20	FLASH_WRN
L15	FLASH_RDN
K17	FLASH_RDY/EMMC_CMD
L16	FLASH_CS0
N19	FLASH_DQS/EMMC_CLKO
L17	FLASH_CS1



U1000I



RK3128:LVDS

RK3228:USB

RK3128:SARADC IN2

RK3228:USB EXTR1



U1000F

R/L out

CODEC\_VCM

CODEC\_AOL

CODEC\_AOR

NC1

NC2

NC3

NC4

NC5

NC6

NC7

NC8

CODEC\_AVDD\_1V8

CODEC\_AVSS

CVBS out

VDAC\_IOUT

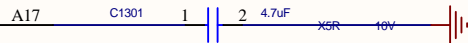
NC11

VDAC\_IREF

VDAC\_AVDD\_1V8

AVSS7

RK3228A



B17 AOL

B15 AOR

E14

C16

B18

D16

E16

A16

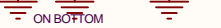
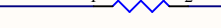
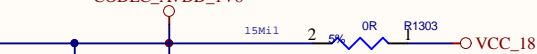
B16

C14

D13

D14

CODEC\_AVDD\_1V8



V7 VDAC\_OUT

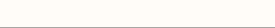
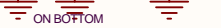
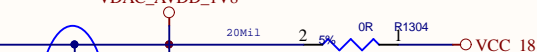
U7

U8 R1301 1 2 2K 1%

T7

T8

VDAC\_AVDD\_1V8



ON BOTTOM  
CLOSE TO T7 PIN

RK3128:3.3V

RK3228:1.8V

Default RK3228

RK3128:1K 1%

RK3228:2K 1%

Default RK3228

RK3128:3.3V

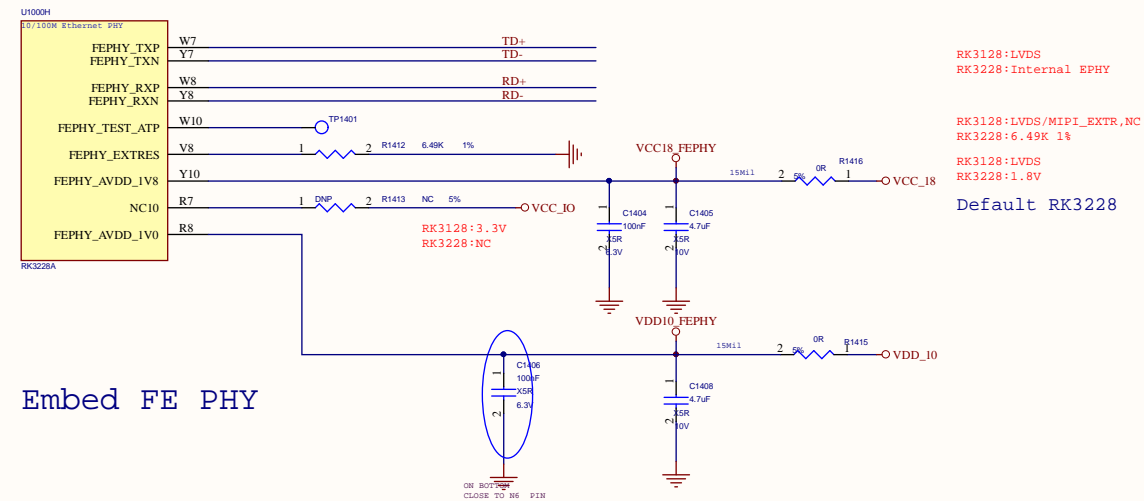
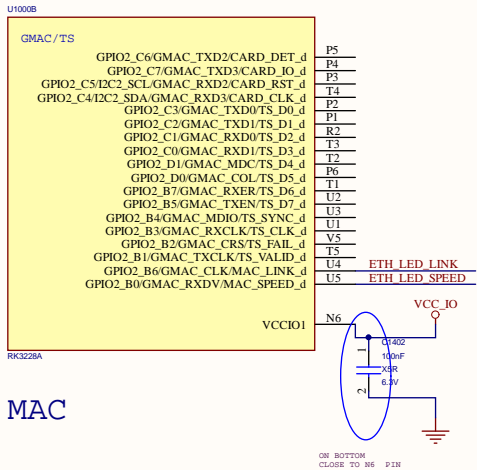
RK3228:1.8V

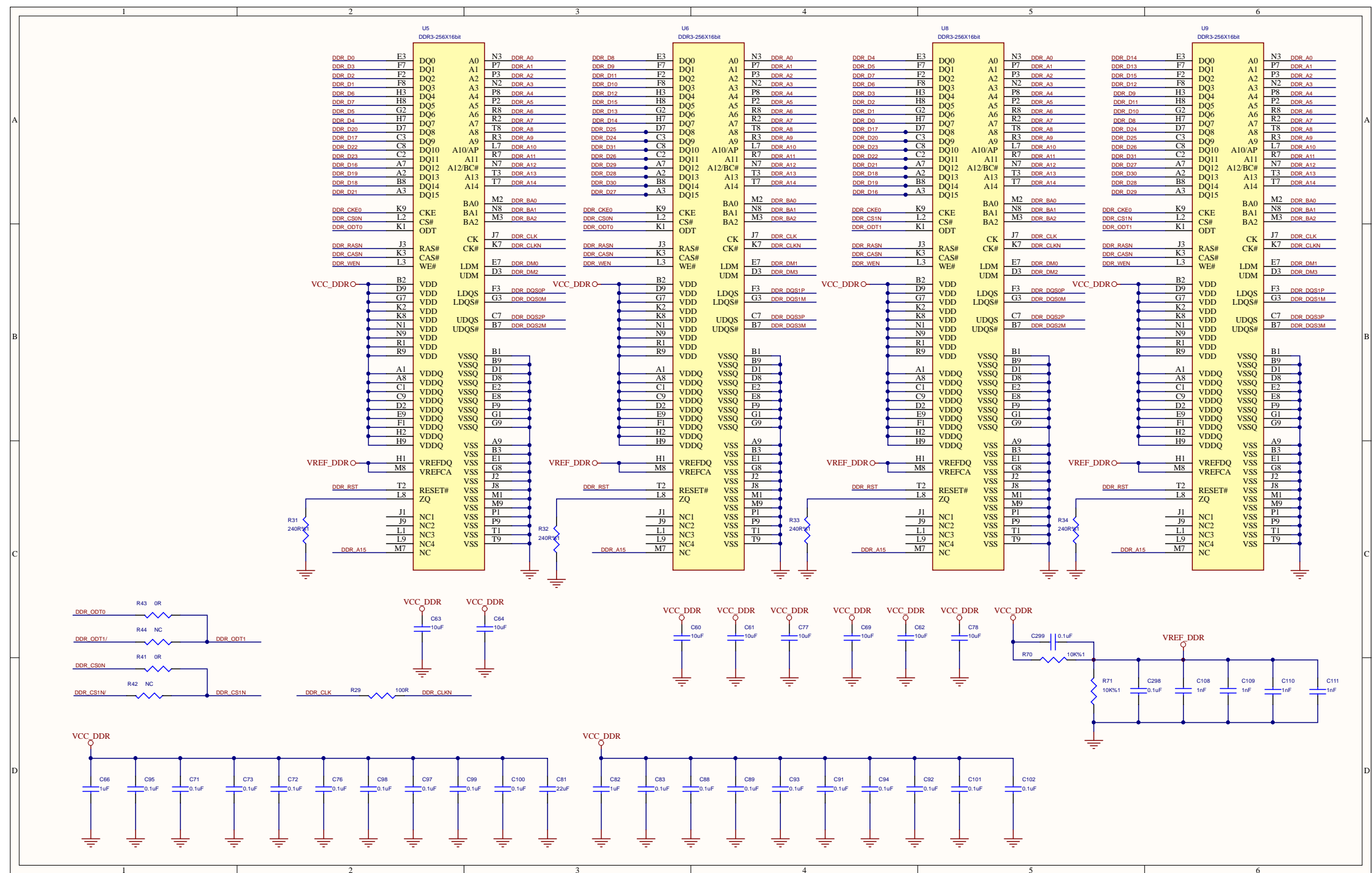
Default RK3228

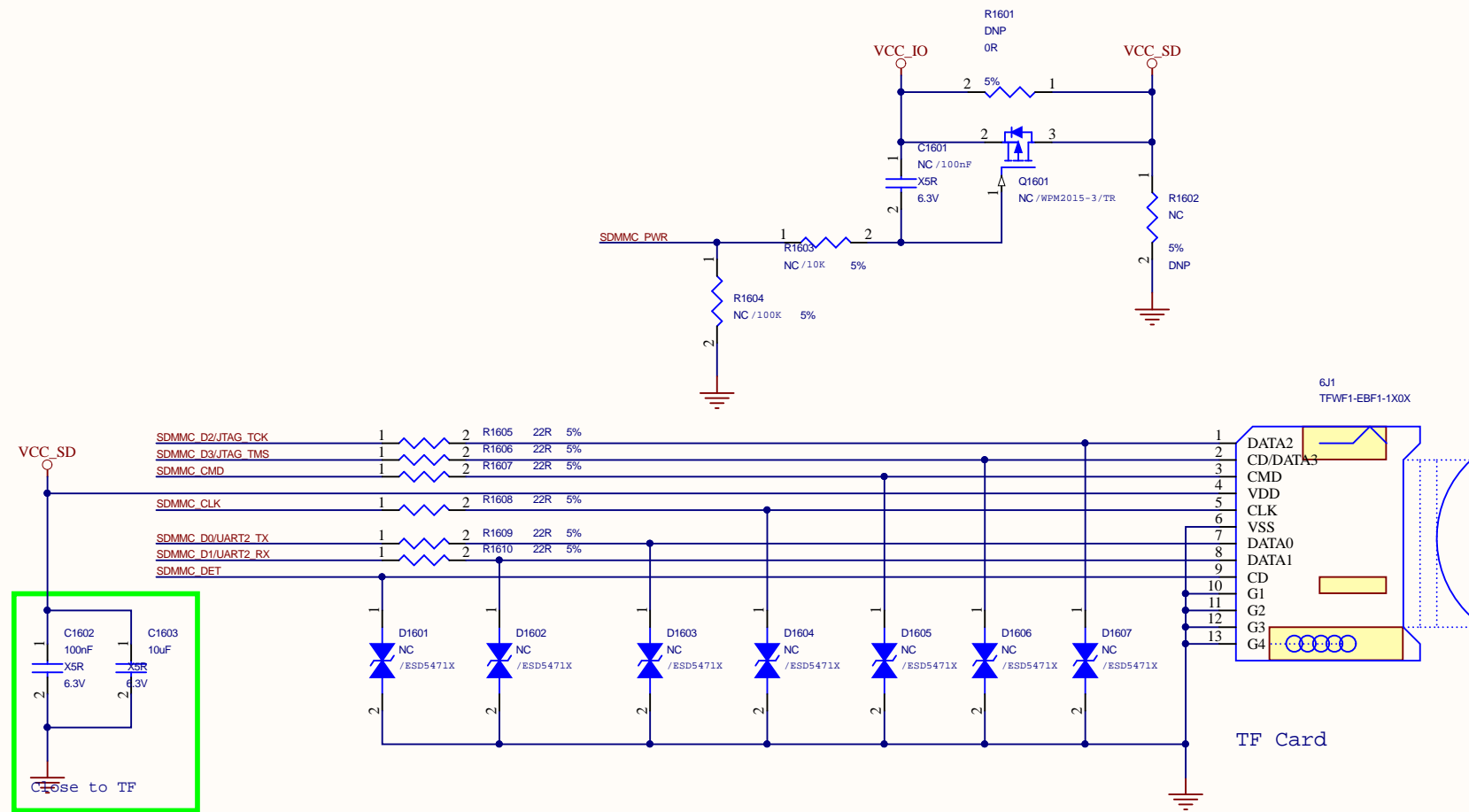
AOL TP706

AOR TP707

VDAC\_OUT TP708







A

B

C

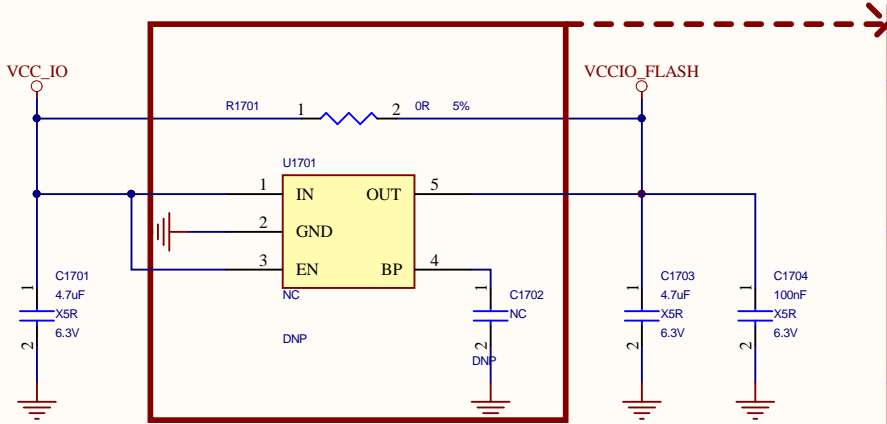
D

A

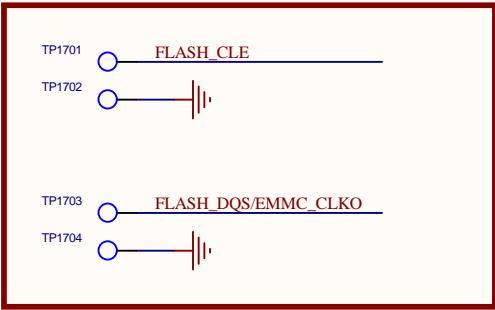
B

C

D



	Flash IO voltage		
eMMC (Default)	1.8V	U1701:PT5108E23E-18 R1701:DNP	Default
	3.3V	U1701:DNP R1701:0R	
Nand Flash	1.8V	U1701:PT5108E23E-18 R1701:DNP	
	3.3V	U1701:DNP R1701:0R	



Note:  
eMMC or Nand Flash Update.



VCCIO\_FLASH

RP1801

10K @eMMC

FLASH\_D0  
FLASH\_D1  
FLASH\_D2  
FLASH\_D3

RP1802

10K @eMMC

FLASH\_D4  
FLASH\_D5  
FLASH\_D6  
FLASH\_D7

R1803

10K 5%  
FLASH\_CS2/EMMC\_CMD  
@eMMC

FLASH\_DQS/EMMC\_CLKO

R1801 22R 5%

FLASH\_WP/EMMC\_PWREN

R1802 DNP  
@eMMC

C1806 100nF  
X5R 6.3V  
@eMMC

TP1801  
TP1802  
TP1803  
TP1804

U1801

FLASH\_D0  
FLASH\_D1  
FLASH\_D2  
FLASH\_D3  
FLASH\_D4  
FLASH\_D5  
FLASH\_D6  
FLASH\_D7  
FLASH\_CS2/EMMC\_CMD

DATA0  
DATA1  
DATA2  
DATA3  
DATA4  
DATA5  
DATA6  
DATA7  
CMD

W5

W6

U5

K2

R5

M9

M10

N10

U10

KLMAG2GEAC-B031

@eMMC 8GB

VCCQ1  
VCCQ2  
VCCQ3  
VCCQ4  
VCCQ5  
VCC1  
VCC2  
VCC3  
VCC4  
CLK  
RST\_n  
VDDi  
VSS1  
VSS2  
VSS3  
VSS4  
VSS5  
VSS6  
VSSQ1  
VSSQ2  
VSSQ3  
VSSQ4  
VSSQ5

AA5  
AA3  
Y4  
W4  
K6

U9  
TI0  
N5  
M6

U8  
R10  
P5  
M7  
H6  
T5

AA6  
AA4  
Y5  
Y2  
K4

VCCIO\_FLASH

C1801 100nF  
X5R 6.3V  
@eMMC

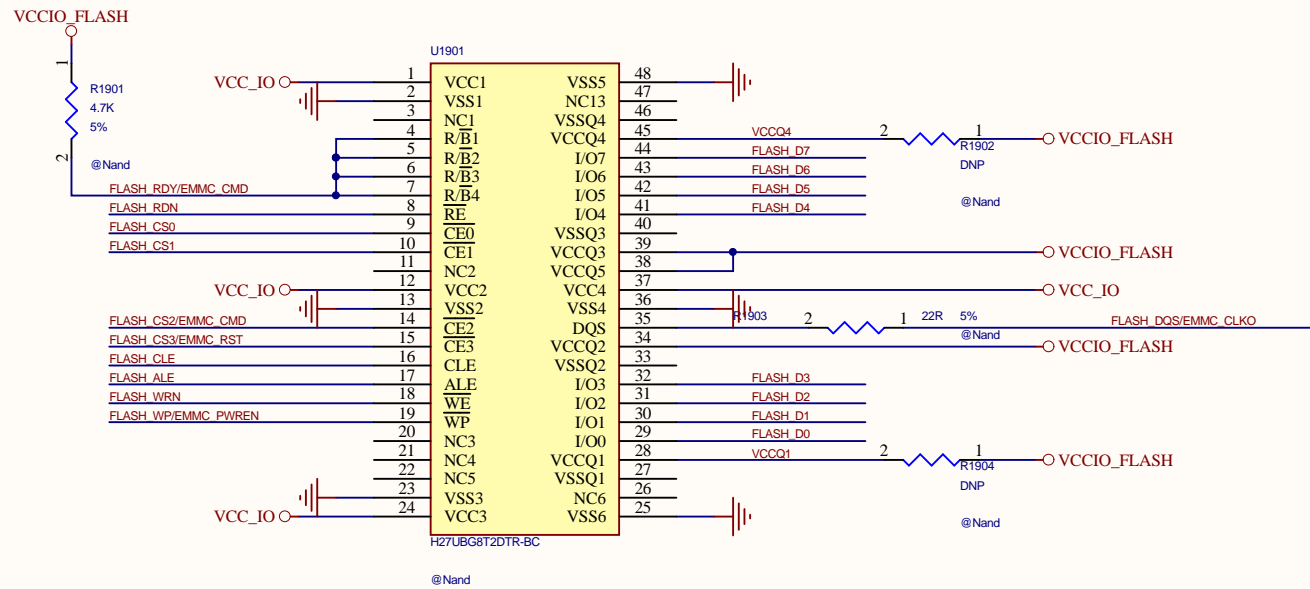
C1802 100nF  
X5R 6.3V  
@eMMC

C1803 100nF  
X5R 6.3V  
@eMMC

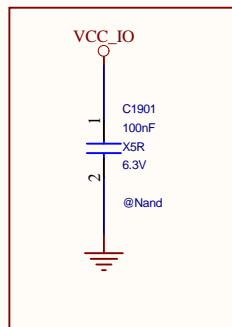
VCC\_IO

C1804 100nF  
X5R 6.3V  
@eMMC

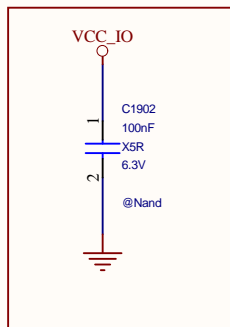
C1805 100nF  
X5R 6.3V  
@eMMC



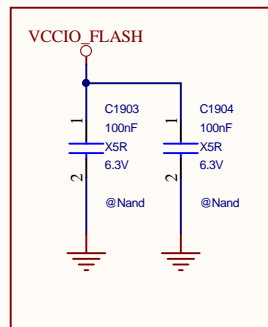
Note?if use toshiba and sandisk DDR mode,  
VCCQ1 and VCCQ4 must be connected to VCC\_IO .



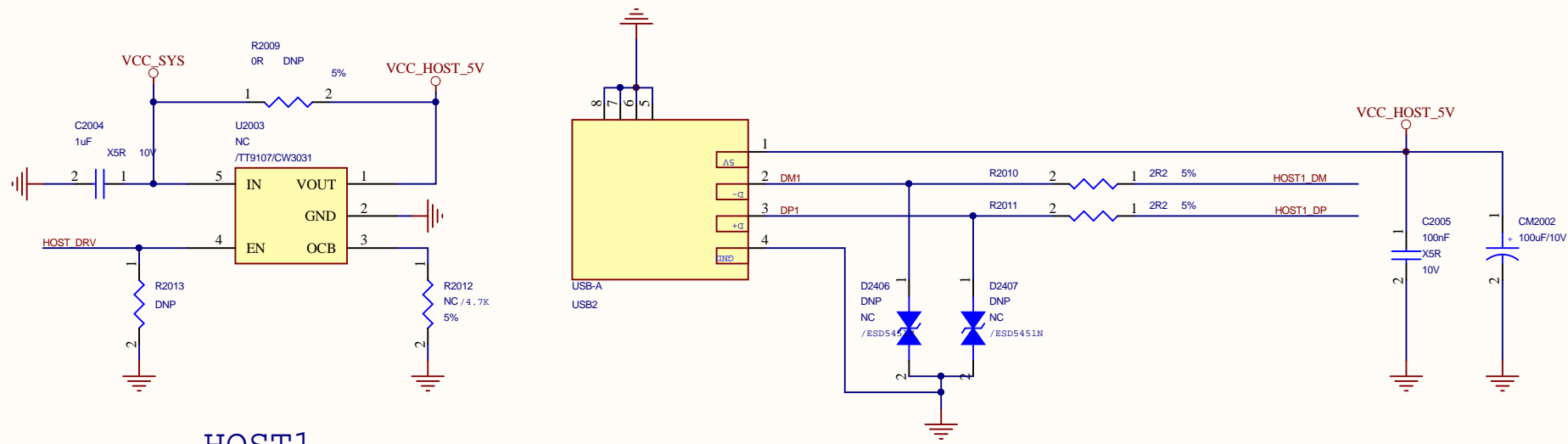
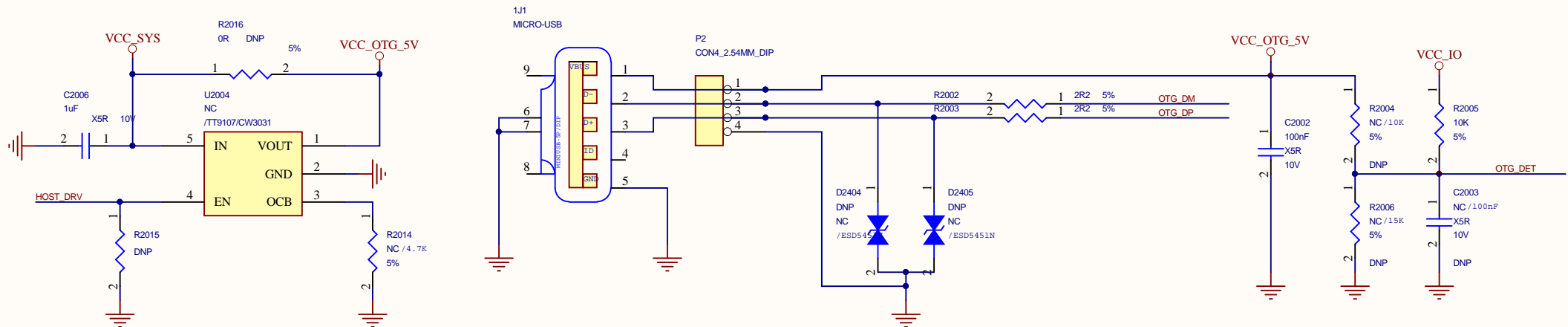
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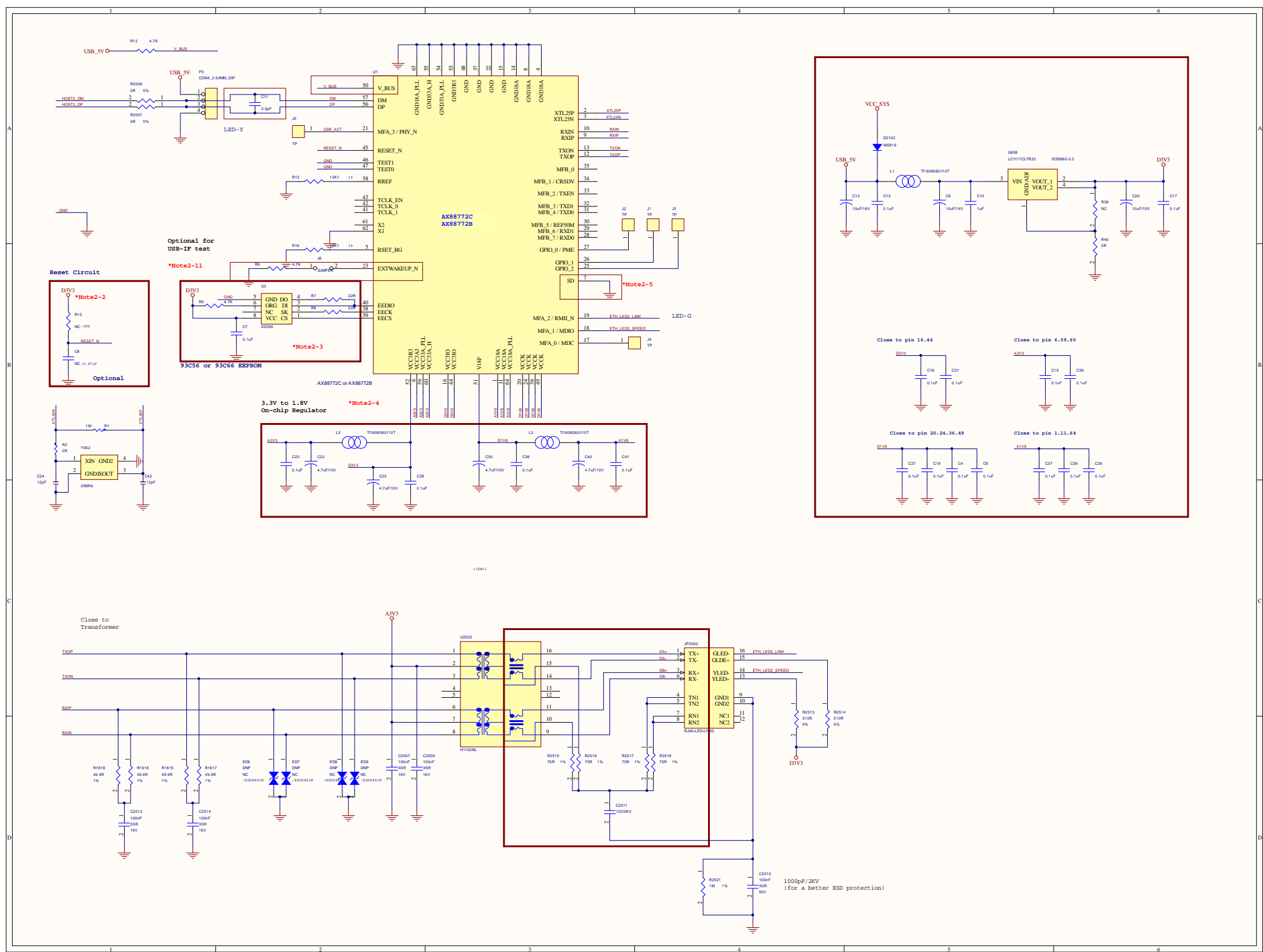


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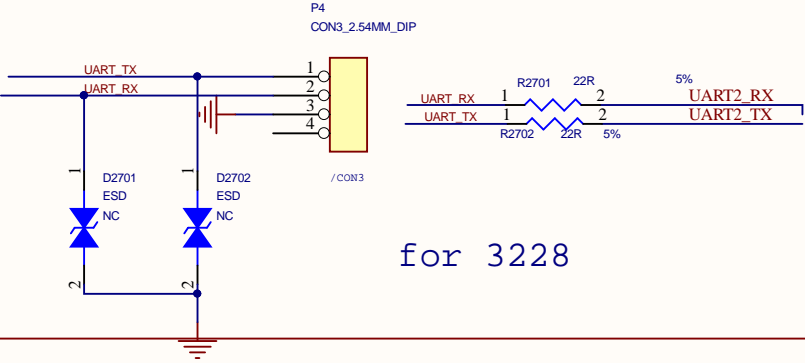


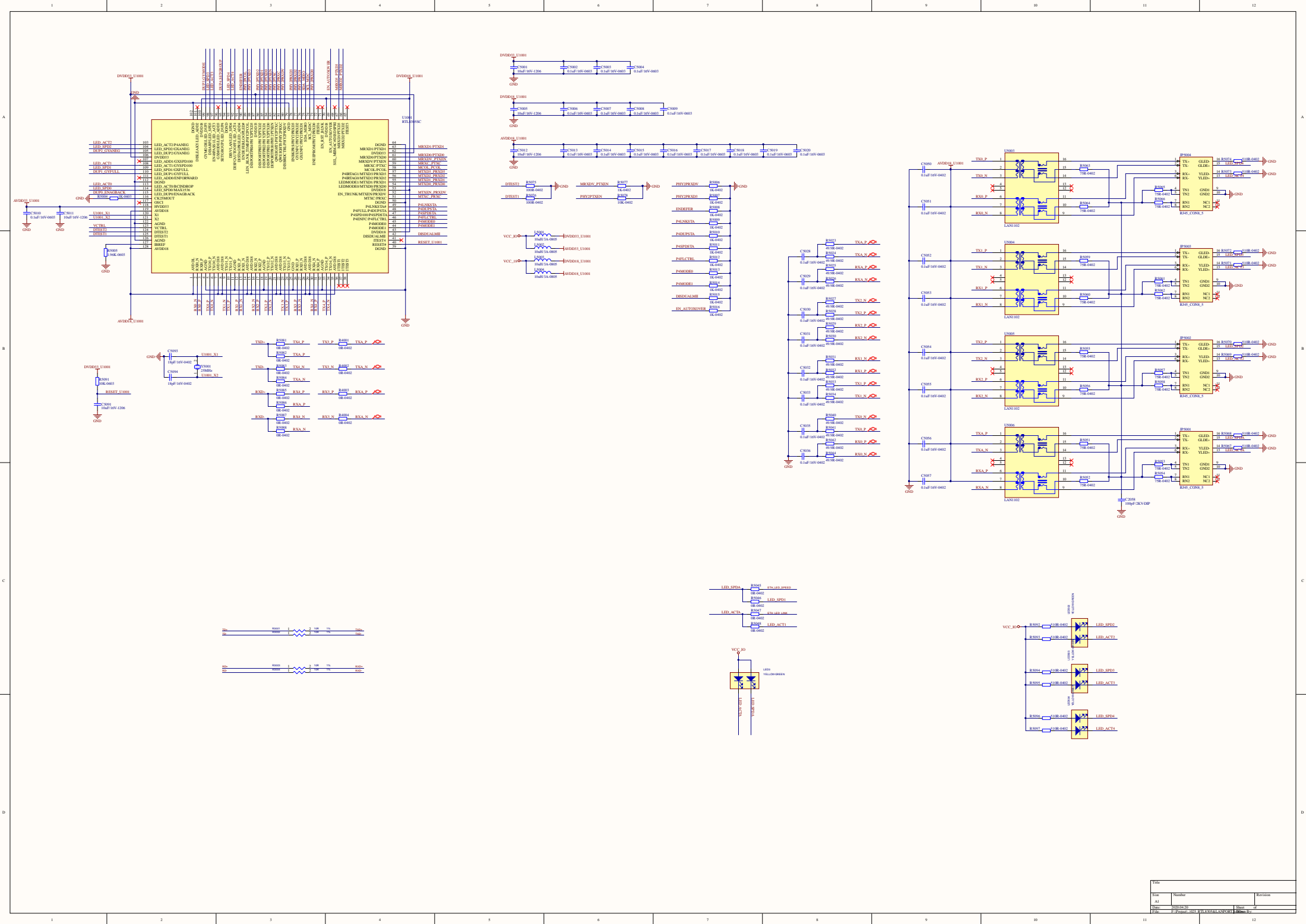
Close to PIN38,34





Debug UART2





Title		
Site	Number	Revision
A1		
Date	2020.04.20	Sheet of
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