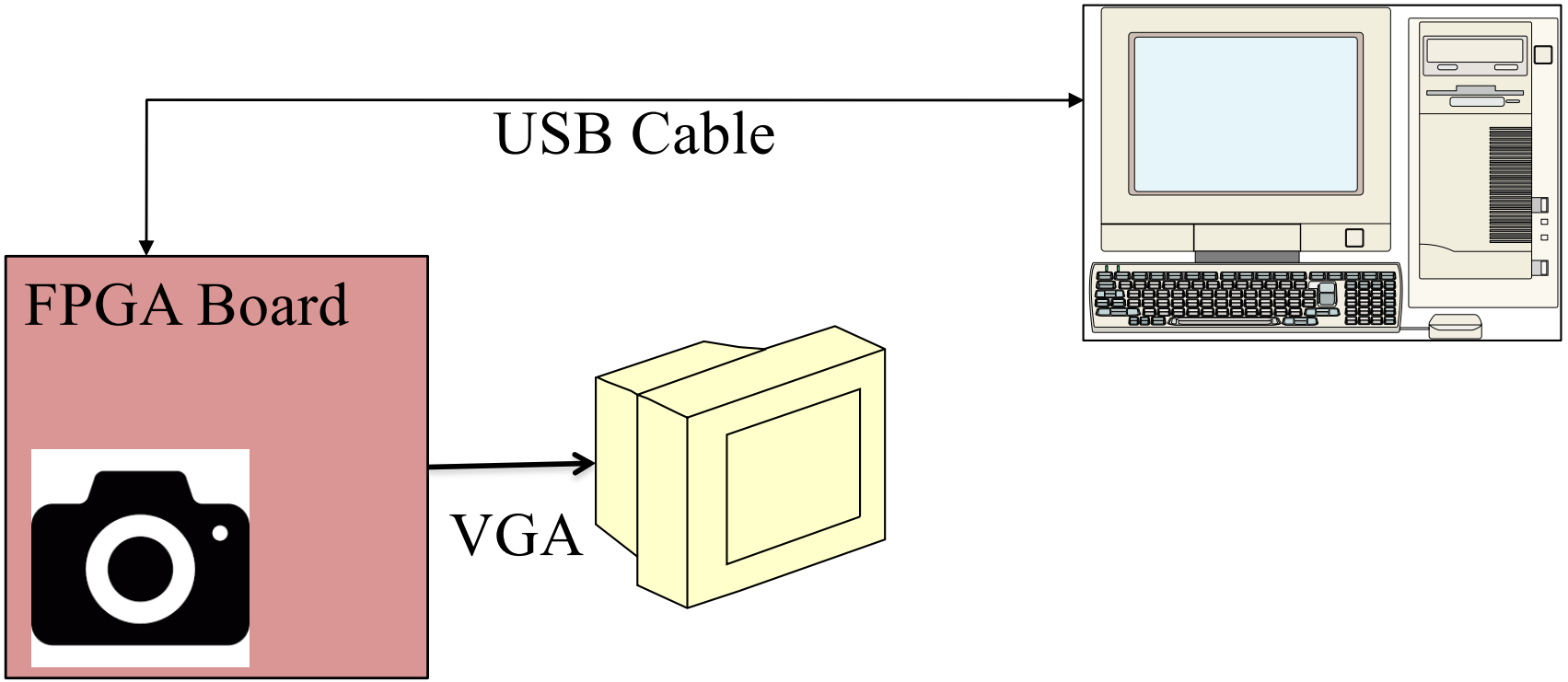
Mini Lab 2 Overview

Mini Lab 2

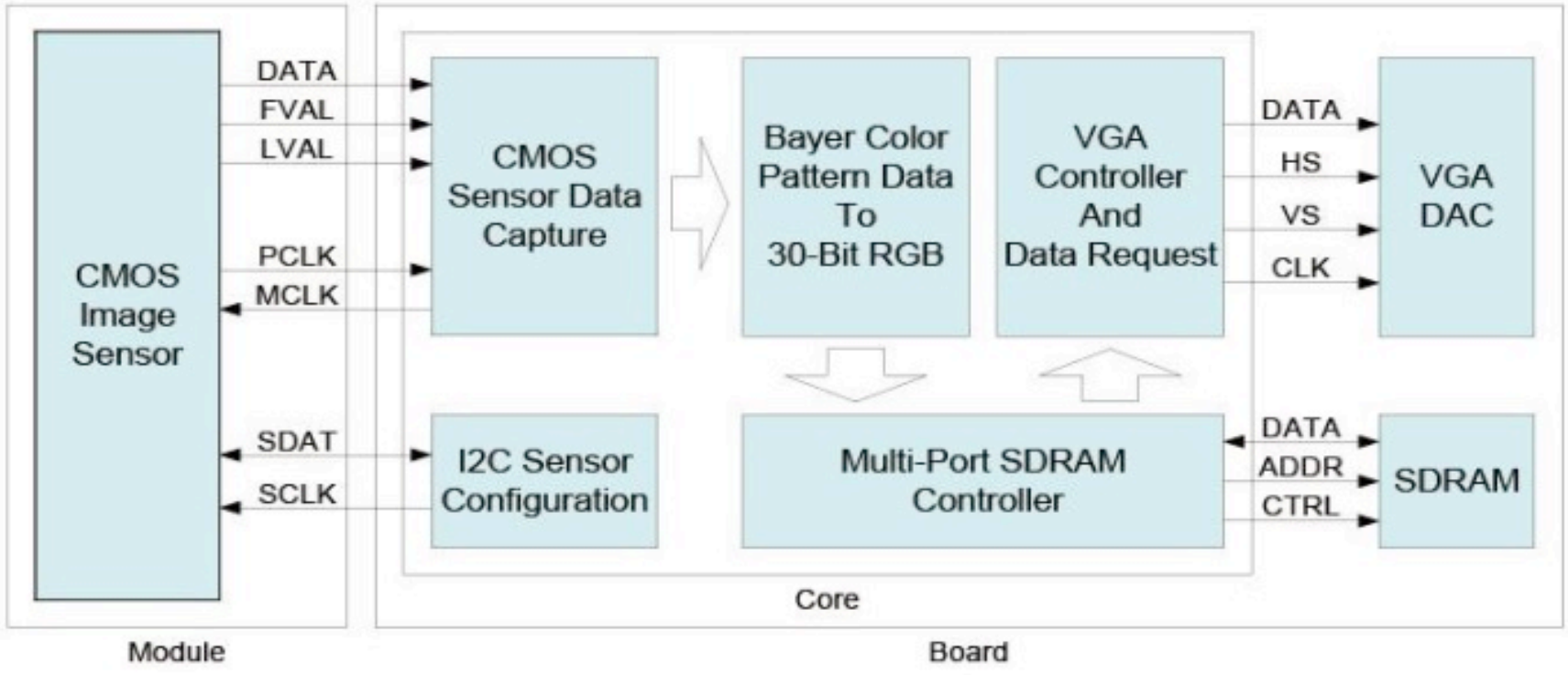
- Work through camera-to-vga demonstration project
- Add image processing step (2D convolution)
  - Detects edges in camera image
- Simulate the design to ensure correct performance
- Download the design and associated files and demonstrate correction functionality
- Prepare a report on your design

Lab Setup



USB port: Configuration download
VGA & Camera: Mini Project 2

Camera Reference Design



- Download and run DE1-SoC-CAMERA1.zip as your reference design to get a demo to capture with camera

Reference Design: UI (User Interface)

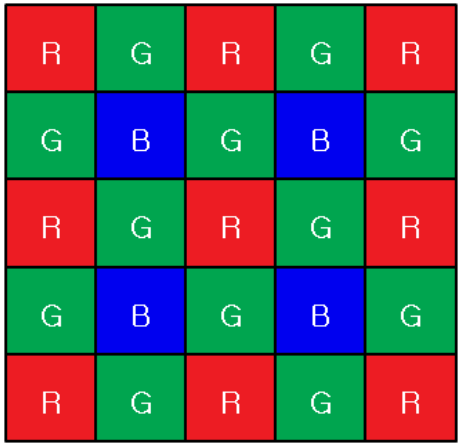
Component	Function Description
KEY[0]	Reset circuit
KEY[1]	Increment or decrement the exposure time (based on SW[0])
KEY[2]	Stop capturing images
KEY[3]	Resume capturing images
SW[0]	Off: Increase exposure time with KEY[1] On: Decrease exposure time with KEY[1]
SW[9]	On: ZOOM Off: normal
HEX[7:0]	Displays frame count since reset

Reference Design: Camera Interface

Pin	Type	Description
D5M_D	Output	12 bit Data Signal
D5M_FVAL	Output	Frame Valid
D5M_LVAL	Output	Line Valid
D5M_PIXLCLK	Output	D5M PLL clock synchronized to D and *val signals
D5M_RESET_N	Input	Reset
D5M_SCLK	Input	I2C Serial Clock
D5M_SDATA	InOut	I2C Serial Data Bus
D5M_STROBE	Output	Active During Exposure
D5M_TRIGGER	Input	Triggers image capture when set to 1
D5M_XCLKIN	Input	Reference Clock

- Please be careful with ribbon cable & connectors

Reference Design: Demosaicing

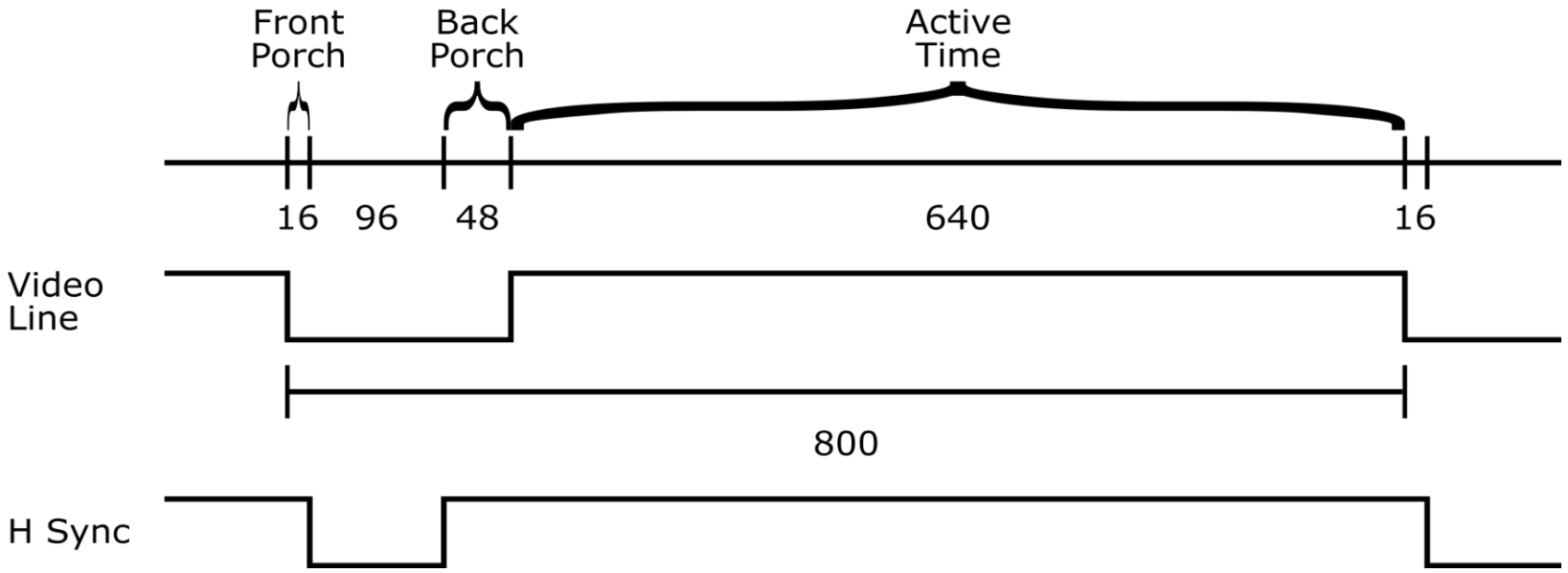


- Camera captures in oversampled Bayer format
  - 1280x960 pixels (cols x rows)
- Demosaicing module converts to RGB
  - At even pixels adjacent pixels are combined
  - Resulting RGB image is 640x480
  - Pixels stored in on-board SDRAM

VGA Interface

- VGA standard based on serial transmission of pixels, row by row, frame by frame
- HSYNC and VSYNC control signals delineate rows and frames
  - Blanking intervals at HSYNC/VSYNC are present to allow time for CRT to reposition to beginning of next row or top of next frame
  - Not needed in modern LCD/LED displays, but…interfaces live on long after the underlying technology has disappeared

VGA Row Timing



- Hsync triggers new row of pixel data w/period = 800 pixel clocks
- Front/back porch give display hardware time to reach after/before new data
- Blanking interval between rows (Hsync low)
- Timing parameters vary for other resolutions/frame rates

VGA Frame Timing

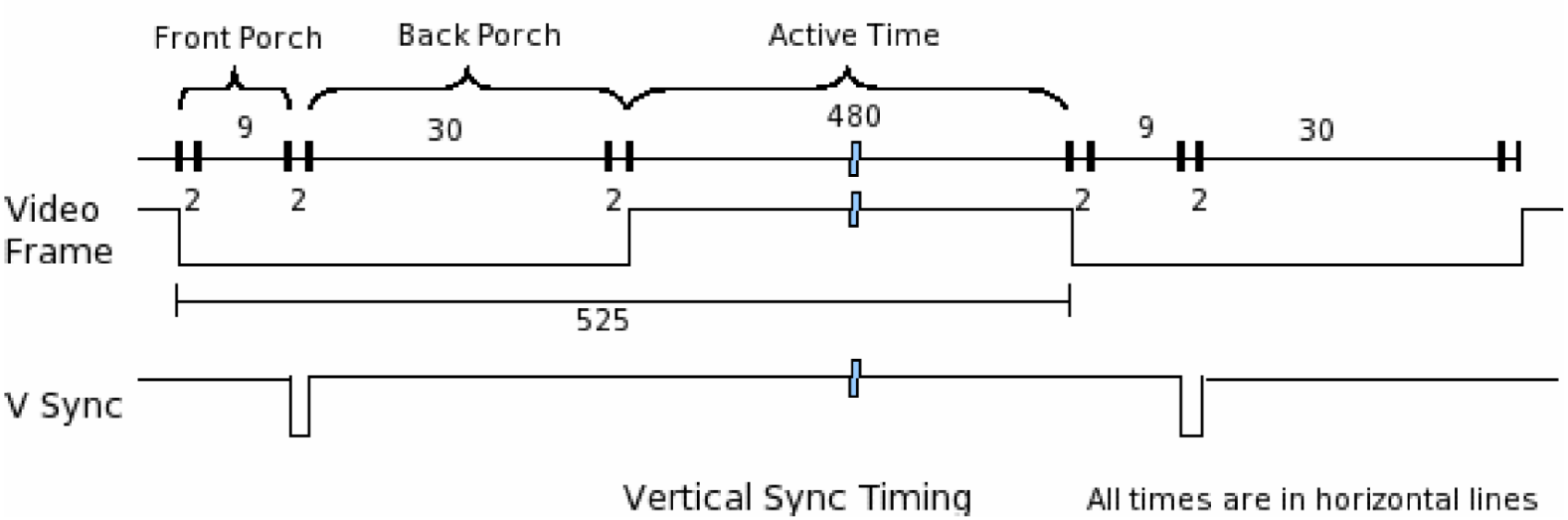
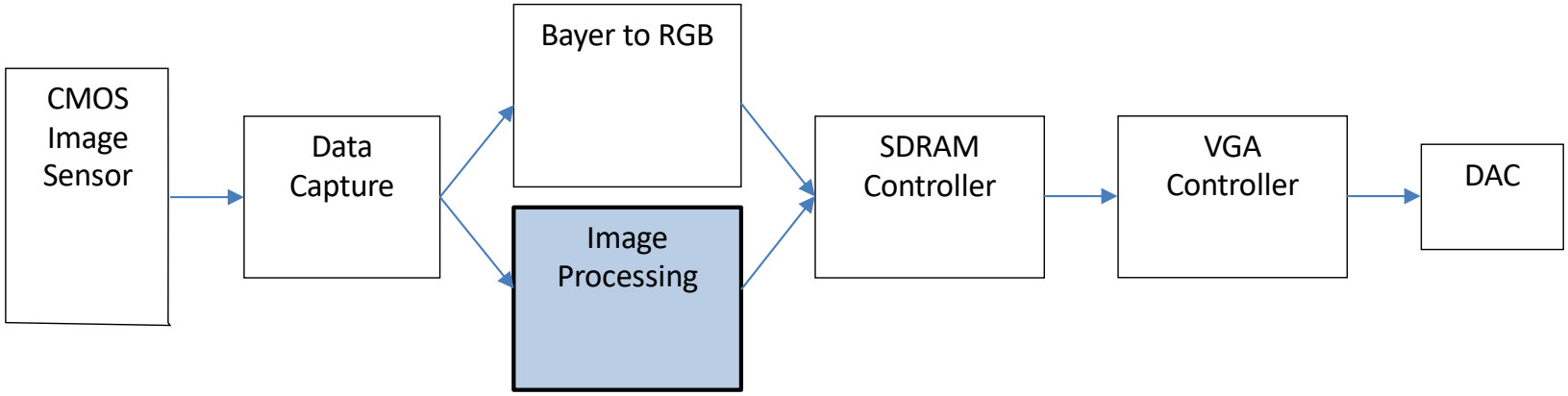


Figure 3: Vertical Sync Timing, © 2008, Mac A. Cody

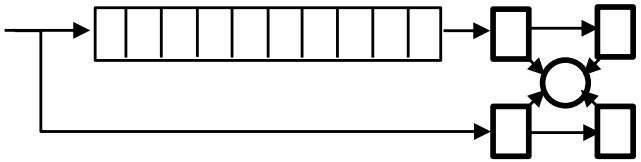
- VSync triggers new frame of pixel data w period = 525 rows
- Front/back porch give display hardware time to reach after/before new data
- Blanking interval between frames (VSync low)
  - Used to embed closed captioning data in NTSC TV broadcasts

What you add: Image Processing Module



- Image processing module is gray scale
  - First need to create a gray scale image by:
    - Average neighboring pixels (RGB) for input
    - Duplicate gray scale value to all three channels (RGB) on output

What you add:
Grey Scale Conversion



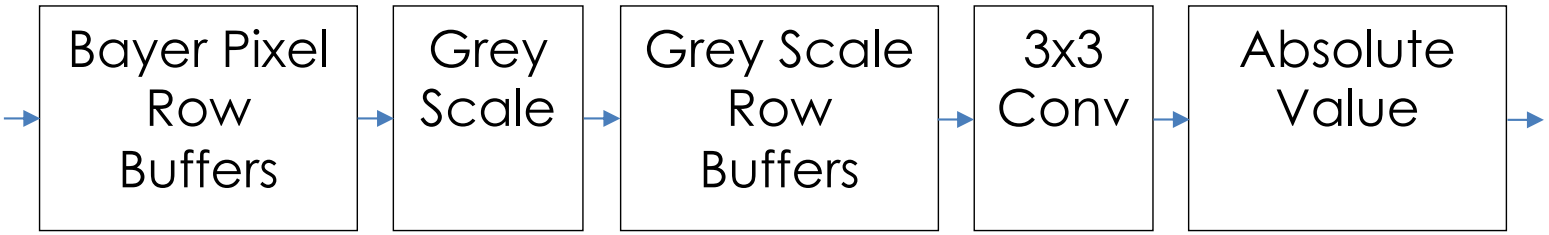
- Need to buffer entire row to interpolate in both dimensions.

What you add:
Image Processing Module

$$y[i][j] = \sum_{m=-1}^{1} \sum_{n=-1}^{1} x[i-m][j-n] \times h[m][n],$$

- 3x3 convolution applies mask to neighboring input pixels (*x*) to compute value of current output pixel (*y*).
- h[m][n] values set for Sobel Edge detector

What you add: Image Processing Pipeline



- Need to buffer at least two grey scale rows for 3x3 convolution
- Sometimes convolution returns negative result: take absolute value

What you add:
Sobel Edge Detectors

Sobel

-1	0	1
-2	0	2
-1	0	1

Sobel

-1	-2	-1
0	0	0
1	2	1

- Read miniproject 2 handout carefully

Mini Lab 2 Submission

Your submission should be a single zip file including

- Well commented Verilog code. Please clearly indicate which Verilog files are written by you, which files are generated, and which files are copied.
- Testbench for the image processing module.
- The Quartus flow summary exported to an rpt file. Make note of the utilization of ALMs, BRAM, and DSP blocks in the report.
- Report describing your implementation, test bench, problems encountered and solutions for those problems (if you solved them).