Project Stage

Jake Neau
Nathan Woolf
Sam Cooper

Project Motivation

This project is a simple implementation of a neuron that can be used in a neural network. It takes in a series of weights and biases, and returns an output value based on some activation function. Our design is a small one, but a larger neuron could be used in a neural network for tasks such as image recognition. Our design is made up of multipliers which multiply inputs by some trained weights used to tune the neuron, adders which turn all multiplied values into a single output, and a mux to implement the ReLU activation function for a neuron. Most of our transistors are sized with a beta ratio of 1.5 to ensure that rise times and fall times are near equal. The exception are our mirror adder cells which were sized with a beta ratio of 1 to stay more compact.

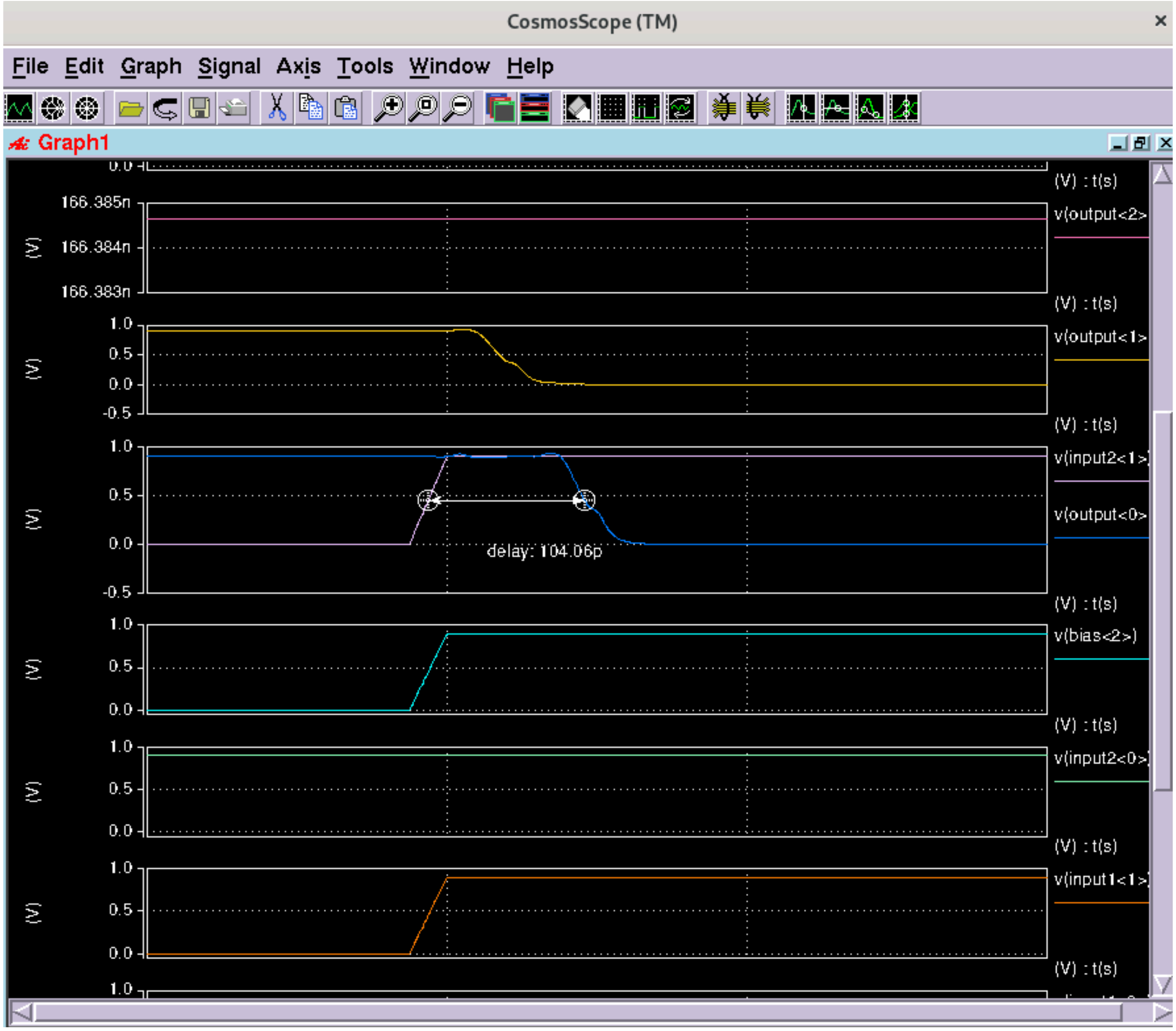
Test Case ID	Input Combination [x1, w1, x2, w2, b]	Expected Output [y]	Actual Output [y]	Pass /Fail	Notes
1	[0, 0, 0, 0, 0]	000	000	P	Verifying no glitches
2	[1, 1, 1, 1, 1] [01, 01, 01, 01, 001]	011	011	P	Testing each output scenario
3**	**[-1, 1, -1, 1, -1] [11, 01, 11, 01, 111]**	**000**	**000**	**P**	**Worst case delay**
4	[0, -1, 1, 1, 0] [00, 11, 01, 01, 000]	001	001	P	Testing each output scenario
5	[1, 1, 0, 1, 1] [01, 01, 00, 01, 001]	010	010	P	Testing each output scenario
6	[0, -1, 1, 0, -1] [00, 11, 01, 00, 111]	000	000	P	Random test
7	[-1, 1, -1, 1, 1] [11, 01, 11, 01, 001]	000	000	P	Random test

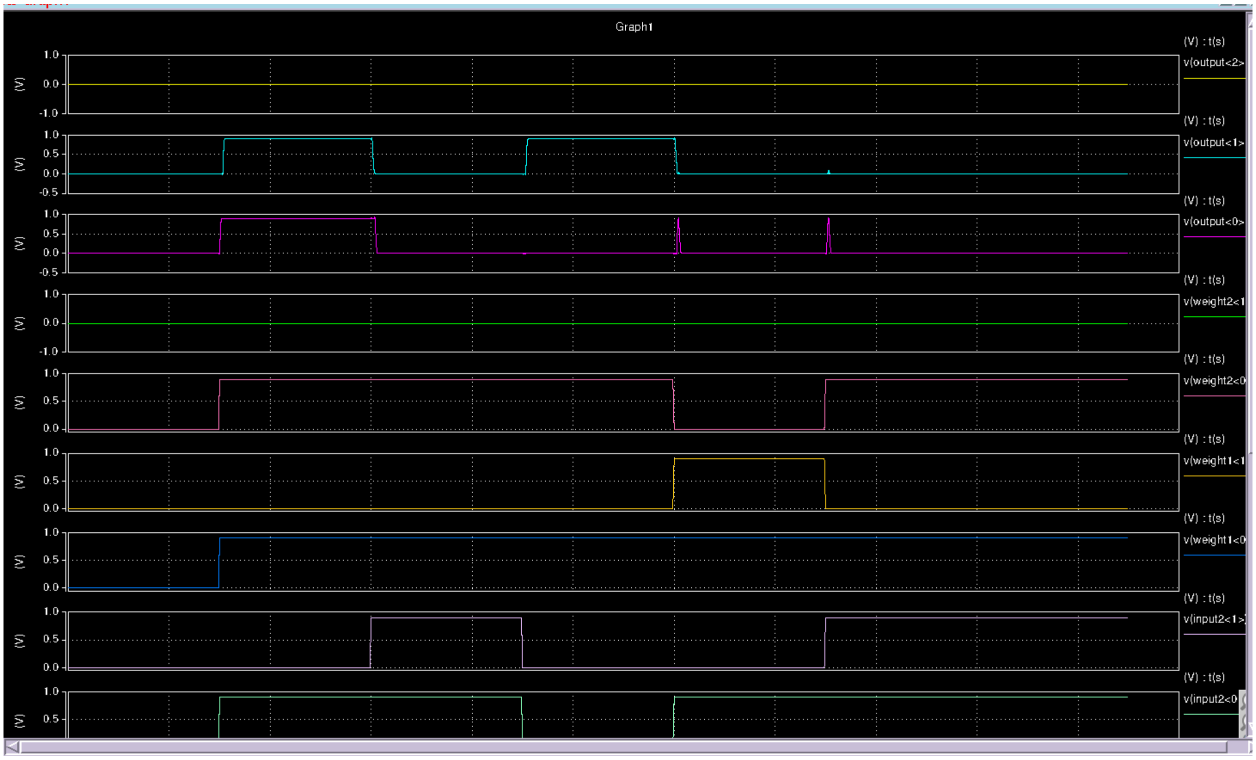
****Worst Case Input Combination**

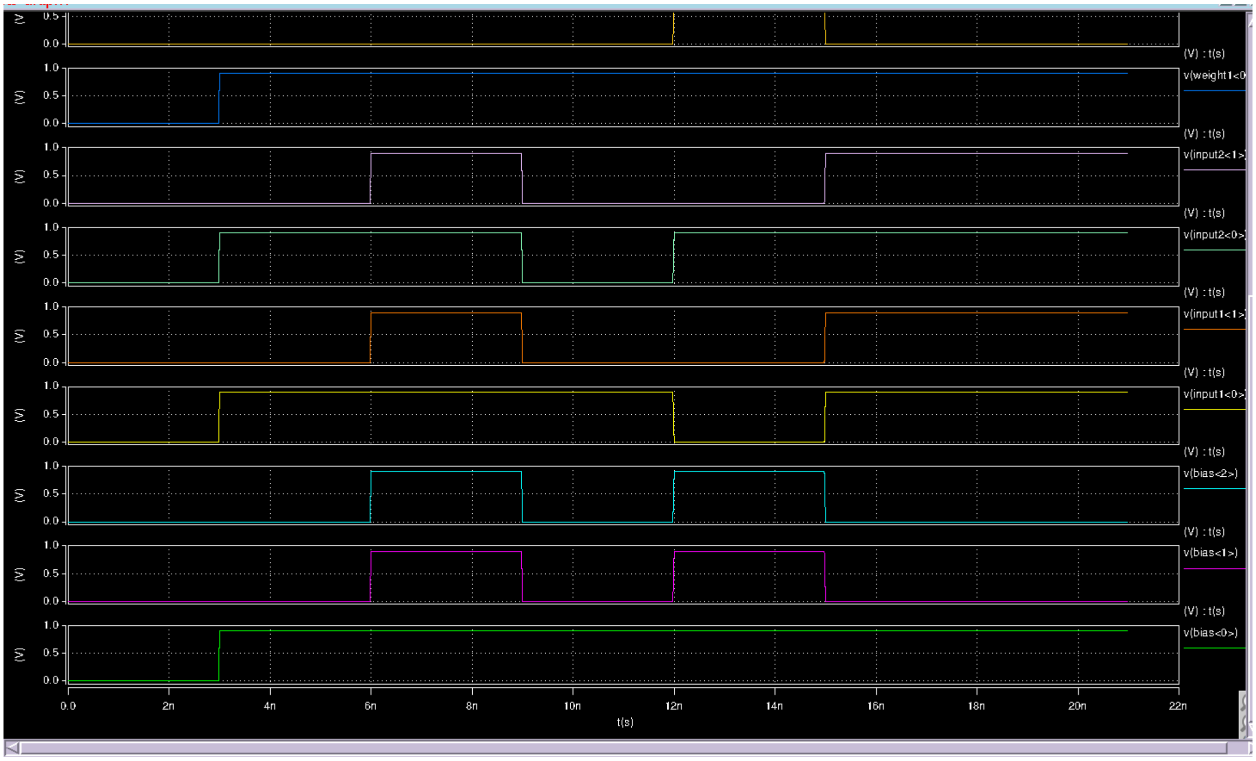
Our worst case input combination was determined to be the inputs listed in row 3 of our test simulation table. This was determined to be the case due to the cells demand of carry out signals from both adders as well as the critical path being used in the multiplication units.

The screenshot below captures the critical delay of our gate of 104.06ps. The screenshot also captures our expected output of 000 on the signals output<2> output<1> and output<0> following the falling edge of signals on output<1> and output<0>.

With the observed delay of 104.06ps, our T is approximately 9.615GHz.




Graph1
(V) : t(s)
v(output<2>
(V) : t(s)
v(output<1>
(V) : t(s)
v(output<0>
(V) : t(s)
v(weight2<1
(V) : t(s)
v(weight2<0
(V) : t(s)
v(weight1<1
(V) : t(s)
v(weight1<0
(V) : t(s)
v(input2<1>
(V) : t(s)
v(input2<0
(V)
1.0
0.5
0.0
-0.5
-1.0


(V) : t(s)
v(weight1<0
(V) : t(s)
v(input2<1>)
(V) : t(s)
v(input2<0>)
(V) : t(s)
v(input1<1>)
(V) : t(s)
v(input1<0>)
(V) : t(s)
v(bias<2>)
(V) : t(s)
v(bias<1>)
(V) : t(s)
v(bias<0>)
(V)
1.0
0.5
0.0
0.0
2n
4n
6n
8n
10n
12n
14n
16n
18n
20n
22n
t(s)

Output glitches

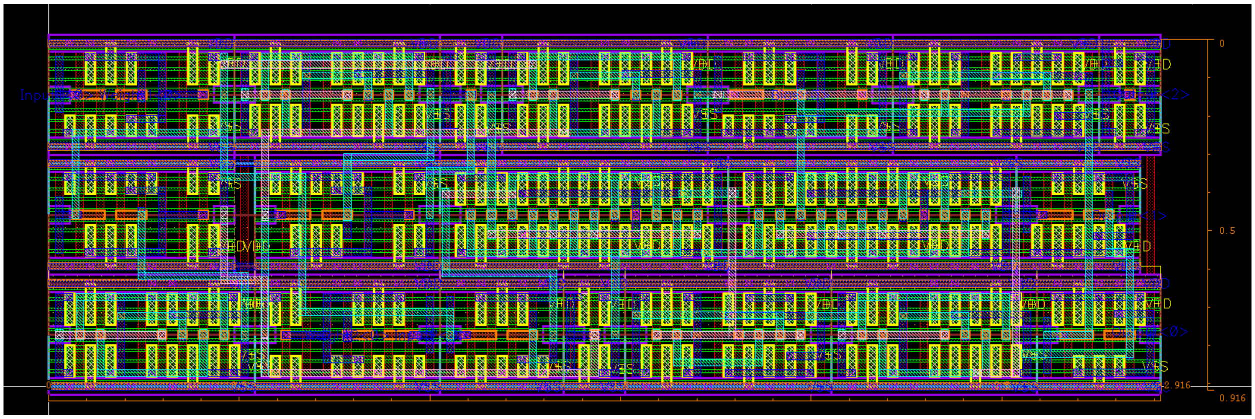
As shown in our output waveforms above, it is apparent our design had rather extreme glitches in the post layout simulation. Our team began this project with a standard cell approach, creating the gate schematics required to perform the logic functions demanded of the neuron. As we moved from milestone 2 to milestone 3, we realized that we could make extreme optimizations by implementing complex gates such as the mirror adder, XOR, and XNOR gates. As we investigated these solutions, we found it inherently easier to design these around a beta ratio of one, where our NAND, AND, NOR, OR, and other ‘simpler’ gates we designed earlier in the project had a beta ratio of 1.5.

Our team spent countless hours attempting to resolve these glitches. We first tried to add inverters to the earlier arriving signals to increase the delay of the path which was causing our outputs to temporarily glitch. We began with trying to include inverters throughout the design in order to increase the drive strength through some of the lower driving gates. We eventually pivoted to changing all of our gates with beta ratios of 1.5 to 1, however we were unable to pass LVS in the time allotted for the project. We are submitting a backup of our project before these changes were attempted.

Having completed this project in its entirety and struggling through the design process associated with performing custom design in Cadence Virtuosos, our team can comfortably say that if we had the chance to do this project over again, we would take a drastically different approach from the start. With the knowledge we have now, we believe that if we had more time, we could create a more reliable cell with less delay with marginally more area, if not the same area.

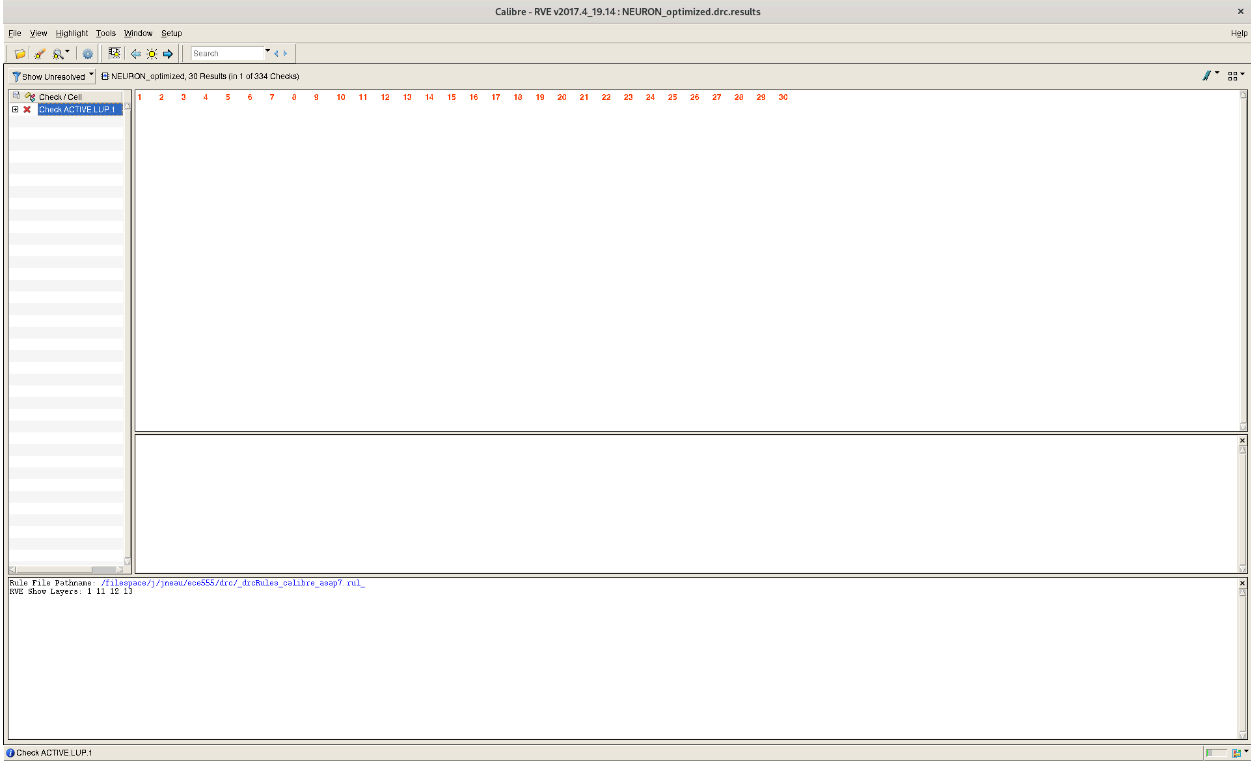
Boundary Report

0.916 µm (Height) x 2.916 µm (Width) = 2.671 µm^2 (area)



You can see in our screenshots that when our checks are set to “Show Unresolved” ACTIVE.LUP.1 is the only error, and we are supposed to ignore that one

Neuron



Calibre - RVE v2017.4_19.14 : NEURON_optimized.drc.results
File View Highlight Tools Window Setup
Help
Search
Show Unresolved
Check / Cell

NEURON_optimized, 30 Results (in 1 of 334 Checks)

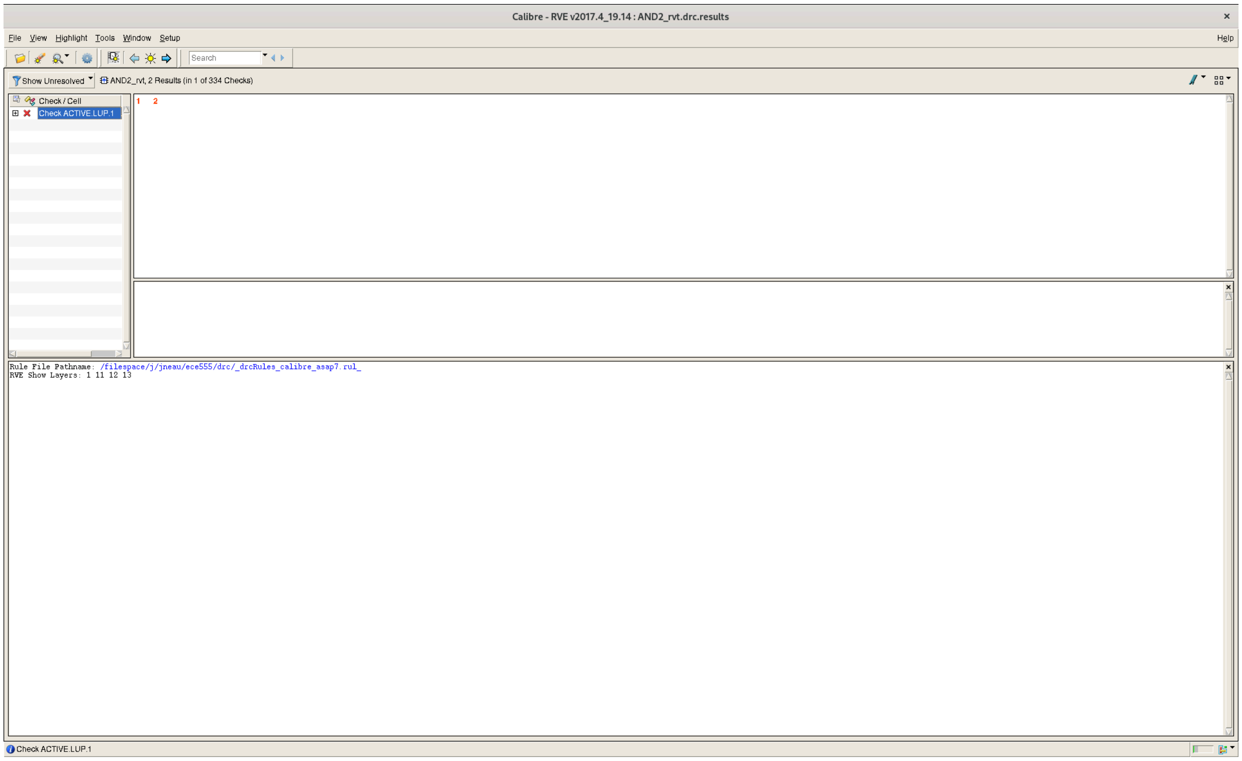
Check ACTIVE.LUP.1

1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30

```
Rule File Pathname: /filespace/j/jneau/ece555/drc/_drcRules_calibre_asap7.rul_
RVE Show Layers: 1 11 12 13
```

Check ACTIVE.LUP.1

AND Gate



Calibre - RVE v2017.4_19.14 : AND2_rvt.drc.results

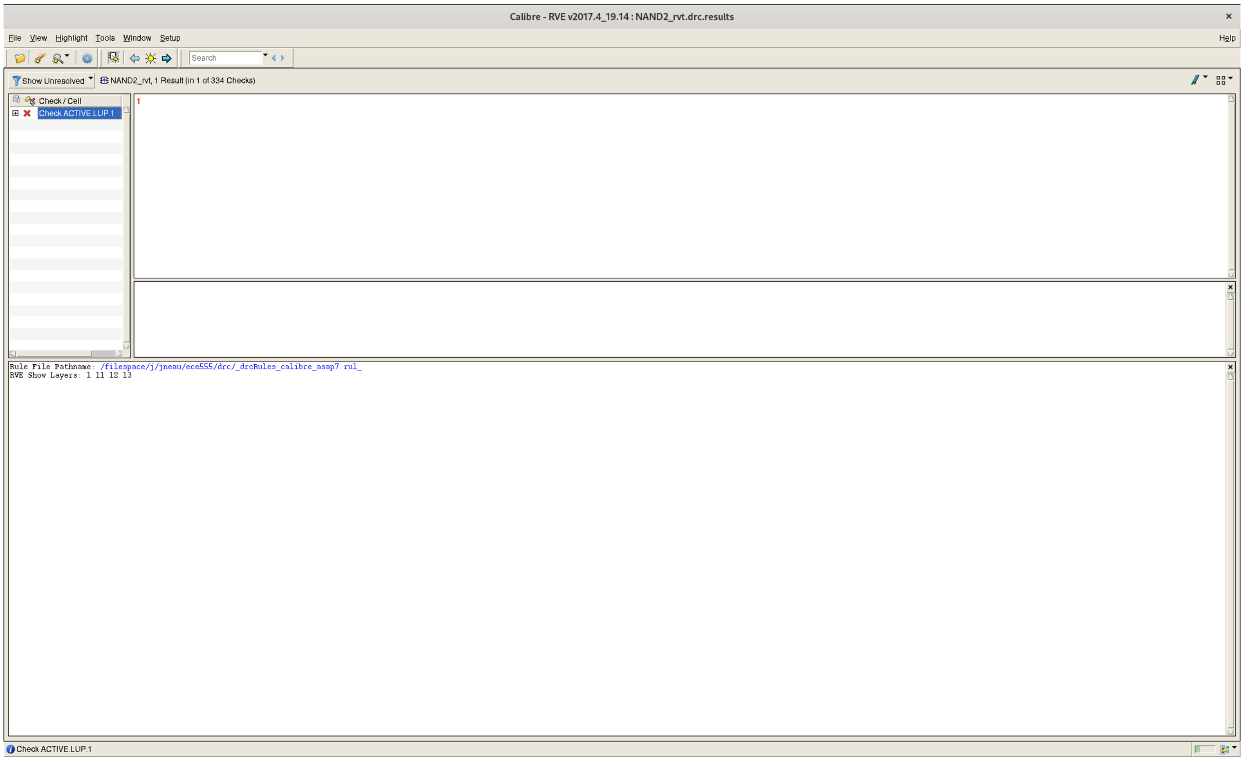
AND2_rvt, 2 Results (in 1 of 334 Checks)

Check ACTIVE.LUP.1

```
Rule File Pathname: /filespace/j/jneau/ece555/drc/_drcRules_calibre_asap7.rul_
RVE Show Layers: 1 11 12 13
```

Check ACTIVE.LUP.1

NAND Gate



Calibre - RVE v2017.4_19.14 : NAND2_rvt.drc.results

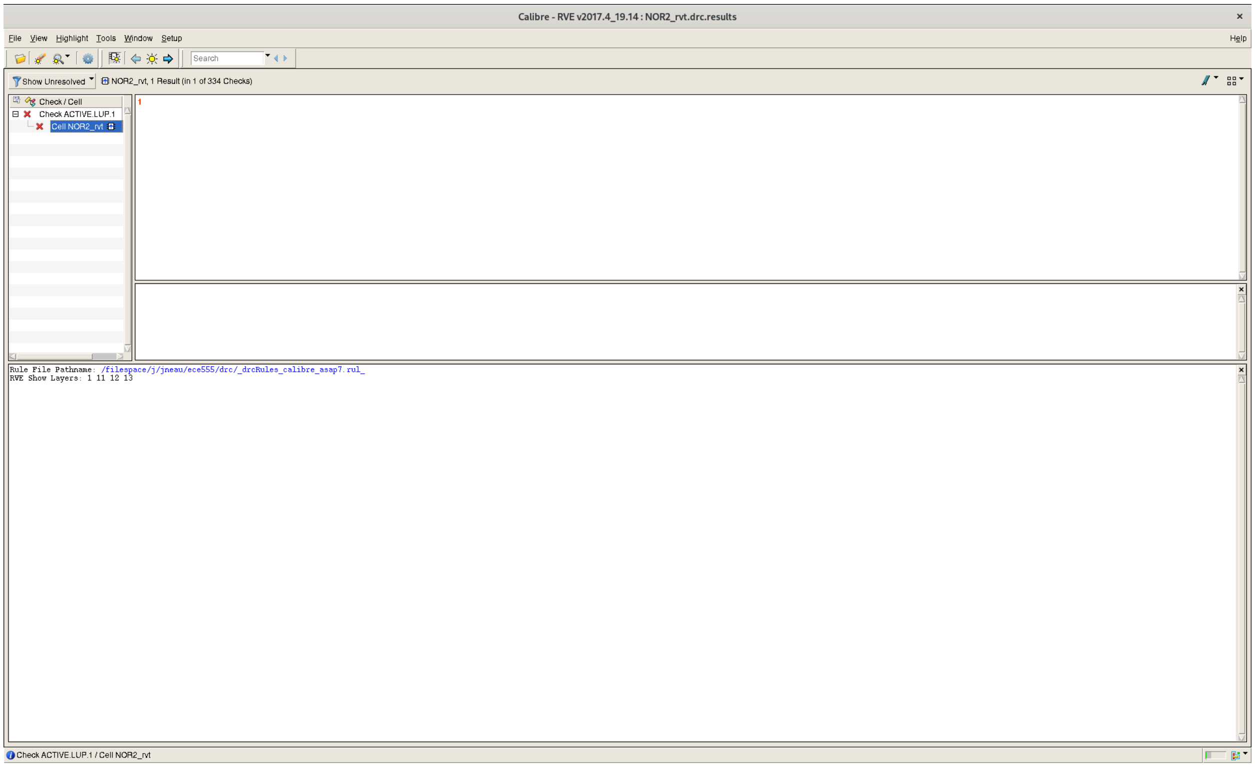
NAND2_rvt, 1 Result (in 1 of 334 Checks)

Check ACTIVE.LUP.1

```
Rule File Pathname: /filespace/j/jneau/ece555/drc/_drcRules_calibre_asap7.rul_
RVE Show Layers: 1 11 12 13
```

Check ACTIVE.LUP.1

NOR Gate



Calibre - RVE v2017.4_19.14 : NOR2_rvt.drc.results
File View Highlight Tools Window Setup
Help
Search
Show Unresolved
Check / Cell

NOR2_rvt, 1 Result (in 1 of 334 Checks)

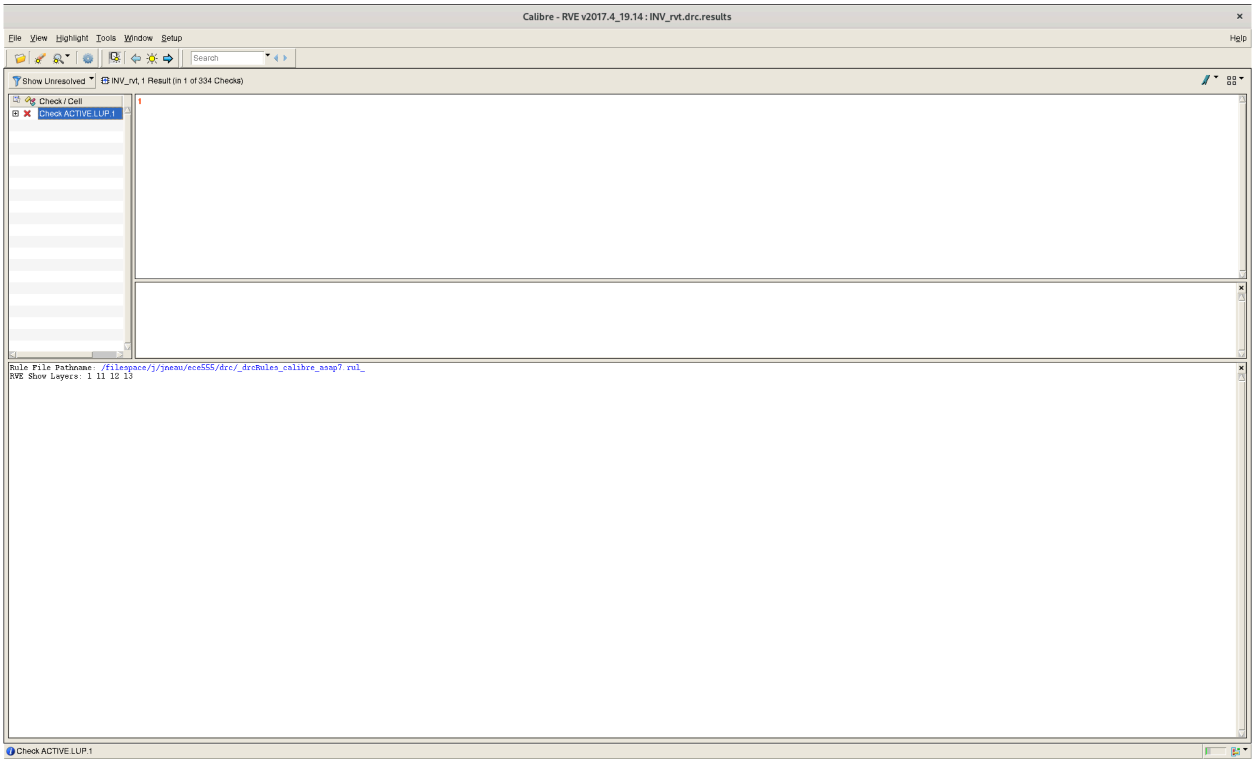
- ☒ Check ACTIVE.LUP.1
  - ☒ Cell NOR2_rvt

1

```
Rule File Pathname: /filespace/j/jneau/ece555/drc/_drcRules_calibre_asap7.rul_
RVE Show Layers: 1 11 12 13
```

Check ACTIVE.LUP.1 / Cell NOR2_rvt

Inverter



Calibre - RVE v2017.4_19.14 : INV_rvt.drc.results
File View Highlight Tools Window Setup
Help
Search
Show Unresolved
Check / Cell

INV_rvt, 1 Result (in 1 of 334 Checks)

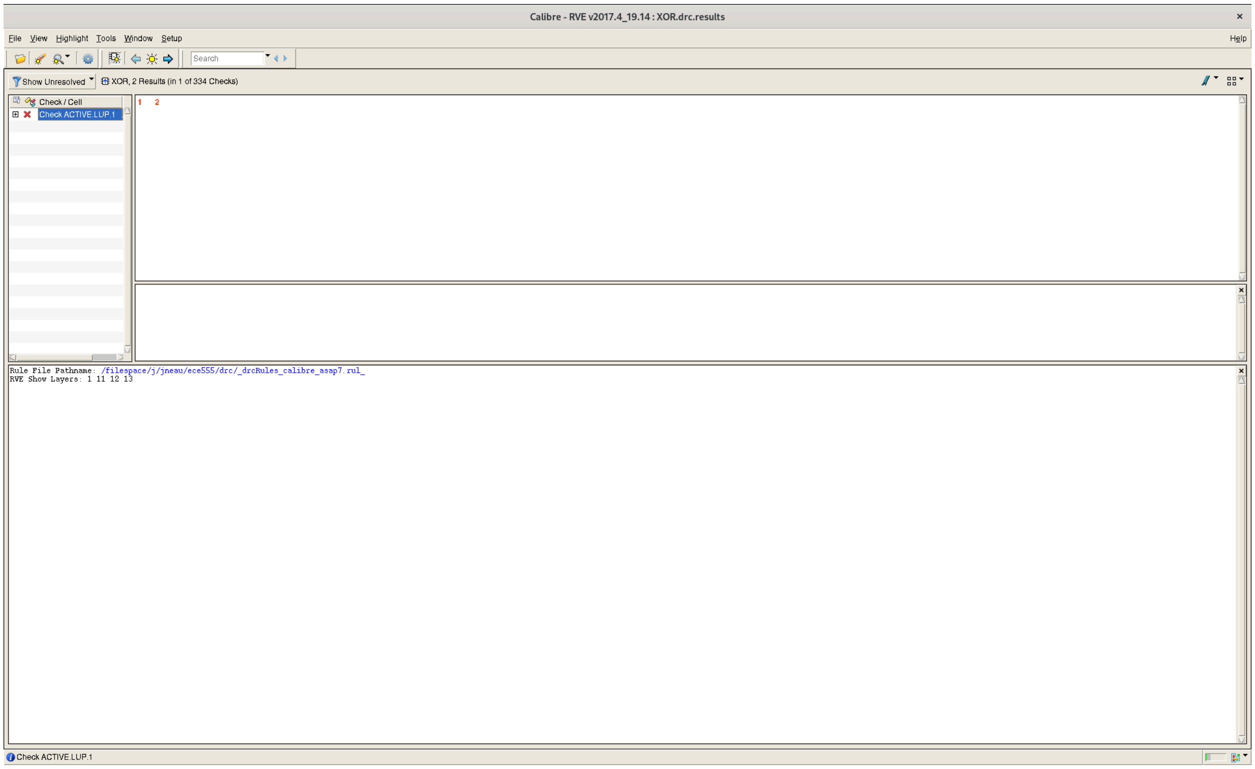
- ☒ Check ACTIVE.LUP.1

1

```
Rule File Pathname: /filespace/j/jneau/ece555/drc/_drcRules_calibre_asap7.rul_
RVE Show Layers: 1 11 12 13
```

Check ACTIVE.LUP.1

XOR Gate



Calibre - RVE v2017.4_19.14 : XOR.drc.results

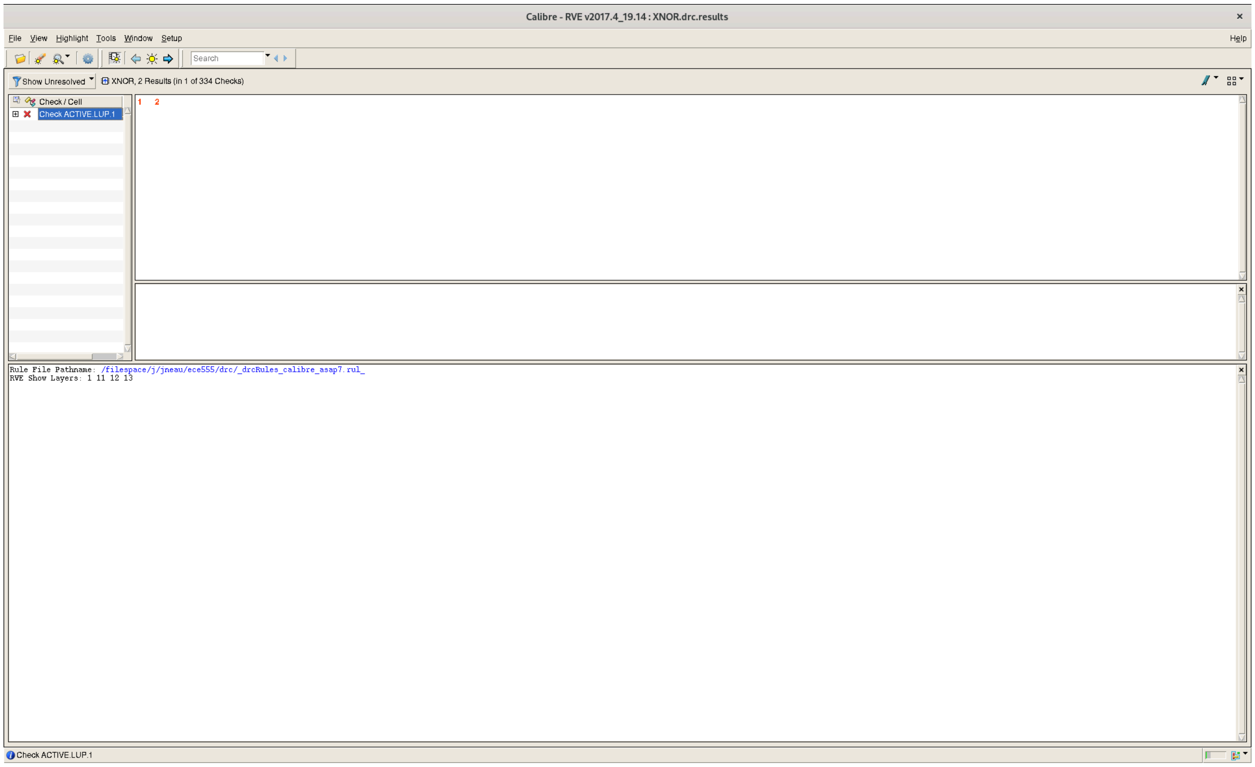
XOR, 2 Results (in 1 of 334 Checks)

Check ACTIVE.LUP.1

```
Rule File Pathname: /filespace/j/jneau/ece555/drc/_drcRules_calibre_asap7.rul_
RVE Show Layers: 1 11 12 13
```

Check ACTIVE.LUP.1

XNOR Gate



Calibre - RVE v2017.4_19.14 : XNOR.drc.results

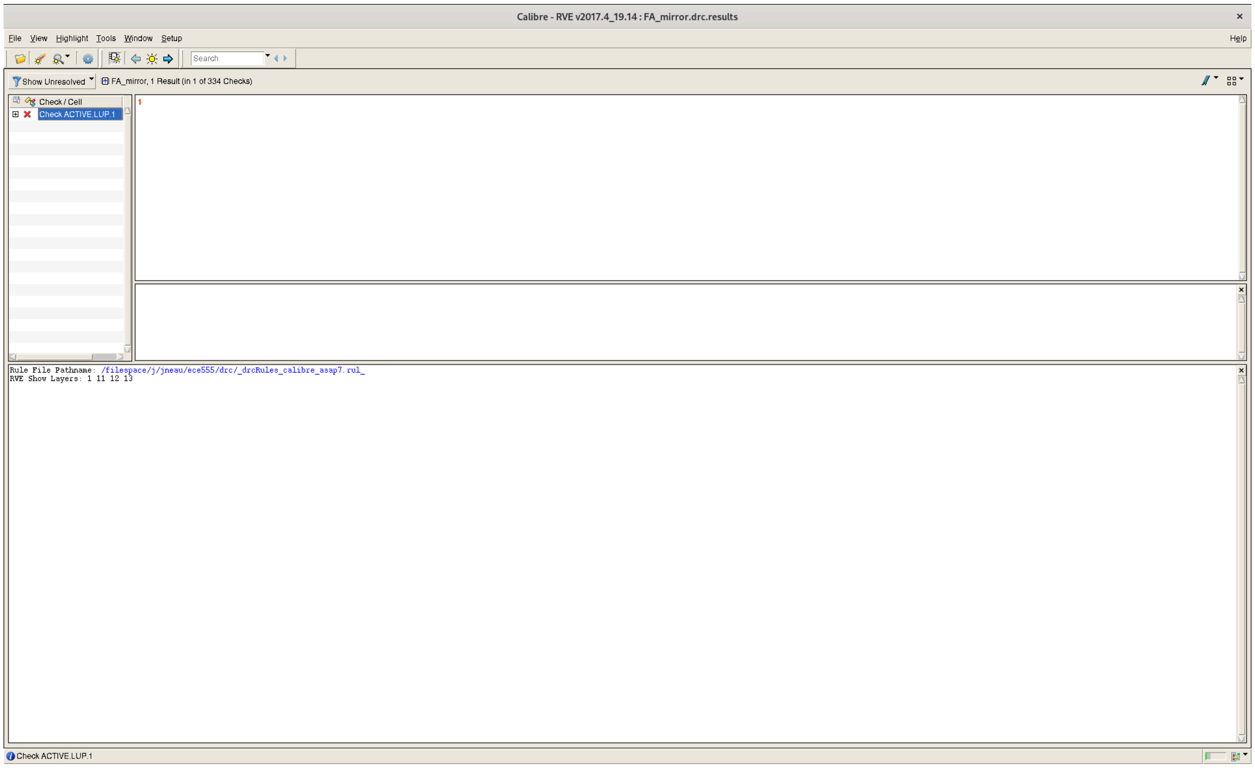
XNOR, 2 Results (in 1 of 334 Checks)

Check ACTIVE.LUP.1

```
Rule File Pathname: /filespace/j/jneau/ece555/drc/_drcRules_calibre_asap7.rul_
RVE Show Layers: 1 11 12 13
```

Check ACTIVE.LUP.1

Mirror Adder Cell



FA_mirror, 1 Result (in 1 of 334 Checks)

Check ACTIVE.LUP.1

1

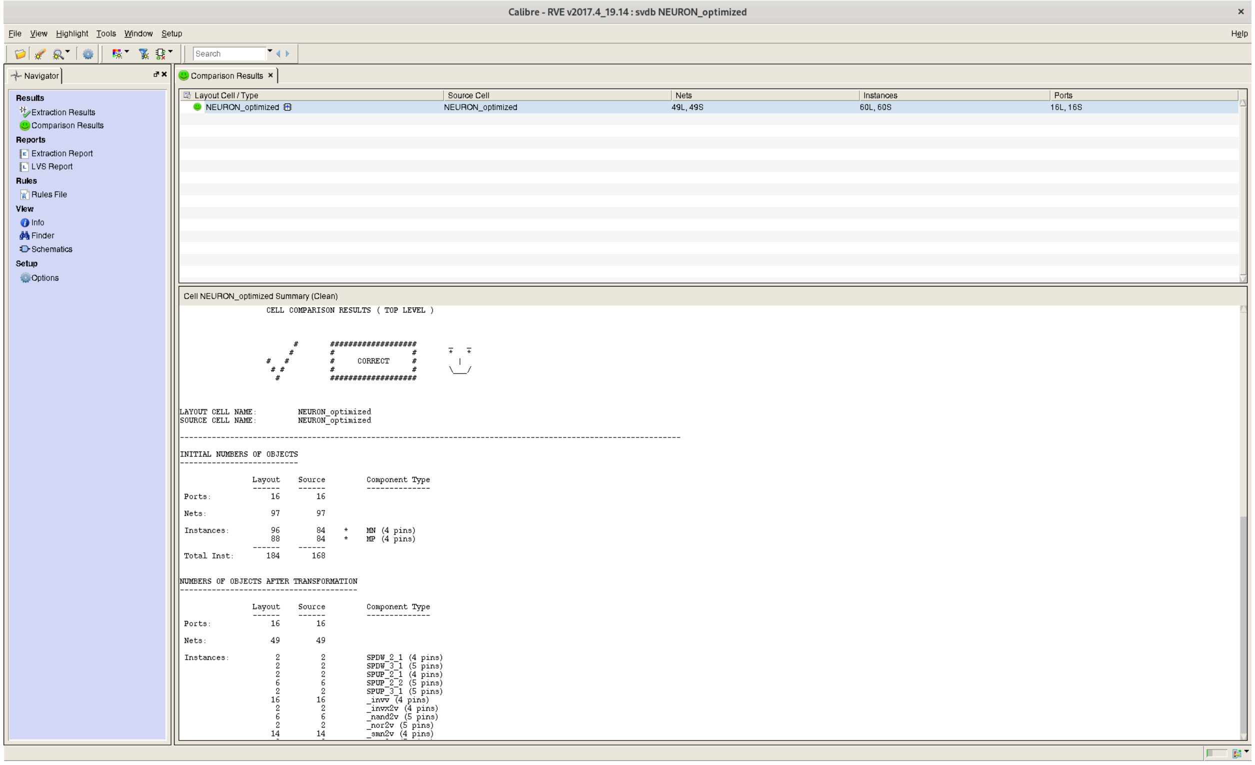
```
Rule File Pathname: /filespace/j/jneau/ece555/drc/_drcRules_calibre_asap7.rul_
RVE Show Layers: 1 11 12 13
```

Check ACTIVE.LUP.1

Appendix II: LVS Screenshots

Note: there are no screenshots to include for the non-gate submodules because the neuron layout was implemented with a flat design

Neuron

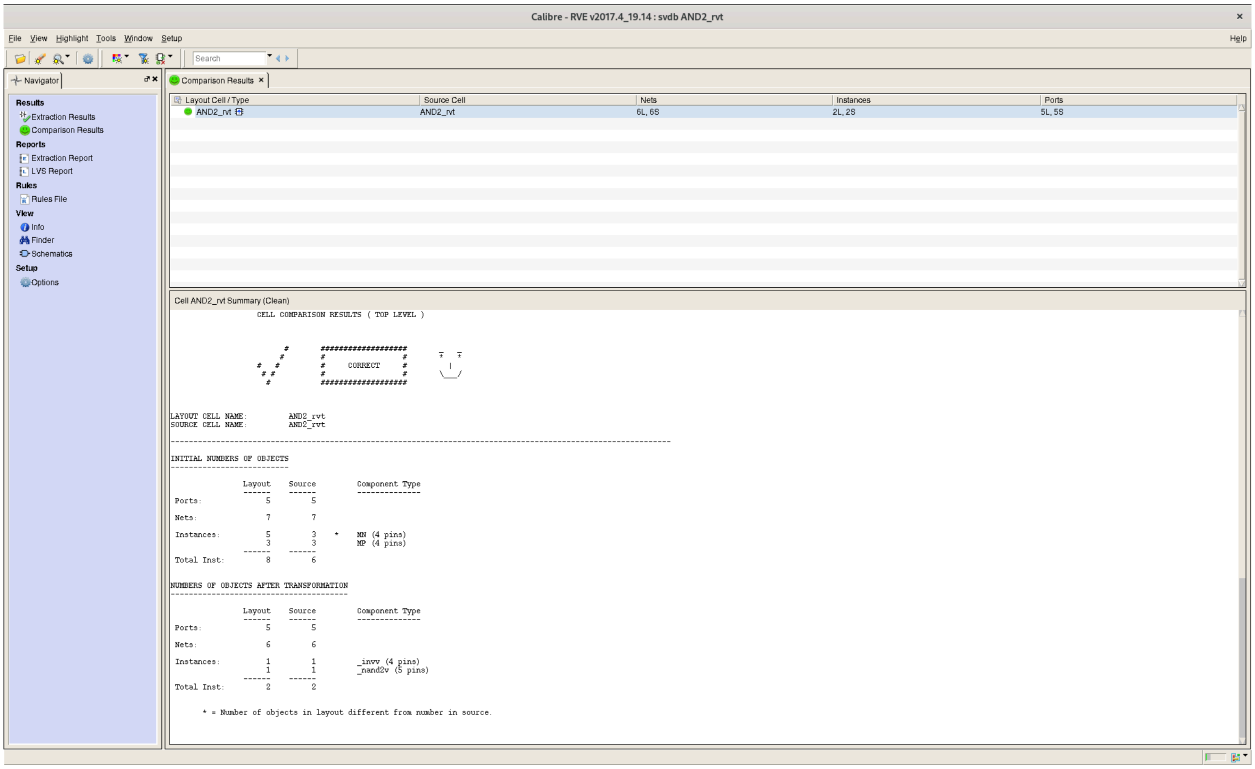


Layout Cell / Type	Source Cell	Nets	Instances	Ports
NEURON_optimized	NEURON_optimized	49L, 49S	60L, 60S	16L, 16S

Cell NEURON_optimized Summary (Clean)

```
                  CELL COMPARISON RESULTS ( TOP LEVEL )



                        #       ###################
                       #        #                 #      _   _
                  #   #         #     CORRECT     #      *   *
                   # #          #                 #        |
                    #           ###################      \___/


LAYOUT CELL NAME:         NEURON_optimized
SOURCE CELL NAME:         NEURON_optimized

--------------------------------------------------------------------------------------------------------------

INITIAL NUMBERS OF OBJECTS
--------------------------

                Layout    Source         Component Type
                ------    ------         --------------
 Ports:           16        16

 Nets:            97        97

 Instances:       96        84    *    MN (4 pins)
                  88        84    *    MP (4 pins)
                ------    ------
 Total Inst:     184       168


NUMBERS OF OBJECTS AFTER TRANSFORMATION
---------------------------------------

                Layout    Source         Component Type
                ------    ------         --------------
 Ports:           16        16

 Nets:            49        49

 Instances:        2         2           SPDW_2_1 (4 pins)
                   2         2           SPDW_3_1 (5 pins)
                   2         2           SPUP_2_1 (4 pins)
                   6         6           SPUP_2_2 (5 pins)
                   2         2           SPUP_3_1 (5 pins)
                  16        16           _invv (4 pins)
                   2         2           _invx2v (4 pins)
                   6         6           _nand2v (5 pins)
                   2         2           _nor2v (5 pins)
                  14        14           _smn2v (4 pins)
```

AND Gate

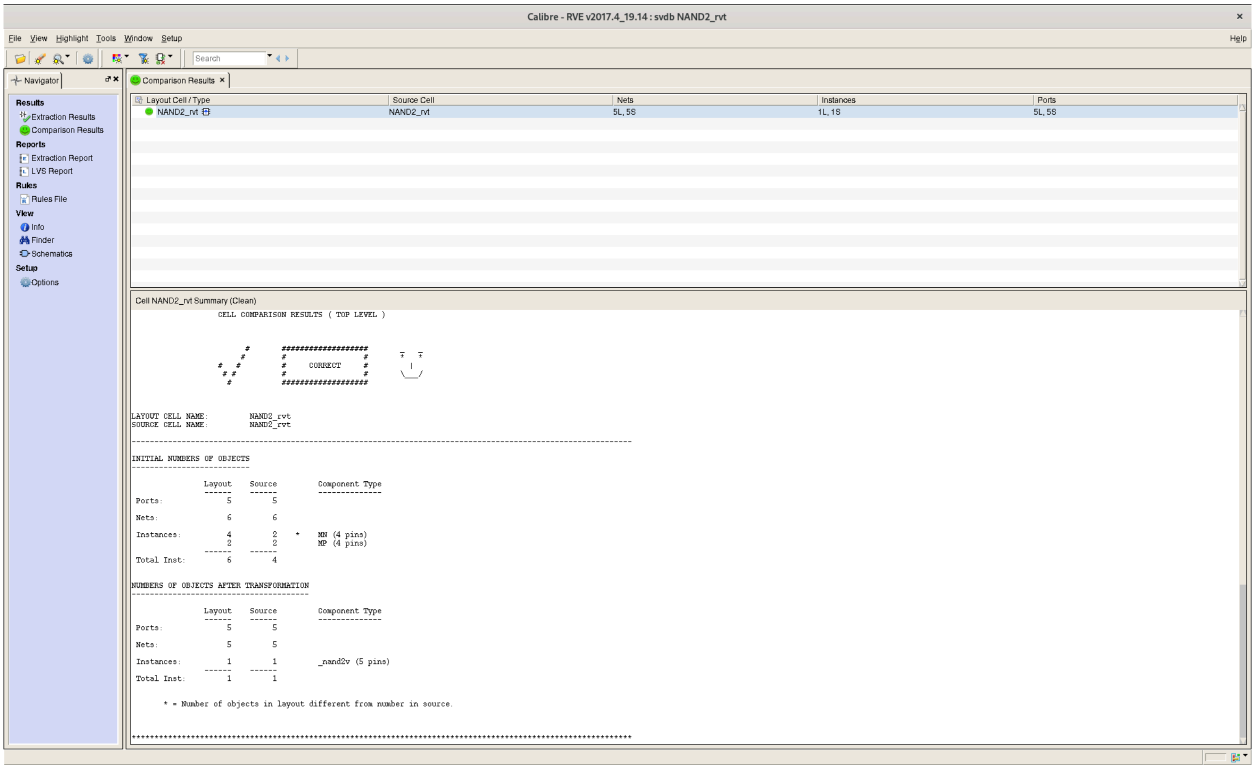


Layout Cell / Type	Source Cell	Nets	Instances	Ports
AND2_rvt	AND2_rvt	6L, 6S	2L, 2S	5L, 5S

Cell AND2_rvt Summary (Clean)

```
                    CELL COMPARISON RESULTS ( TOP LEVEL )


                       #       ###################
                      #        #                 #
                 #   #         #     CORRECT     #       _   _
                  # #          #                 #       *   *
                   #           ###################         |
                                                         \___/


LAYOUT CELL NAME:         AND2_rvt
SOURCE CELL NAME:         AND2_rvt

--------------------------------------------------------------------------------------------------------------

INITIAL NUMBERS OF OBJECTS
--------------------------

                Layout    Source         Component Type
                ------    ------         --------------
 Ports:              5         5

 Nets:               7         7

 Instances:          5         3    *    MN (4 pins)
                     3         3         MP (4 pins)
                ------    ------
 Total Inst:         8         6


NUMBERS OF OBJECTS AFTER TRANSFORMATION
---------------------------------------

                Layout    Source         Component Type
                ------    ------         --------------
 Ports:              5         5

 Nets:               6         6

 Instances:          1         1         _invv (4 pins)
                     1         1         _nand2v (5 pins)
                ------    ------
 Total Inst:         2         2


       * = Number of objects in layout different from number in source.
```

NAND Gate

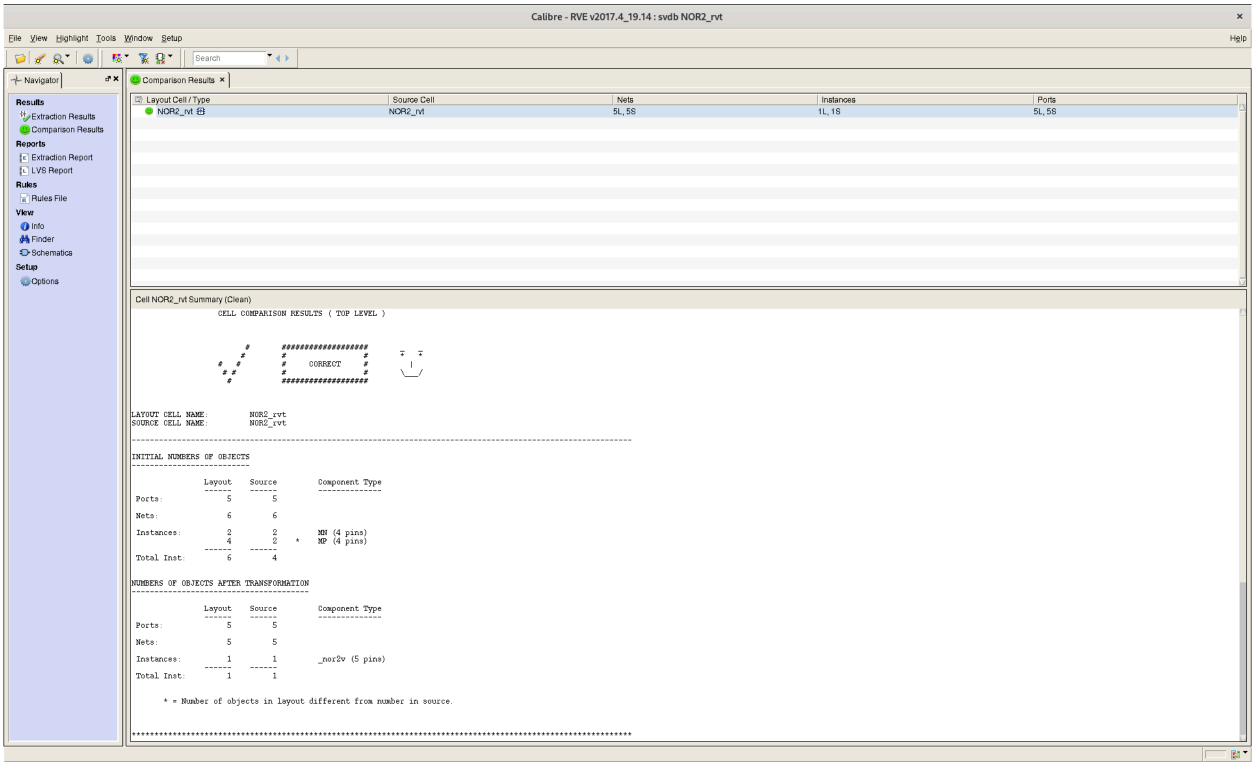


Layout Cell / Type	Source Cell	Nets	Instances	Ports
NAND2_rvt	NAND2_rvt	5L, 5S	1L, 1S	5L, 5S

Cell NAND2_rvt Summary (Clean)

```
                    CELL COMPARISON RESULTS ( TOP LEVEL )


                       #       ###################
                      #        #                 #
                 #   #         #     CORRECT     #       _   _
                  # #          #                 #       *   *
                   #           ###################         |
                                                         \___/


LAYOUT CELL NAME:         NAND2_rvt
SOURCE CELL NAME:         NAND2_rvt

--------------------------------------------------------------------------------------------------------------

INITIAL NUMBERS OF OBJECTS
--------------------------

                Layout    Source         Component Type
                ------    ------         --------------
 Ports:              5         5

 Nets:               6         6

 Instances:          4         2    *    MN (4 pins)
                     2         2         MP (4 pins)
                ------    ------
 Total Inst:         6         4


NUMBERS OF OBJECTS AFTER TRANSFORMATION
---------------------------------------

                Layout    Source         Component Type
                ------    ------         --------------
 Ports:              5         5

 Nets:               5         5

 Instances:          1         1         _nand2v (5 pins)
                ------    ------
 Total Inst:         1         1


       * = Number of objects in layout different from number in source.


**************************************************************************************************************
```

NOR Gate



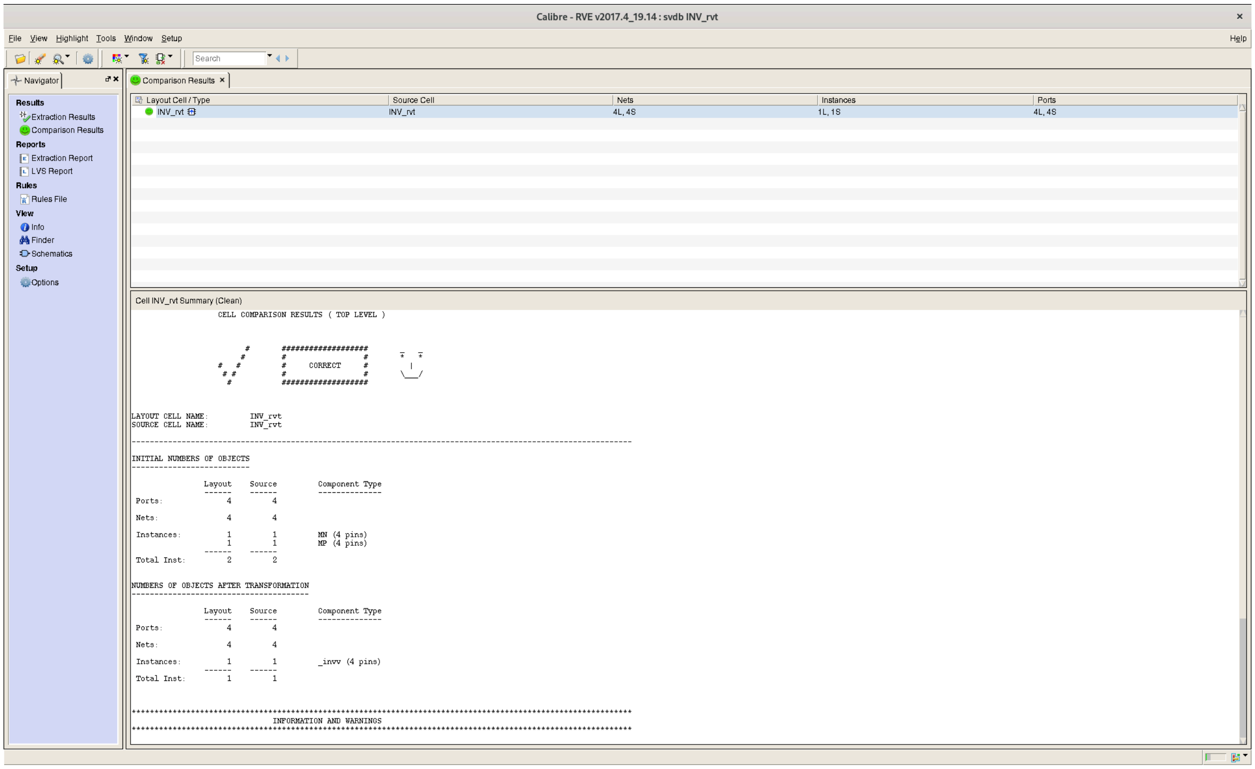
Calibre - RVE v2017.4_19.14 : svdb NOR2_rvt

Layout Cell / Type	Source Cell	Nets	Instances	Ports
● NOR2_rvt	NOR2_rvt	5L, 5S	1L, 1S	5L, 5S

Cell NOR2_rvt Summary (Clean)

```
                  CELL COMPARISON RESULTS ( TOP LEVEL )



                       #       ##################
                      #        #                #        _   _
                  #   #        #     CORRECT    #        *   *
                   # #         #                #          |
                    #          ##################        \___/


LAYOUT CELL NAME:         NOR2_rvt
SOURCE CELL NAME:         NOR2_rvt

--------------------------------------------------------------------------------------------------------------

INITIAL NUMBERS OF OBJECTS
--------------------------

                Layout    Source         Component Type
                ------    ------         --------------
 Ports:              5         5

 Nets:               6         6

 Instances:          2         2         MN (4 pins)
                     4         2    *    MP (4 pins)
                ------    ------
 Total Inst:         6         4


NUMBERS OF OBJECTS AFTER TRANSFORMATION
---------------------------------------

                Layout    Source         Component Type
                ------    ------         --------------
 Ports:              5         5

 Nets:               5         5

 Instances:          1         1         _nor2v (5 pins)
                ------    ------
 Total Inst:         1         1


       * = Number of objects in layout different from number in source.



**************************************************************************************************************
```

Inverter



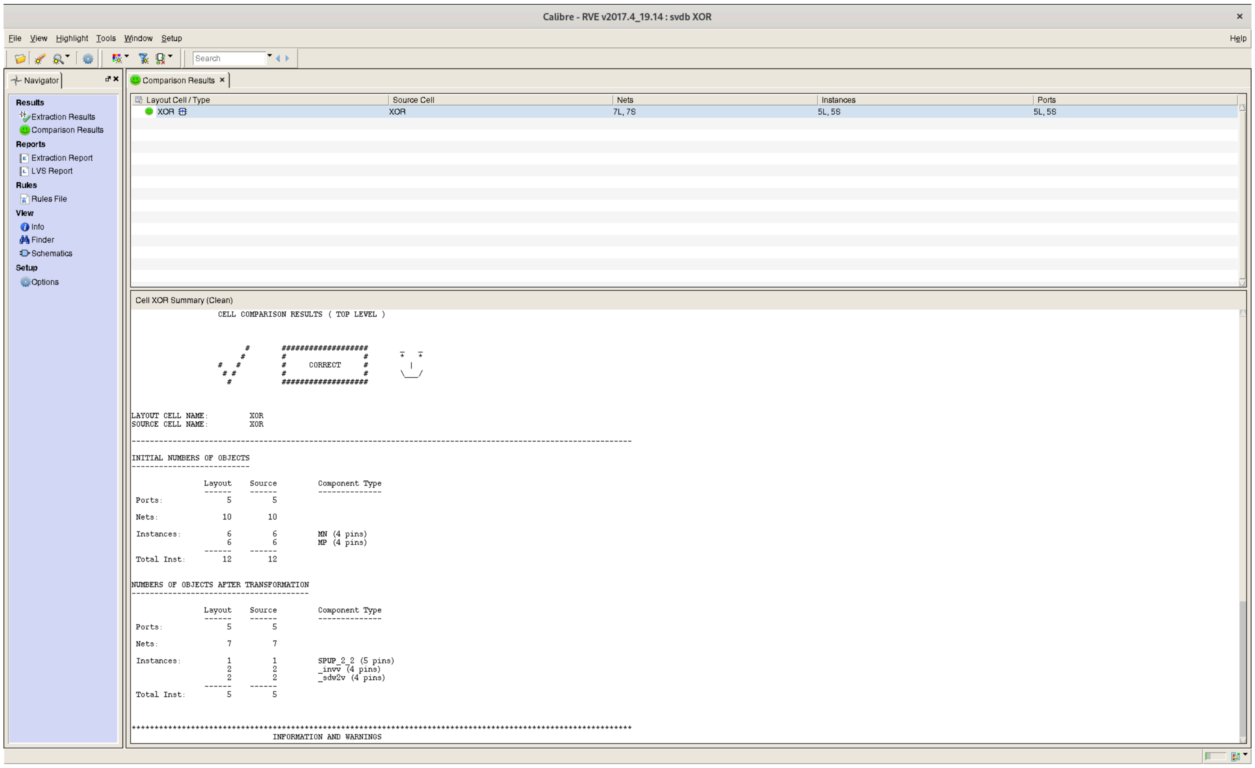
Calibre - RVE v2017.4_19.14 : svdb INV_rvt

Layout Cell / Type	Source Cell	Nets	Instances	Ports
● INV_rvt	INV_rvt	4L, 4S	1L, 1S	4L, 4S

Cell INV_rvt Summary (Clean)

```
                  CELL COMPARISON RESULTS ( TOP LEVEL )



                       #       ##################
                      #        #                #        _   _
                  #   #        #     CORRECT    #        *   *
                   # #         #                #          |
                    #          ##################        \___/


LAYOUT CELL NAME:         INV_rvt
SOURCE CELL NAME:         INV_rvt

--------------------------------------------------------------------------------------------------------------

INITIAL NUMBERS OF OBJECTS
--------------------------

                Layout    Source         Component Type
                ------    ------         --------------
 Ports:              4         4

 Nets:               4         4

 Instances:          1         1         MN (4 pins)
                     1         1         MP (4 pins)
                ------    ------
 Total Inst:         2         2


NUMBERS OF OBJECTS AFTER TRANSFORMATION
---------------------------------------

                Layout    Source         Component Type
                ------    ------         --------------
 Ports:              4         4

 Nets:               4         4

 Instances:          1         1         _invv (4 pins)
                ------    ------
 Total Inst:         1         1



**************************************************************************************************************
                               INFORMATION AND WARNINGS
**************************************************************************************************************
```

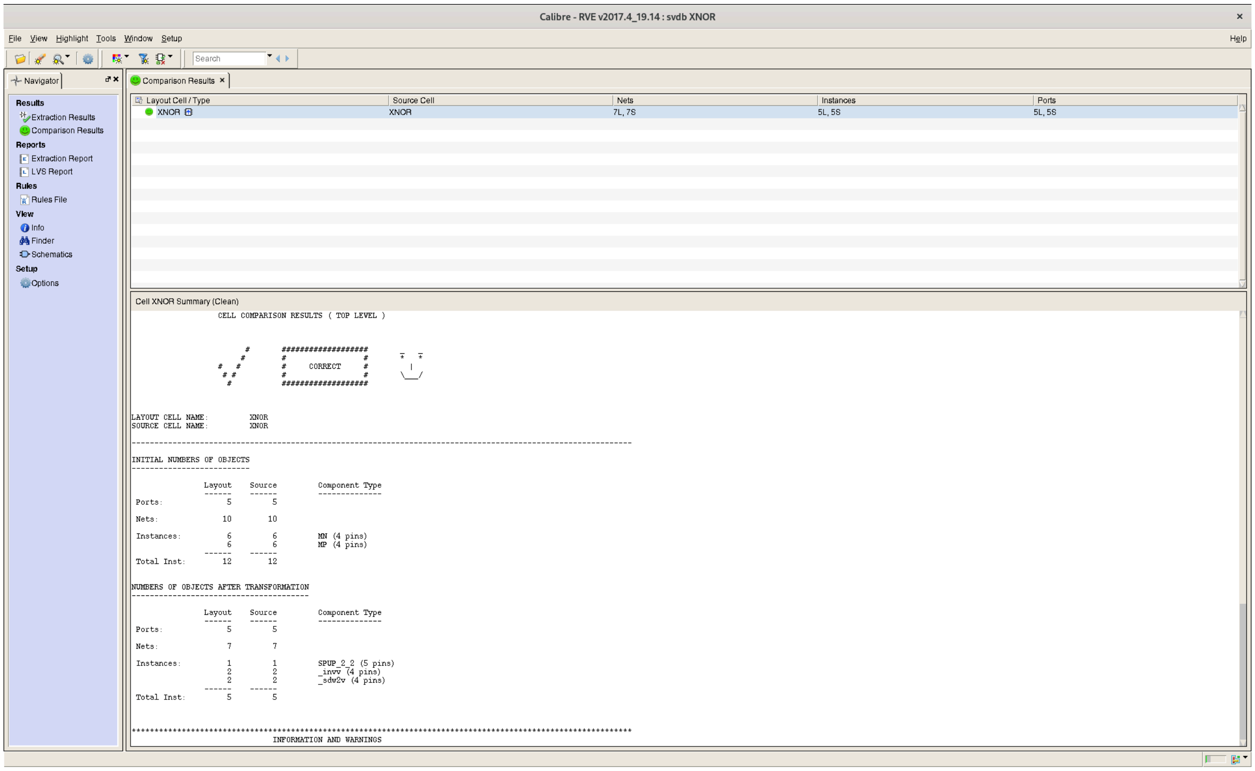
XOR Gate



Layout Cell / Type	Source Cell	Nets	Instances	Ports
XOR	XOR	7L, 7S	5L, 5S	5L, 5S

```
                  CELL COMPARISON RESULTS ( TOP LEVEL )



                        #        ##################
                       #         #                #        _   _
                   #   #         #     CORRECT    #          |
                    # #          #                #        \___/
                     #           ##################


LAYOUT CELL NAME:          XOR
SOURCE CELL NAME:          XOR

--------------------------------------------------------------------------------------------------------------

INITIAL NUMBERS OF OBJECTS
--------------------------

                 Layout    Source         Component Type
                 ------    ------         --------------
 Ports:              5         5

 Nets:              10        10

 Instances:          6         6          MN (4 pins)
                     6         6          MP (4 pins)
                 ------    ------
 Total Inst:        12        12


NUMBERS OF OBJECTS AFTER TRANSFORMATION
---------------------------------------

                 Layout    Source         Component Type
                 ------    ------         --------------
 Ports:              5         5

 Nets:               7         7

 Instances:          1         1          SPUP_2_2 (5 pins)
                     2         2          _invv (4 pins)
                     2         2          _sdw2v (4 pins)
                 ------    ------
 Total Inst:         5         5


**************************************************************************************************************
                               INFORMATION AND WARNINGS
```

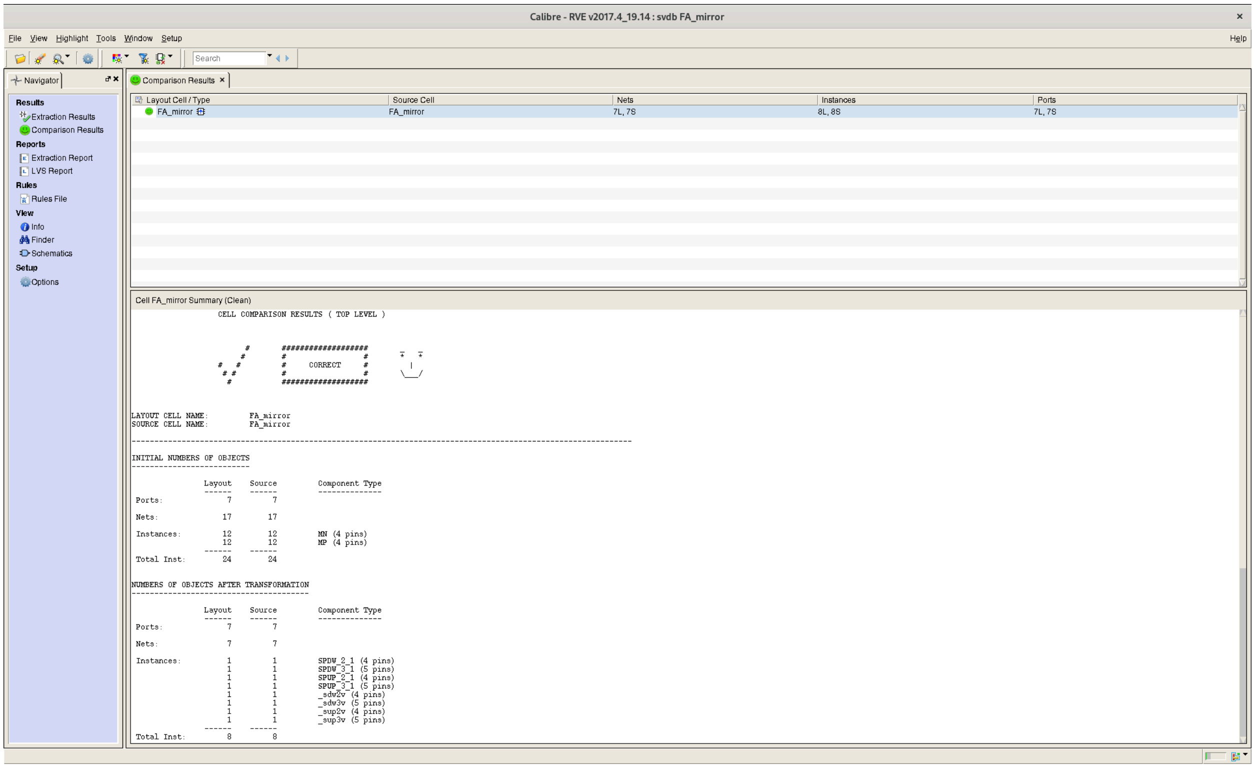
XNOR Gate



Layout Cell / Type	Source Cell	Nets	Instances	Ports
XNOR	XNOR	7L, 7S	5L, 5S	5L, 5S

```
                  CELL COMPARISON RESULTS ( TOP LEVEL )



                        #        ##################
                       #         #                #        _   _
                   #   #         #     CORRECT    #          |
                    # #          #                #        \___/
                     #           ##################


LAYOUT CELL NAME:          XNOR
SOURCE CELL NAME:          XNOR

--------------------------------------------------------------------------------------------------------------

INITIAL NUMBERS OF OBJECTS
--------------------------

                 Layout    Source         Component Type
                 ------    ------         --------------
 Ports:              5         5

 Nets:              10        10

 Instances:          6         6          MN (4 pins)
                     6         6          MP (4 pins)
                 ------    ------
 Total Inst:        12        12


NUMBERS OF OBJECTS AFTER TRANSFORMATION
---------------------------------------

                 Layout    Source         Component Type
                 ------    ------         --------------
 Ports:              5         5

 Nets:               7         7

 Instances:          1         1          SPUP_2_2 (5 pins)
                     2         2          _invv (4 pins)
                     2         2          _sdw2v (4 pins)
                 ------    ------
 Total Inst:         5         5


**************************************************************************************************************
                               INFORMATION AND WARNINGS
```

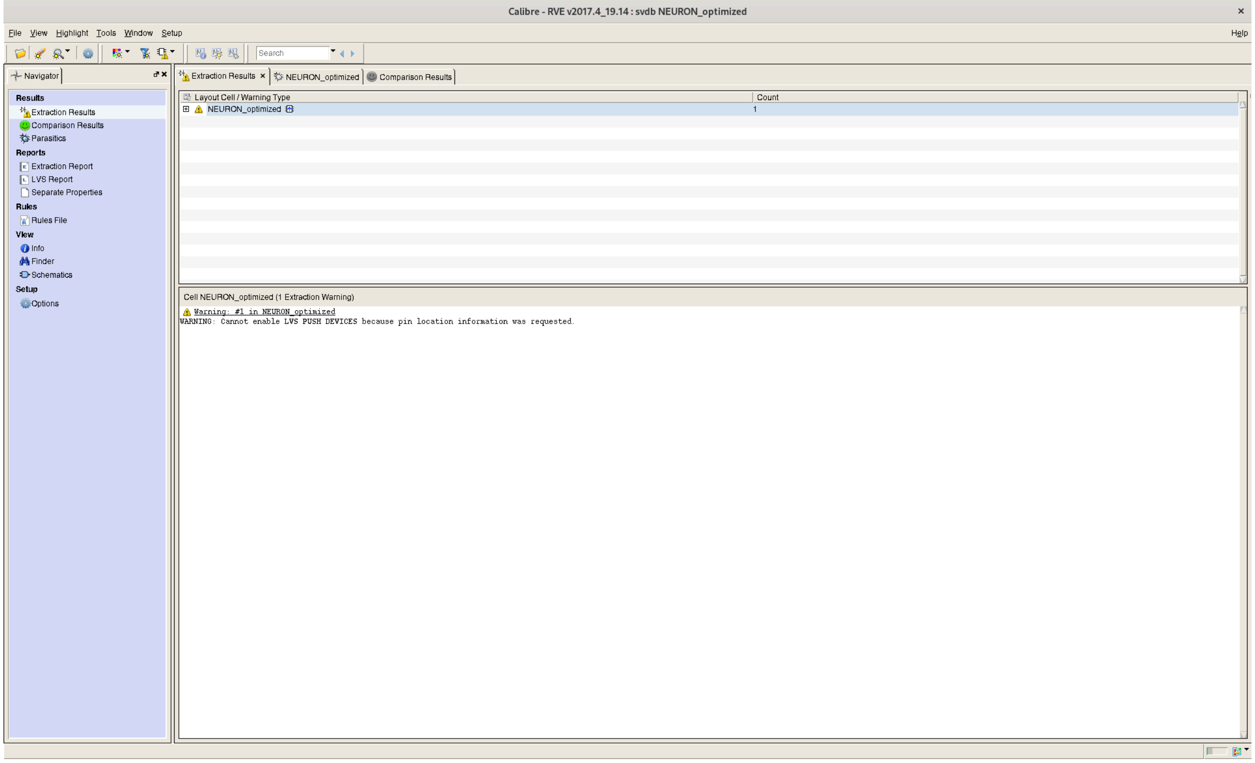
Mirror Adder Cell



Layout Cell / Type	Source Cell	Nets	Instances	Ports
● FA_mirror	FA_mirror	7L, 7S	8L, 8S	7L, 7S

```
                  CELL COMPARISON RESULTS ( TOP LEVEL )



                        #        ##################
                       #         #                #      _   _
                   #   #         #     CORRECT    #      *   *
                    # #          #                #        |
                     #           ##################      \___/



LAYOUT CELL NAME:         FA_mirror
SOURCE CELL NAME:         FA_mirror

--------------------------------------------------------------------------------------------------------------

INITIAL NUMBERS OF OBJECTS
--------------------------

                Layout    Source         Component Type
                ------    ------         --------------
 Ports:              7         7

 Nets:              17        17

 Instances:         12        12         MN (4 pins)
                    12        12         MP (4 pins)
                ------    ------
 Total Inst:        24        24


NUMBERS OF OBJECTS AFTER TRANSFORMATION
---------------------------------------

                Layout    Source         Component Type
                ------    ------         --------------
 Ports:              7         7

 Nets:               7         7

 Instances:          1         1         SPDW_2_1 (4 pins)
                     1         1         SPDW_3_1 (5 pins)
                     1         1         SPUP_2_1 (4 pins)
                     1         1         SPUP_3_1 (5 pins)
                     1         1         _sdw2v (4 pins)
                     1         1         _sdw3v (5 pins)
                     1         1         _sup2v (4 pins)
                     1         1         _sup3v (5 pins)
                ------    ------
 Total Inst:         8         8
```

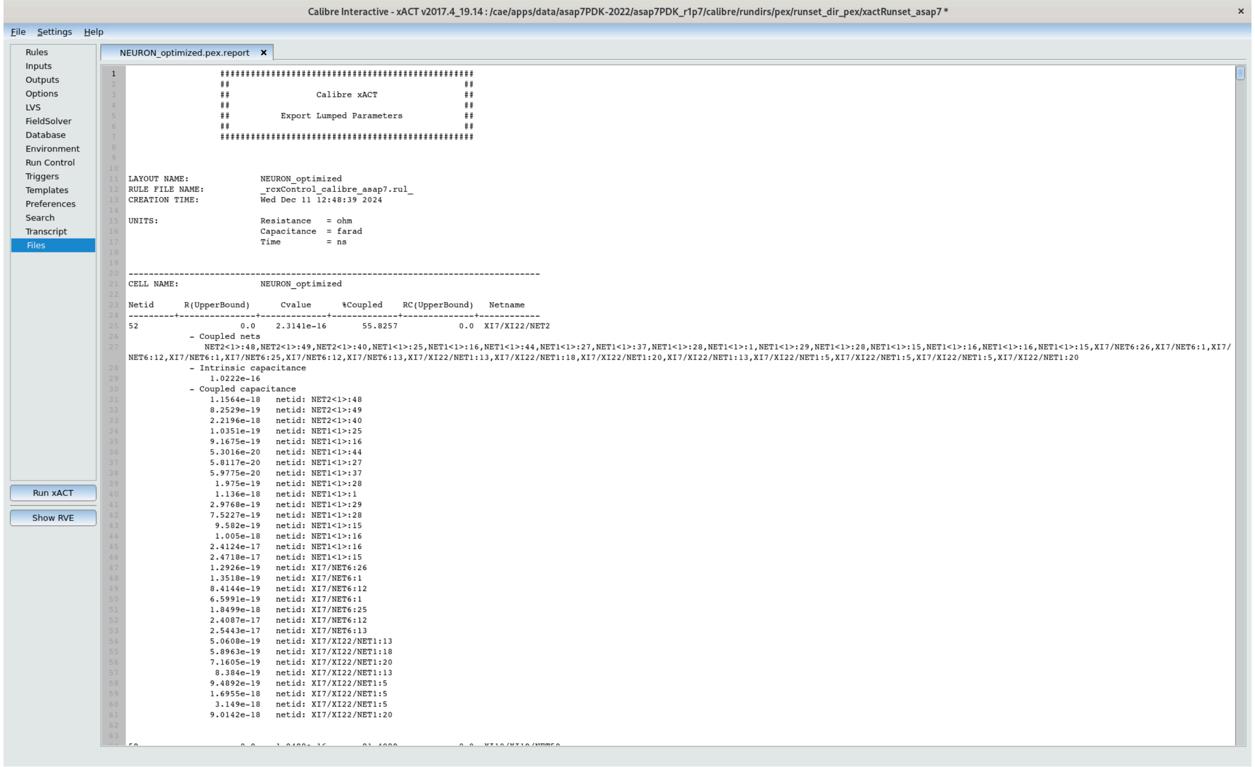
Neuron Calibre Extraction Screenshots



Layout Cell / Warning Type	Count
⊞ ⚠ NEURON_optimized	1

Cell NEURON_optimized (1 Extraction Warning)

```
⚠ Warning: #1 in NEURON_optimized
WARNING: Cannot enable LVS PUSH DEVICES because pin location information was requested.
```

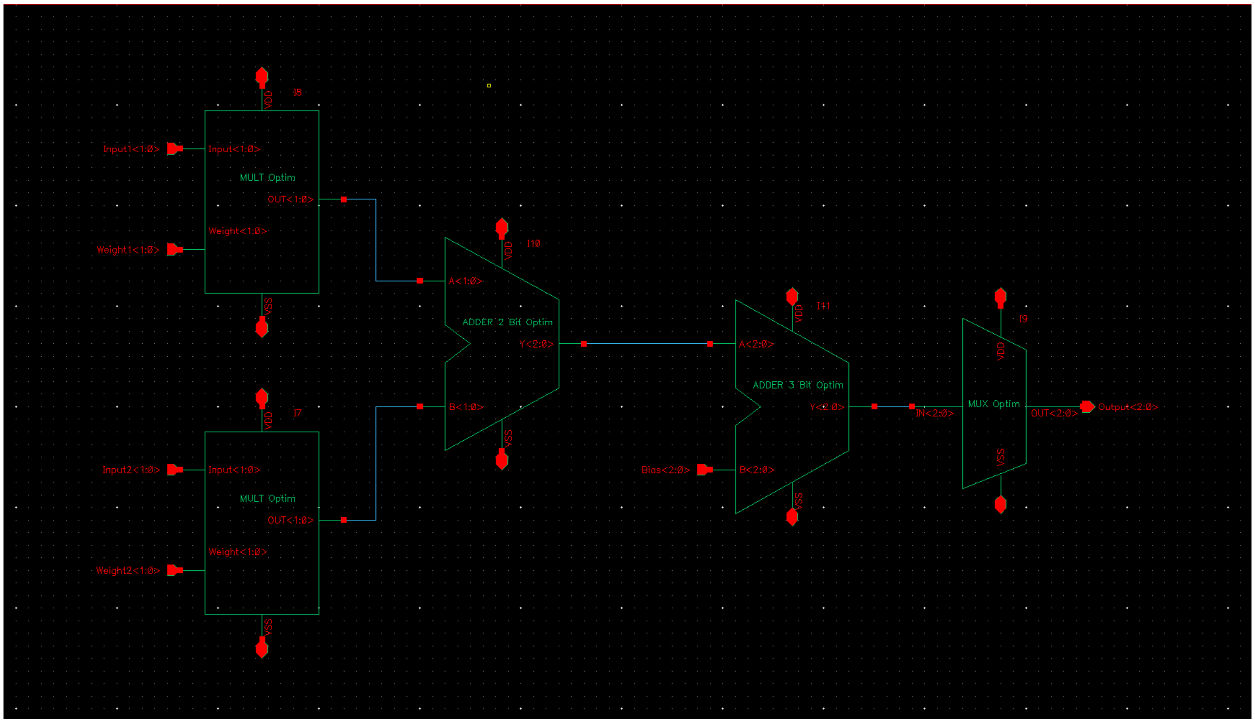


Calibre Interactive - xACT v2017.4_19.14 : /cae/apps/data/asap7PDK-2022/asap7PDK_r1p7/calibre/rundirs/pex/runset_dir_pex/xactRunset_asap7 *
File Settings Help
Rules
Inputs
Outputs
Options
LVS
FieldSolver
Database
Environment
Run Control
Triggers
Templates
Preferences
Search
Transcript
Files
Run xACT
Show RVE
NEURON_optimized.pex.report

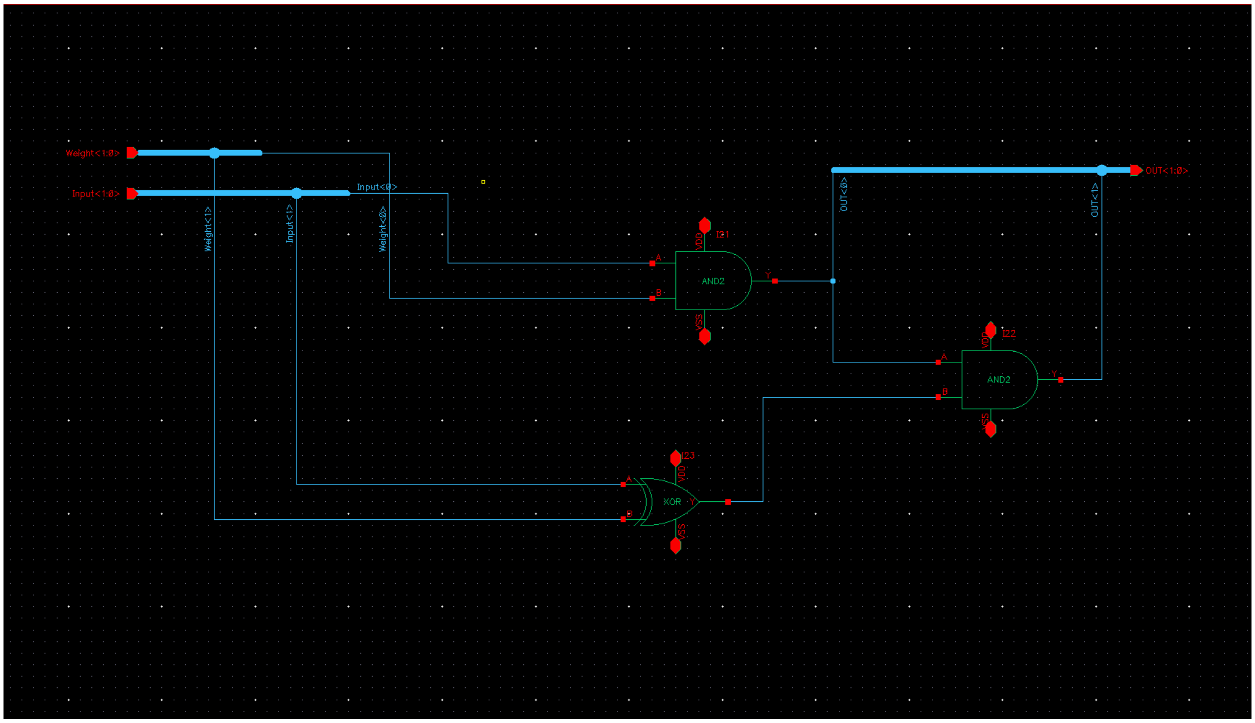
```
                  ##################################################
                  ##                                              ##
                  ##                 Calibre xACT                 ##
                  ##                                              ##
                  ##          Export Lumped Parameters            ##
                  ##                                              ##
                  ##################################################



LAYOUT NAME:               NEURON_optimized
RULE FILE NAME:            _rcxControl_calibre_asap7.rul_
CREATION TIME:             Wed Dec 11 12:48:39 2024

UNITS:                     Resistance   = ohm
                           Capacitance  = farad
                           Time         = ns


--------------------------------------------------------------------------------
CELL NAME:                 NEURON_optimized

Netid      R(UpperBound)      Cvalue      %Coupled    RC(UpperBound)   Netname
---------+---------------+-------------+-------------+--------------+------------
52                    0.0    2.3141e-16       55.8257            0.0  XI7/XI22/NET2
            - Coupled nets
               NET2<1>:48,NET2<1>:49,NET2<1>:40,NET1<1>:25,NET1<1>:16,NET1<1>:44,NET1<1>:27,NET1<1>:37,NET1<1>:28,NET1<1>:1,NET1<1>:29,NET1<1>:28,NET1<1>:15,NET1<1>:16,NET1<1>:16,NET1<1>:15,XI7/NET6:26,XI7/NET6:1,XI7/
NET6:12,XI7/NET6:1,XI7/NET6:25,XI7/NET6:12,XI7/NET6:13,XI7/XI22/NET1:13,XI7/XI22/NET1:18,XI7/XI22/NET1:20,XI7/XI22/NET1:13,XI7/XI22/NET1:5,XI7/XI22/NET1:5,XI7/XI22/NET1:5,XI7/XI22/NET1:20
            - Intrinsic capacitance
                1.0222e-16
            - Coupled capacitance
                1.1564e-18   netid: NET2<1>:48
                8.2529e-19   netid: NET2<1>:49
                2.2196e-18   netid: NET2<1>:40
                1.0351e-19   netid: NET1<1>:25
                9.1675e-19   netid: NET1<1>:16
                5.3016e-20   netid: NET1<1>:44
                5.8117e-20   netid: NET1<1>:27
                5.9775e-20   netid: NET1<1>:37
                 1.975e-19   netid: NET1<1>:28
                 1.136e-18   netid: NET1<1>:1
                2.9768e-19   netid: NET1<1>:29
                7.5227e-19   netid: NET1<1>:28
                 9.582e-19   netid: NET1<1>:15
                 1.005e-18   netid: NET1<1>:16
                2.4124e-17   netid: NET1<1>:16
                2.4718e-17   netid: NET1<1>:15
                1.2926e-19   netid: XI7/NET6:26
                1.3518e-19   netid: XI7/NET6:1
                8.4144e-19   netid: XI7/NET6:12
                6.5991e-19   netid: XI7/NET6:1
                1.8499e-18   netid: XI7/NET6:25
                2.4087e-17   netid: XI7/NET6:12
                2.5443e-17   netid: XI7/NET6:13
                5.0608e-19   netid: XI7/XI22/NET1:13
                5.8963e-19   netid: XI7/XI22/NET1:18
                7.1605e-19   netid: XI7/XI22/NET1:20
                 8.384e-19   netid: XI7/XI22/NET1:13
                9.4892e-19   netid: XI7/XI22/NET1:5
                1.6955e-18   netid: XI7/XI22/NET1:5
                 3.149e-18   netid: XI7/XI22/NET1:5
                9.0142e-18   netid: XI7/XI22/NET1:20
```

Appendix III: Schematics

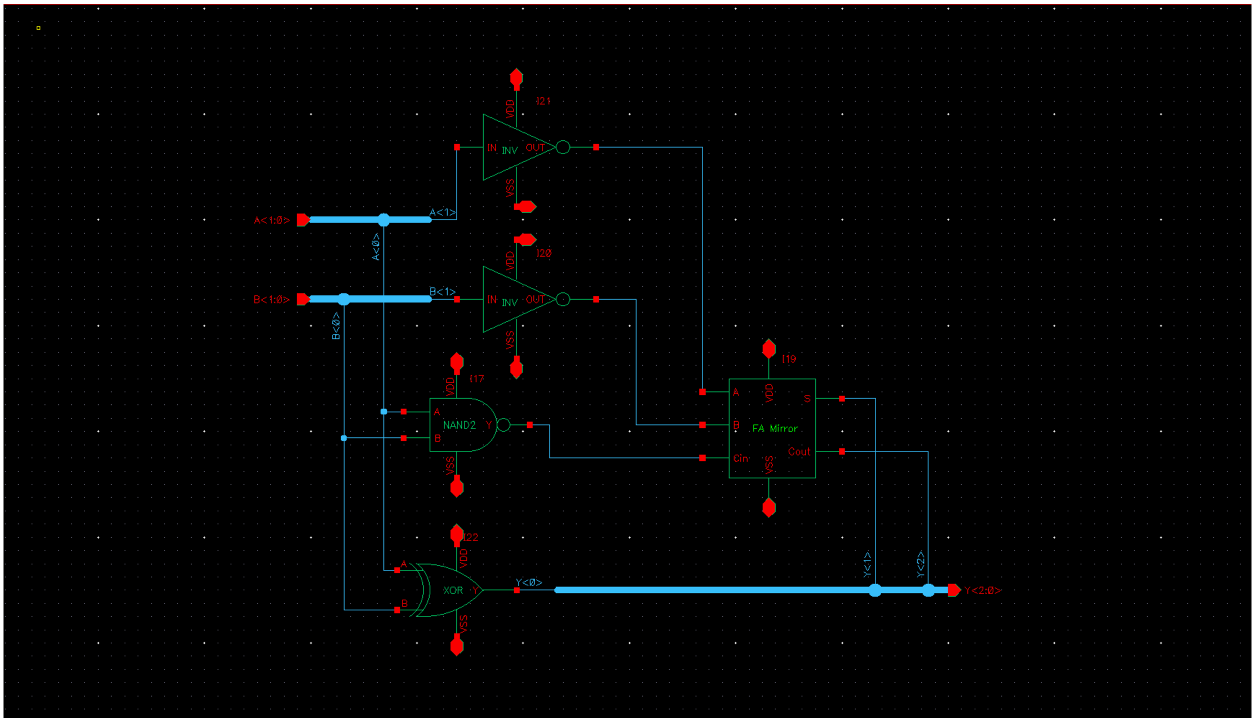
Neuron



Multiplier

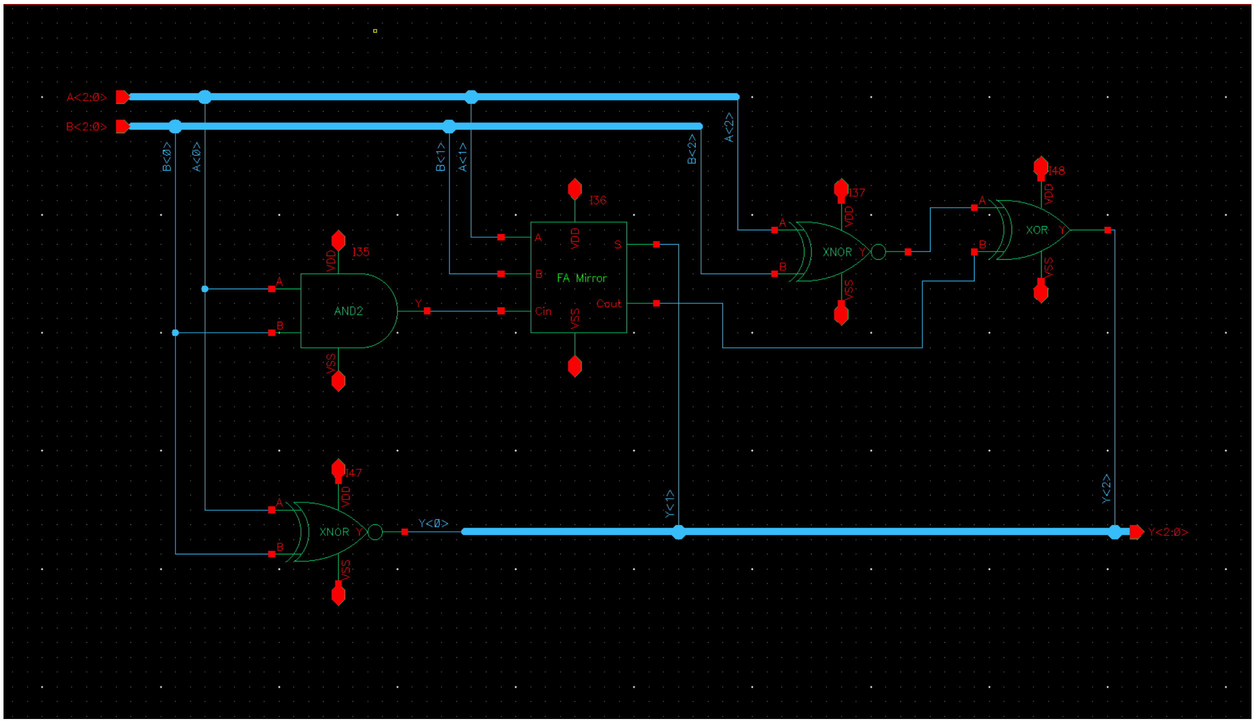


2-Bit Adder



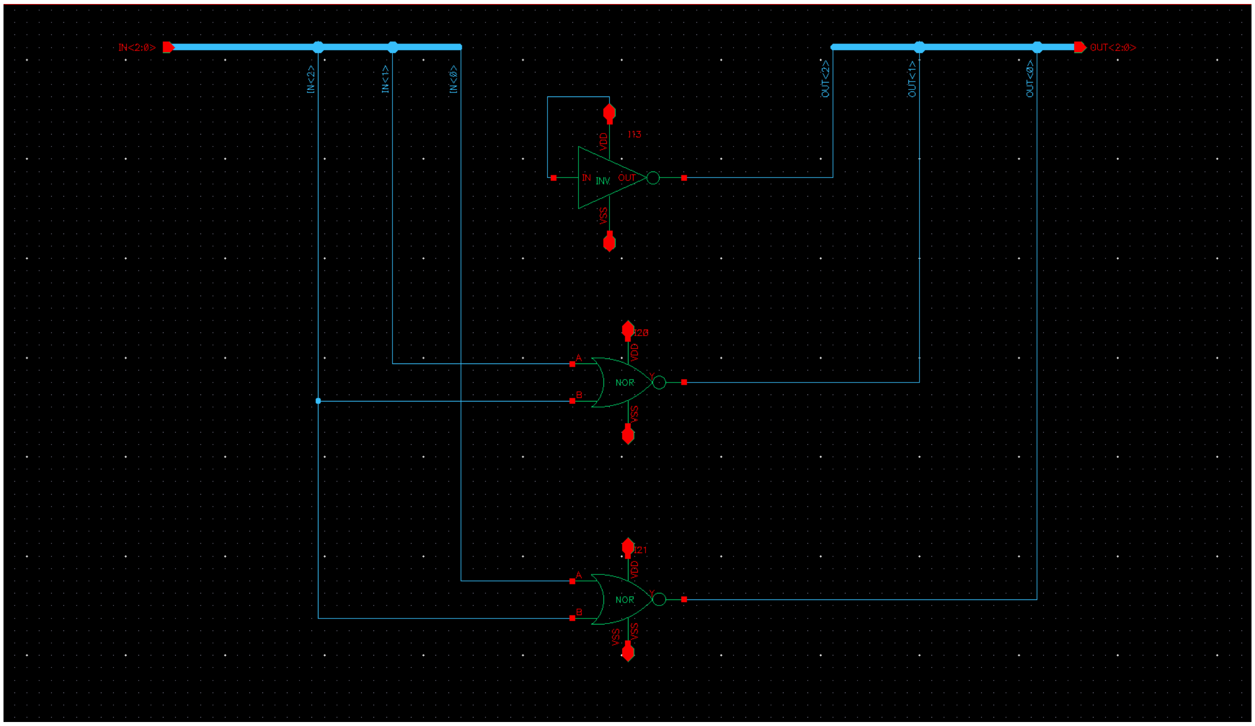
3-Bit Adder

Note: The output of this stage is the inverse of the sum

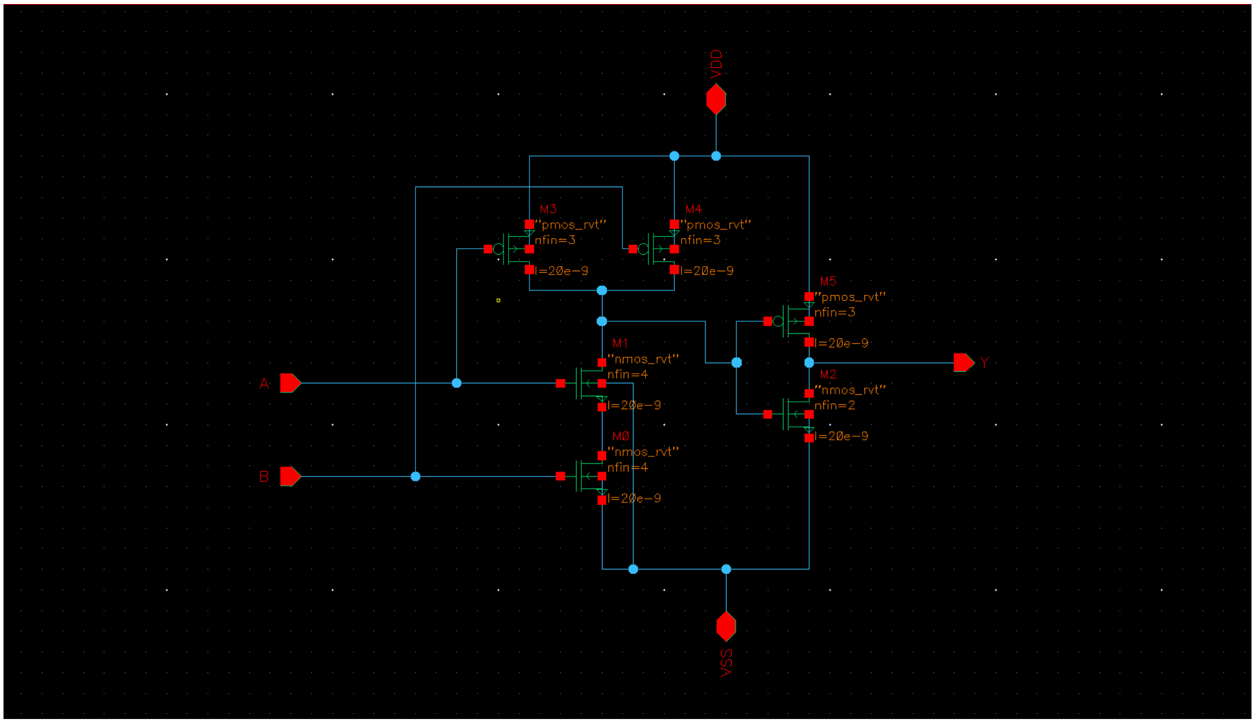


MUX

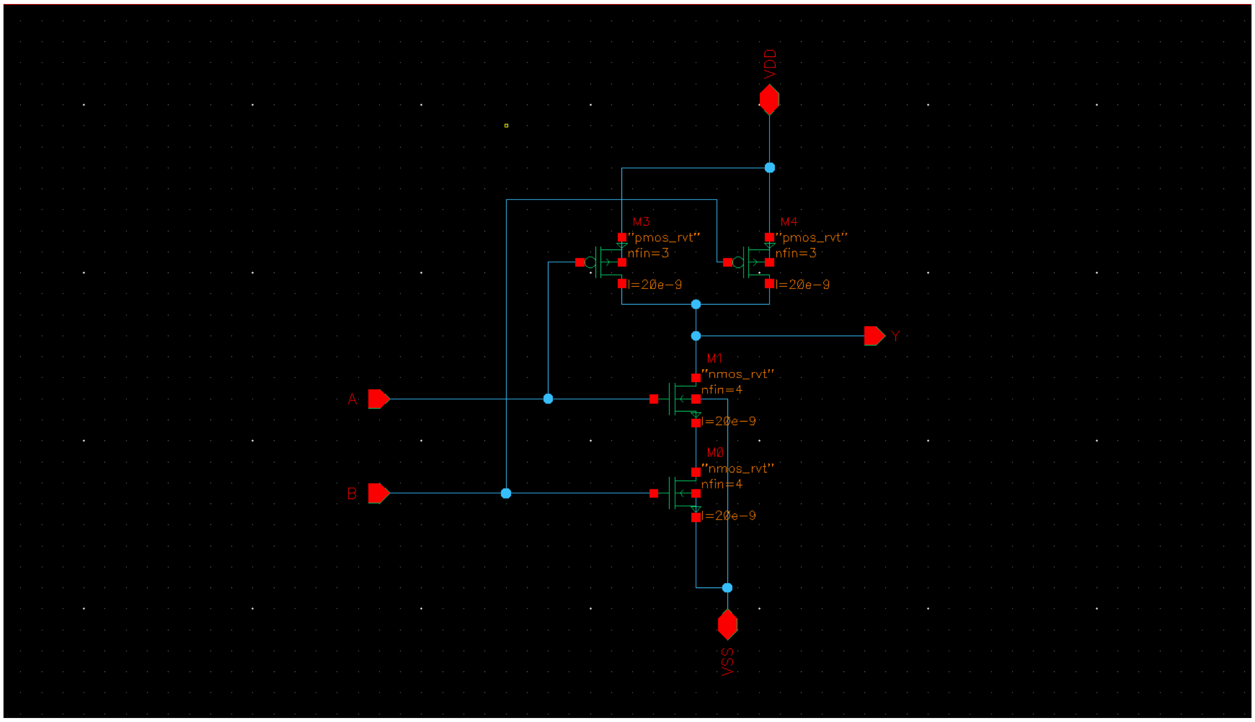
Note: the input to this stage is the inverse of what is to be multiplexed



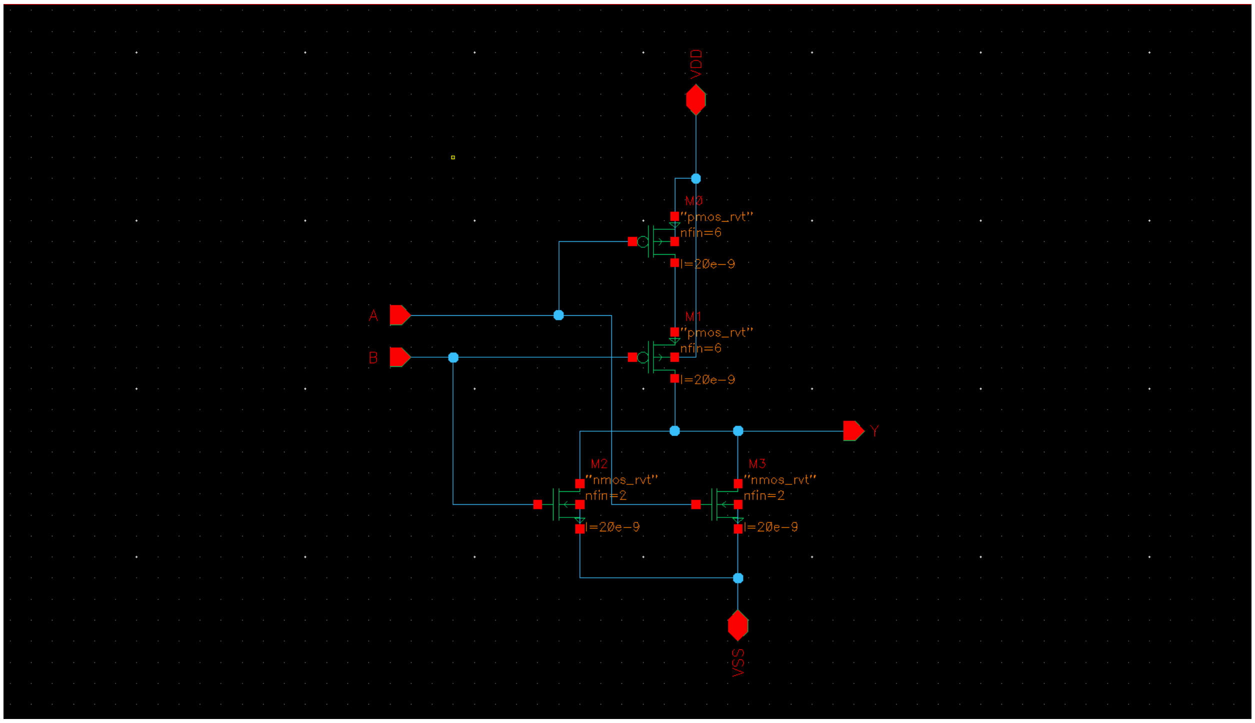
AND Gate



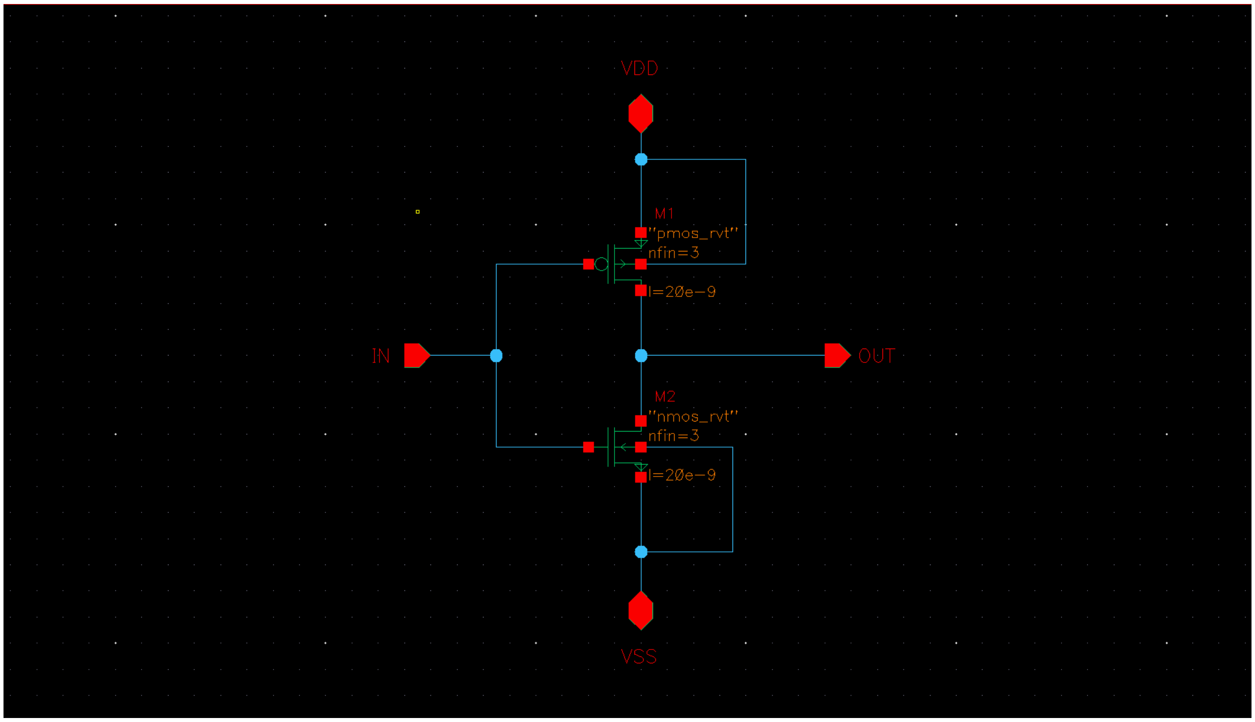
NAND Gate



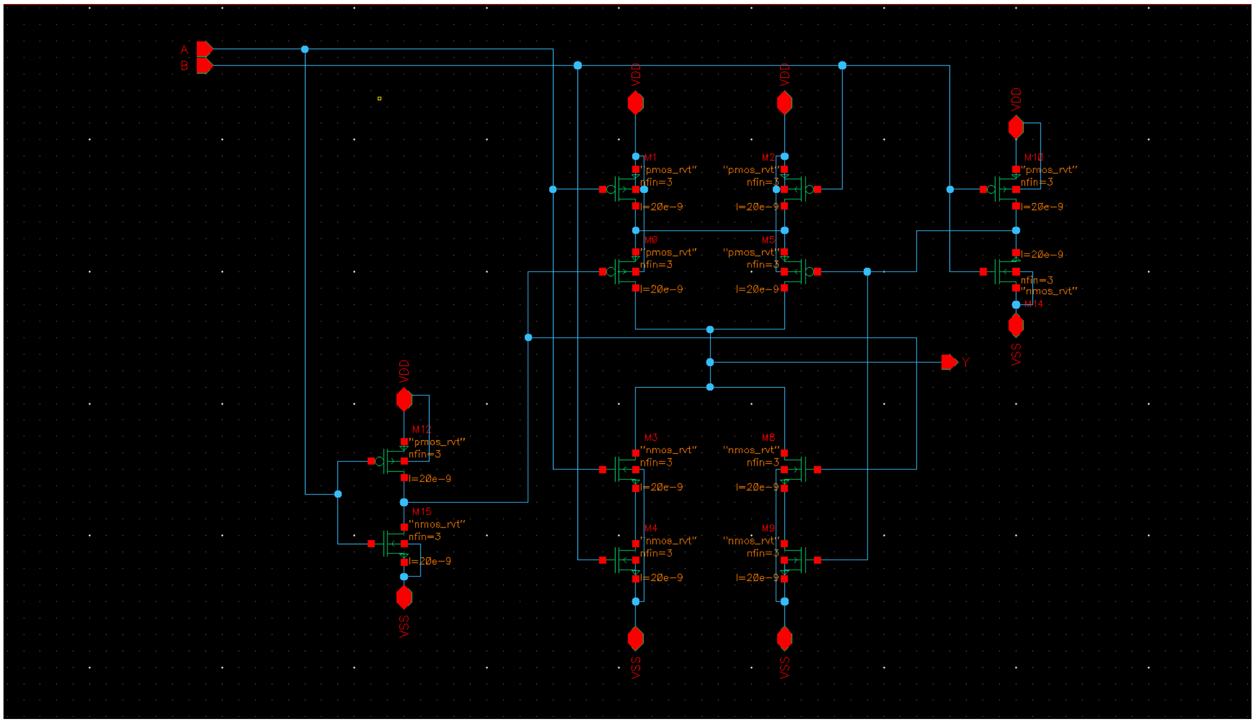
NOR Gate



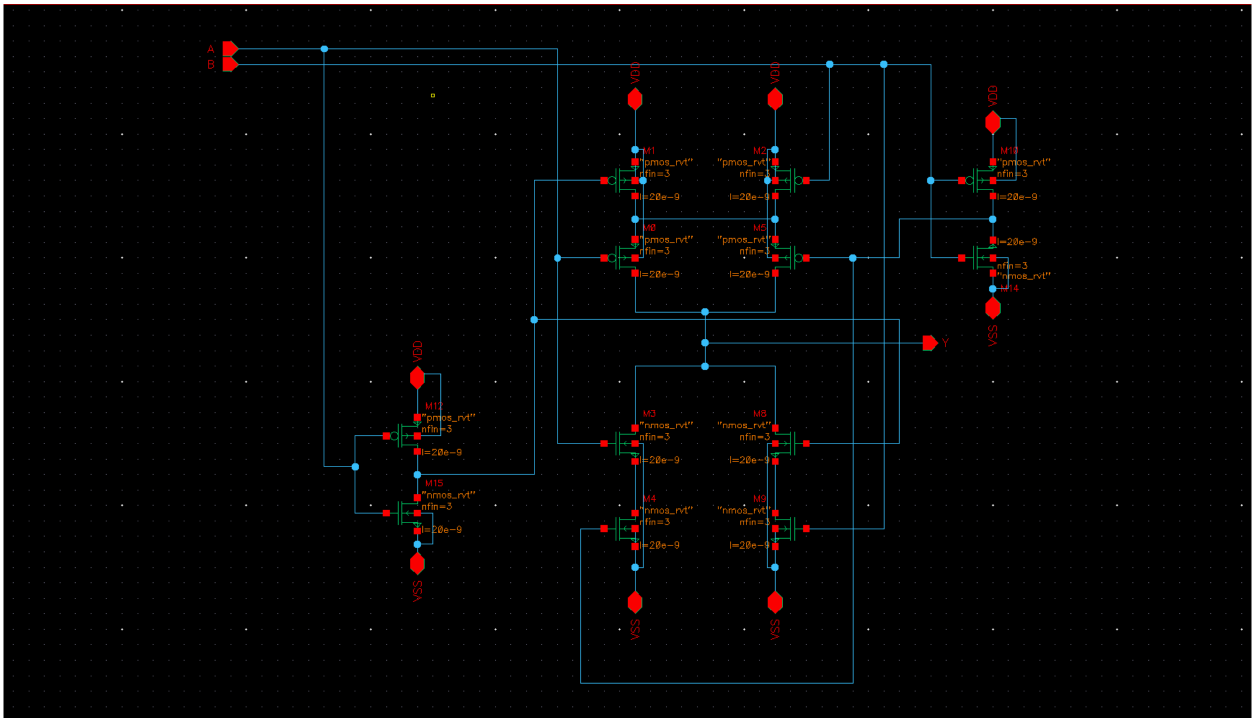
Inverter



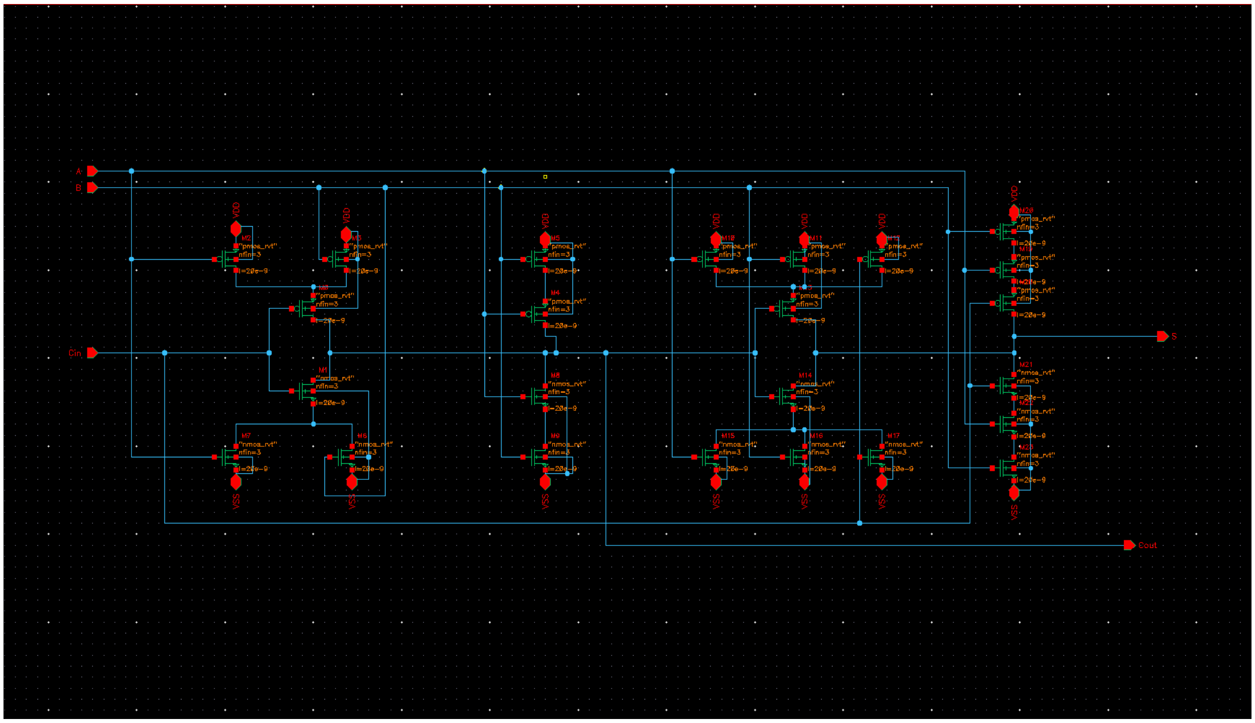
XOR Gate



XNOR Gate

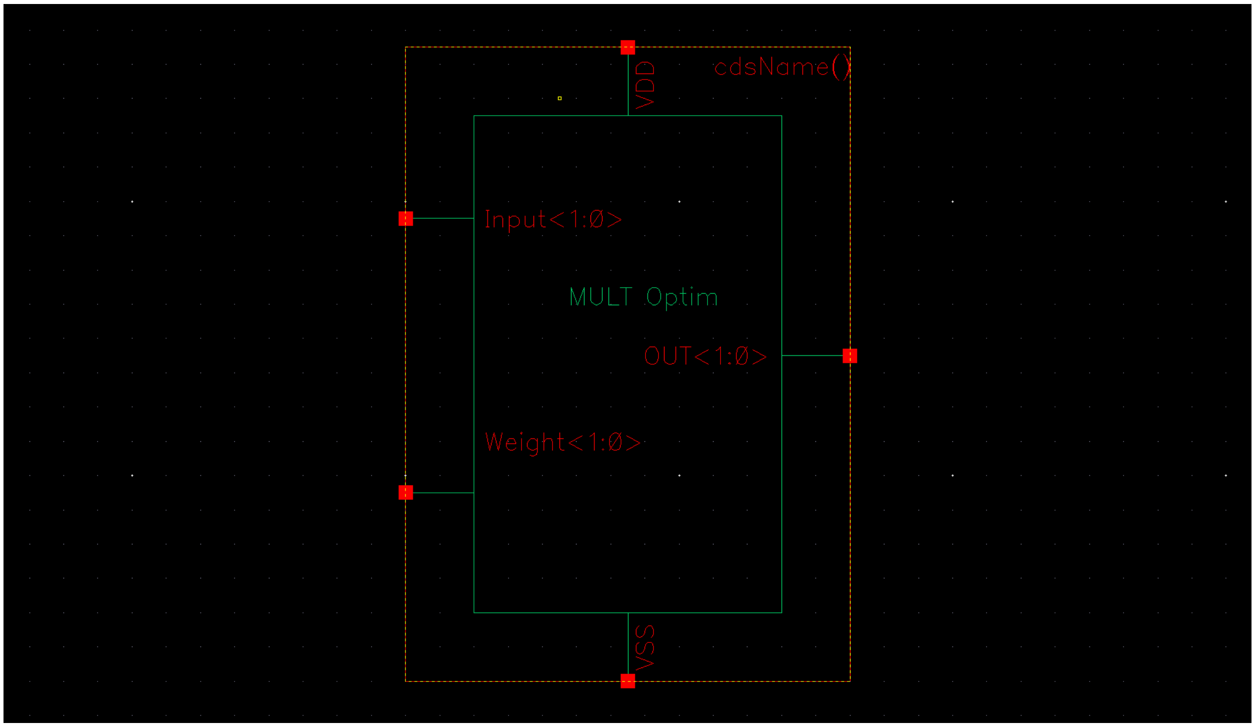


Mirror Adder Cell

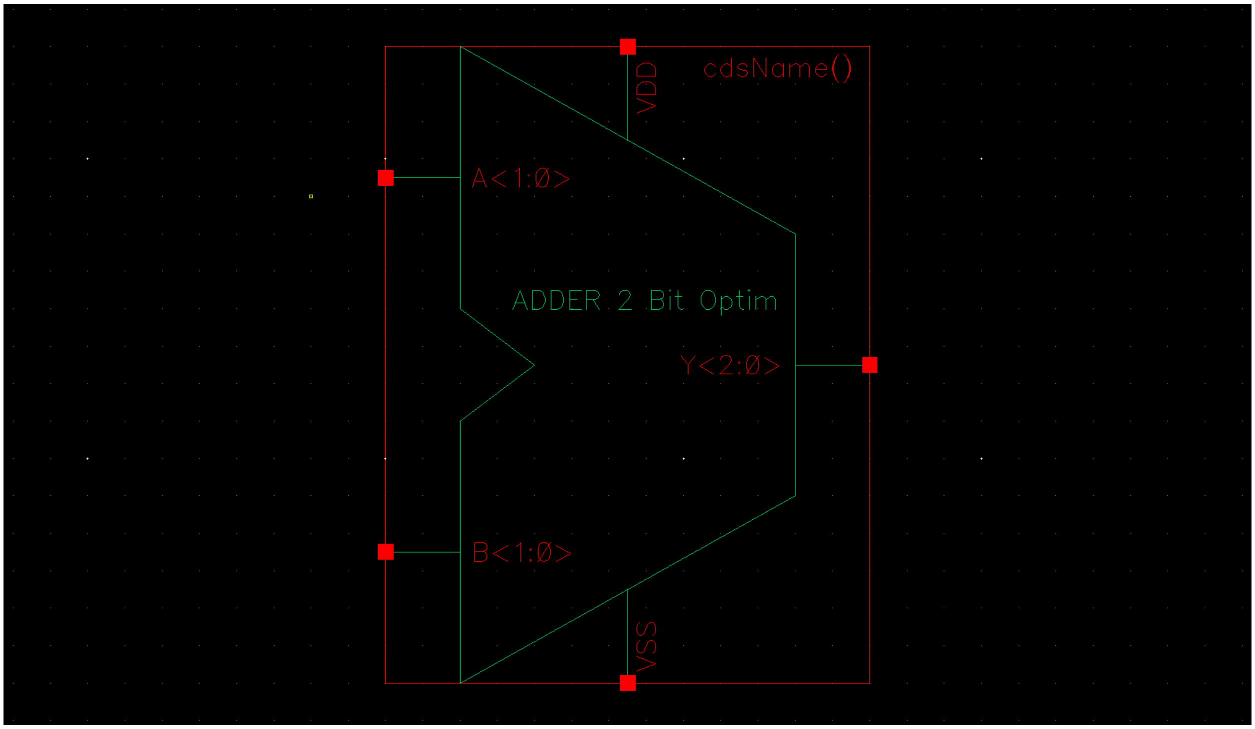


Appendix IV: Symbols

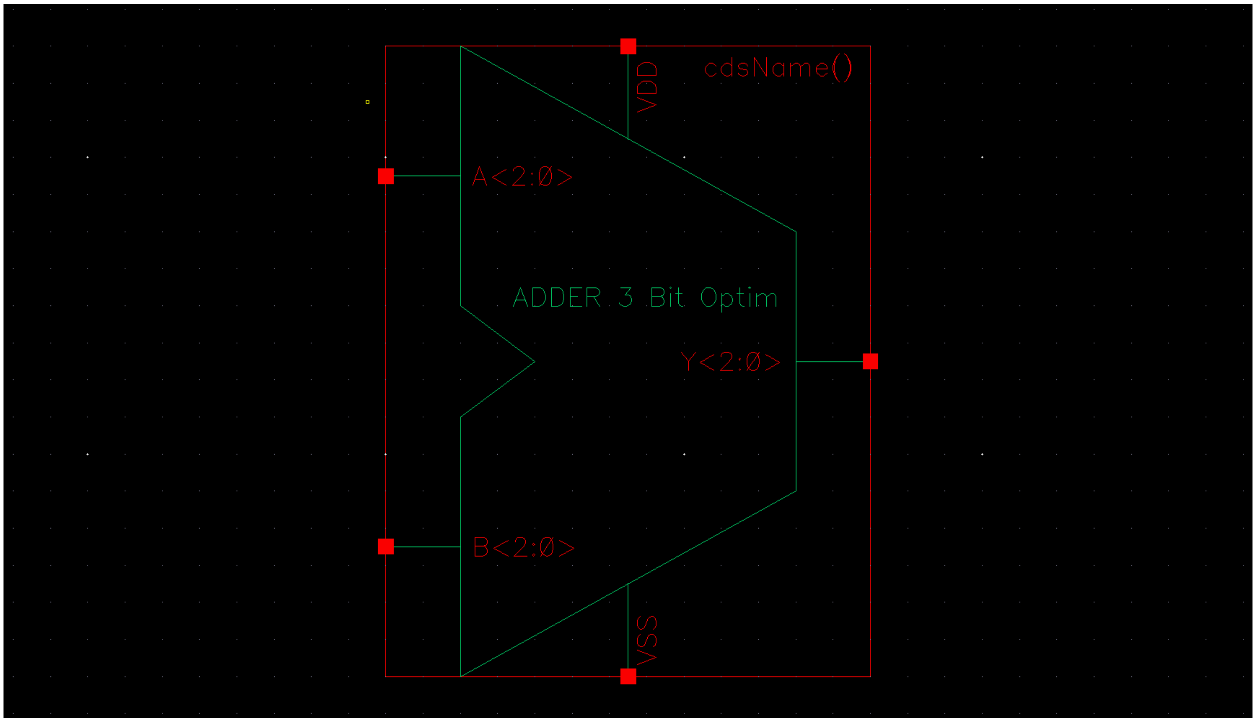
Multiplier



2-Bit Adder

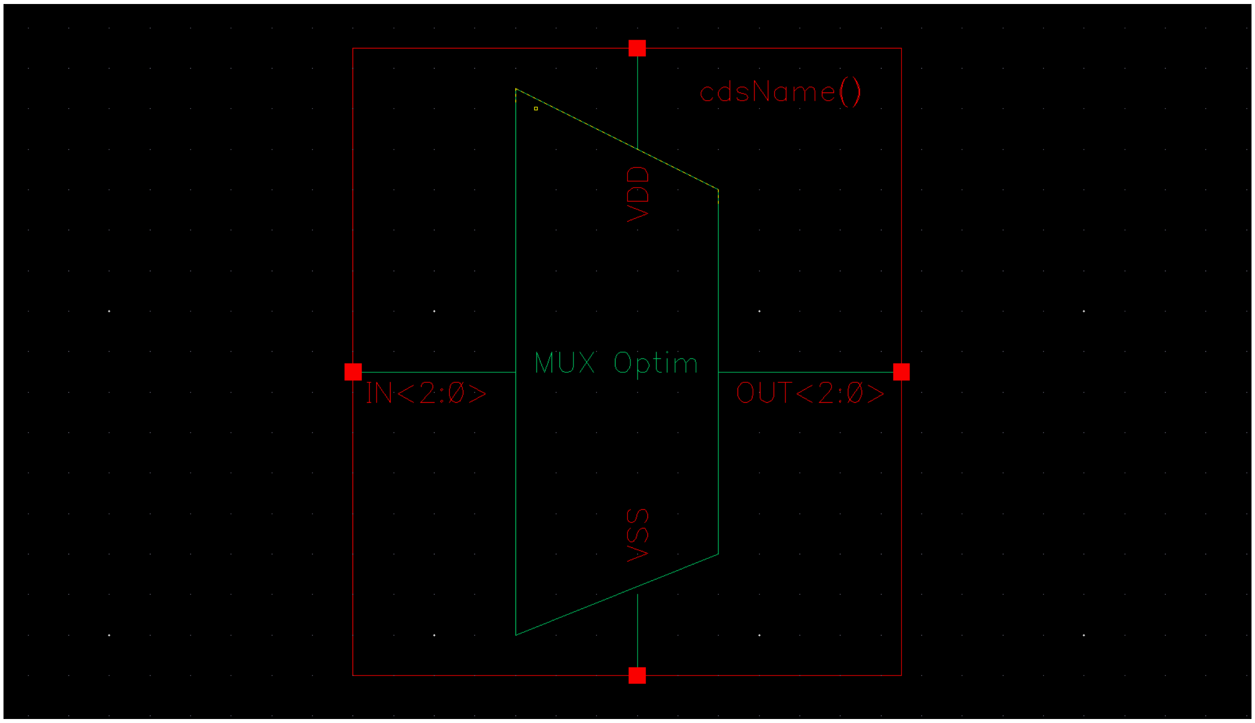


3-Bit Adder

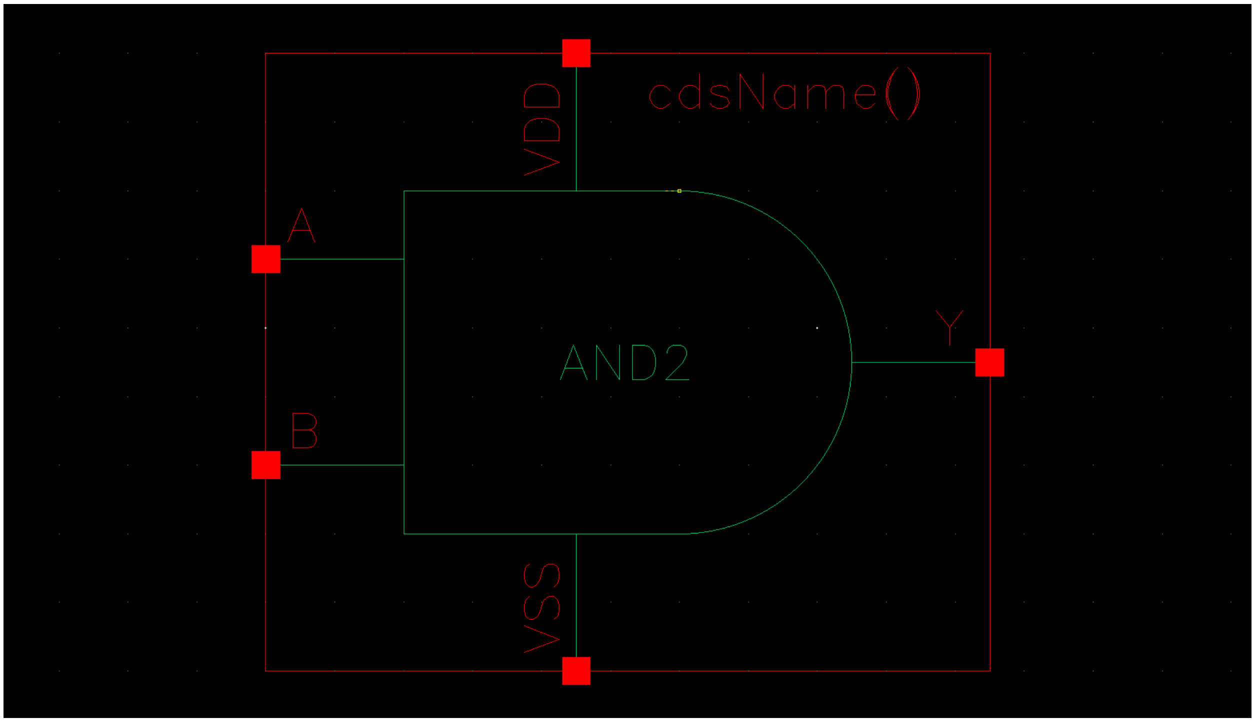


001

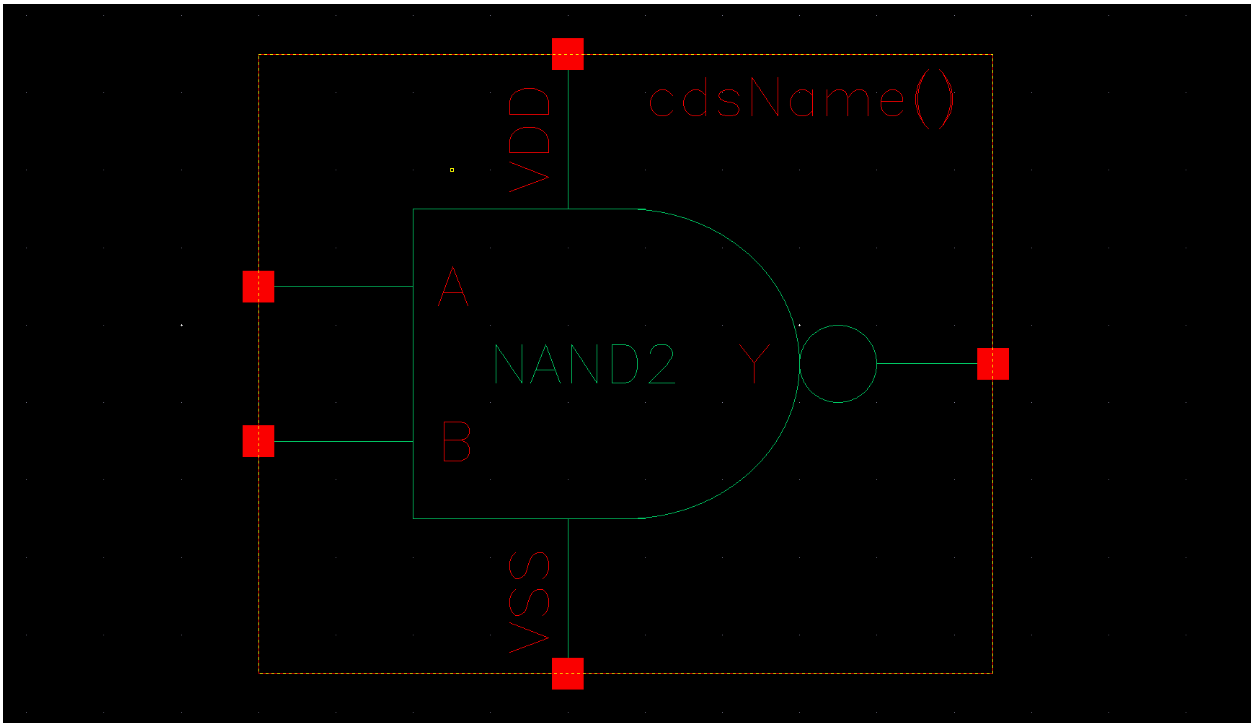
MUX



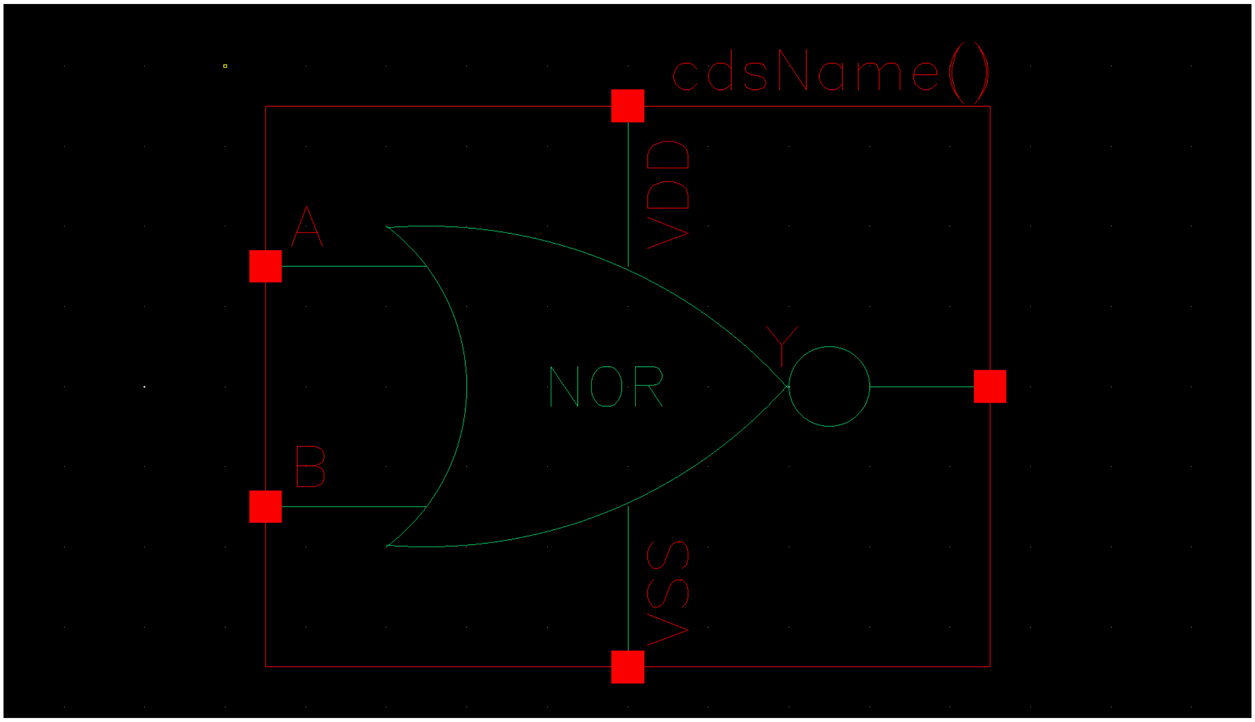
AND Gate



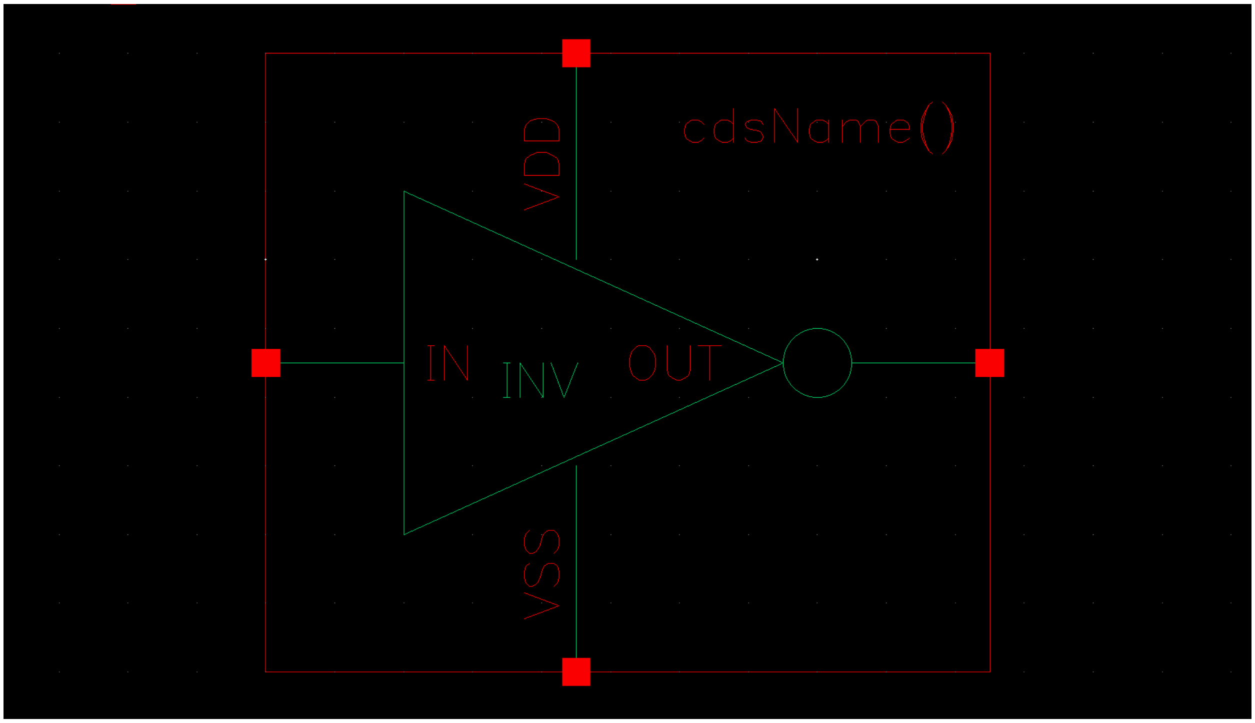
NAND Gate



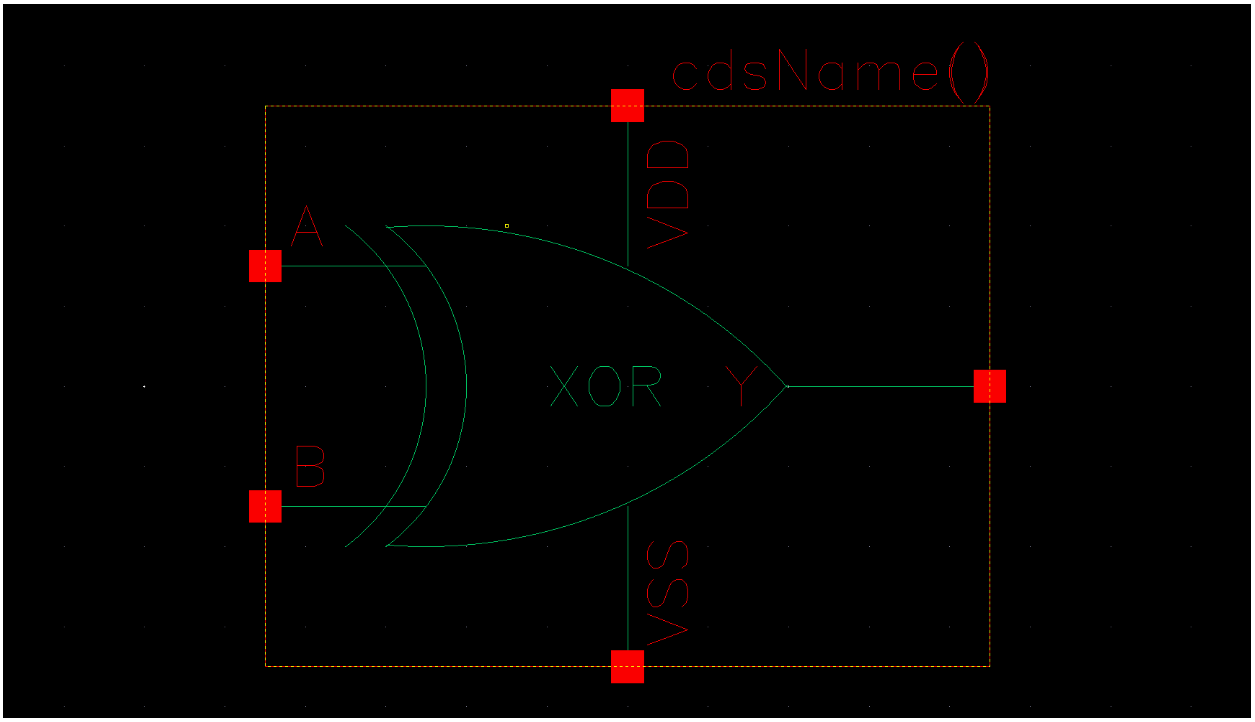
NOR Gate



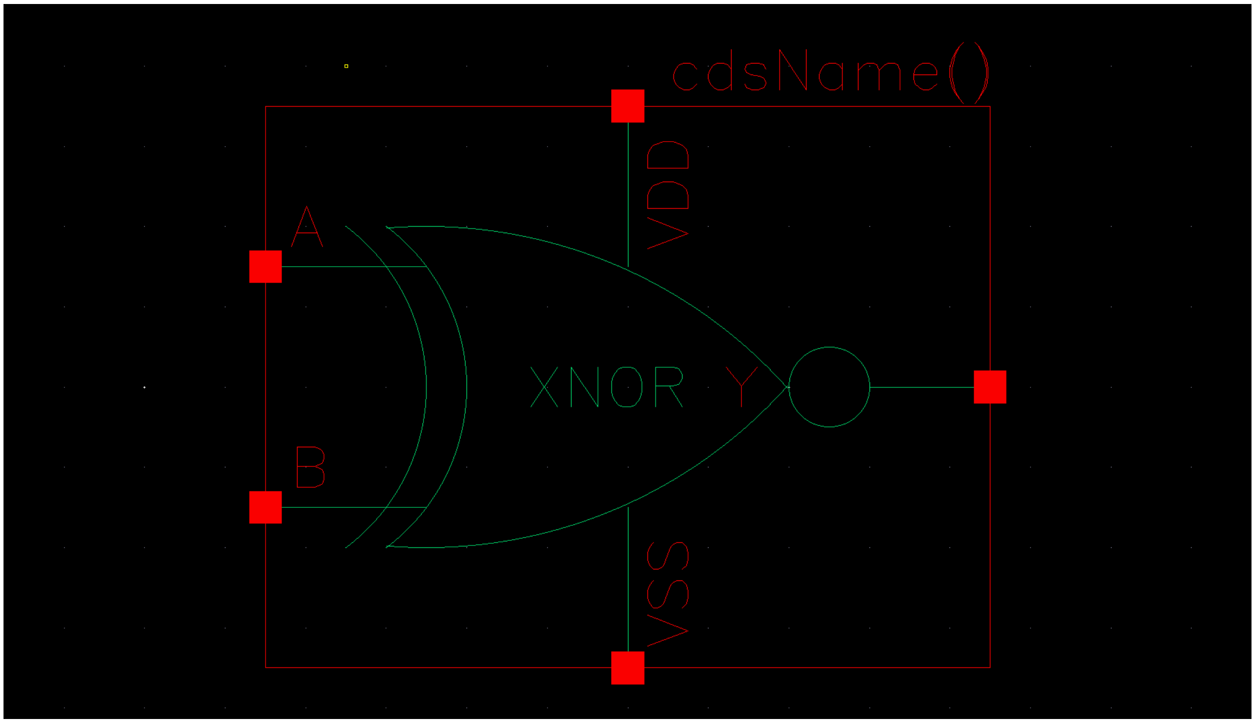
Inverter



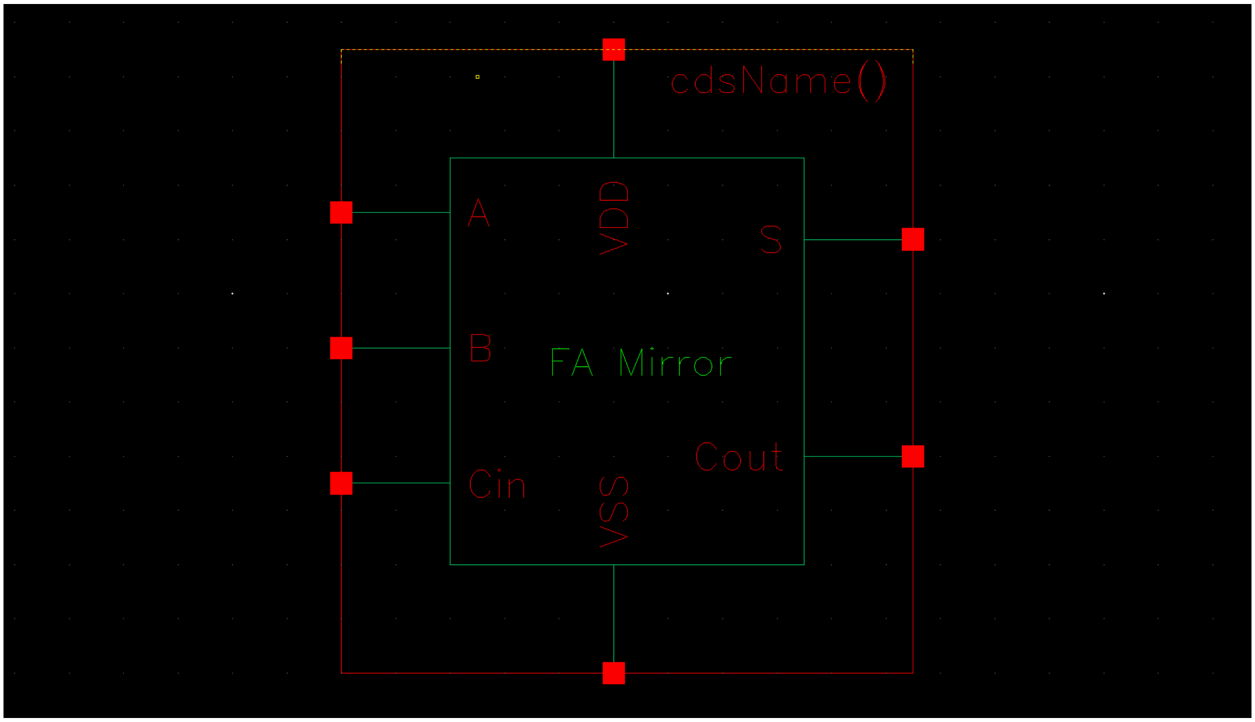
XOR Gate



XNOR Gate



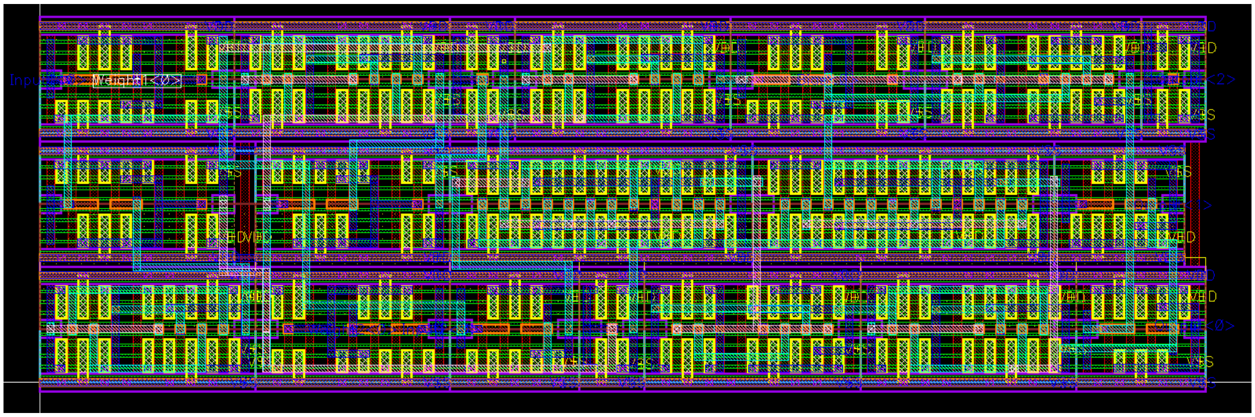
Mirror Adder Cell


cdsName()
A
VDD
S
B
FA Mirror
Cout
Cin
VSS

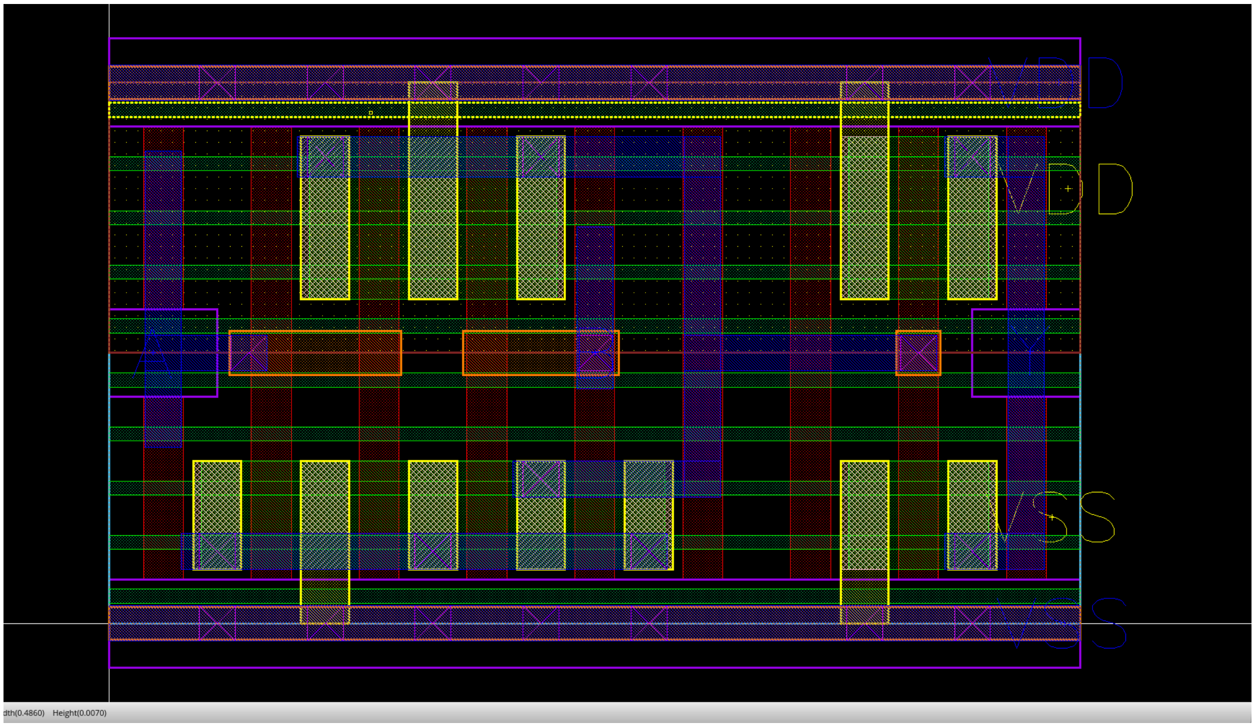
Appendix V: Layouts

Note: The non-gate submodules do not have a layout because we flattened the neuron

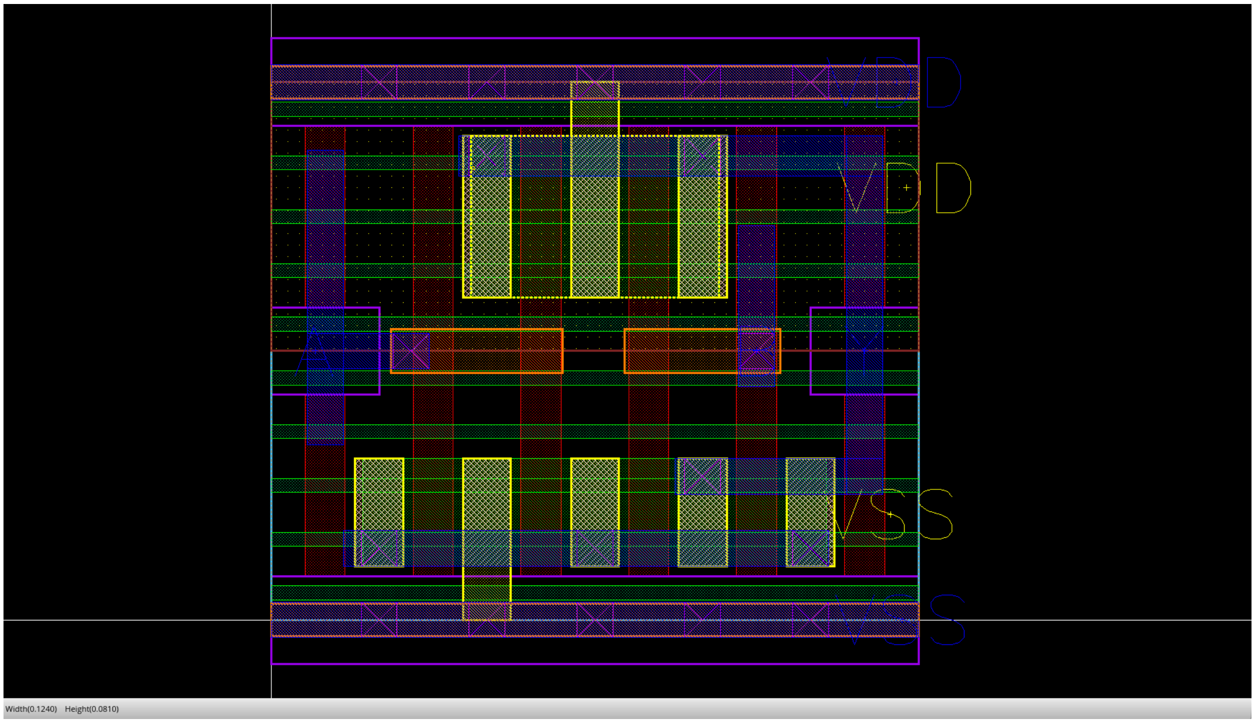
Neuron



AND Gate

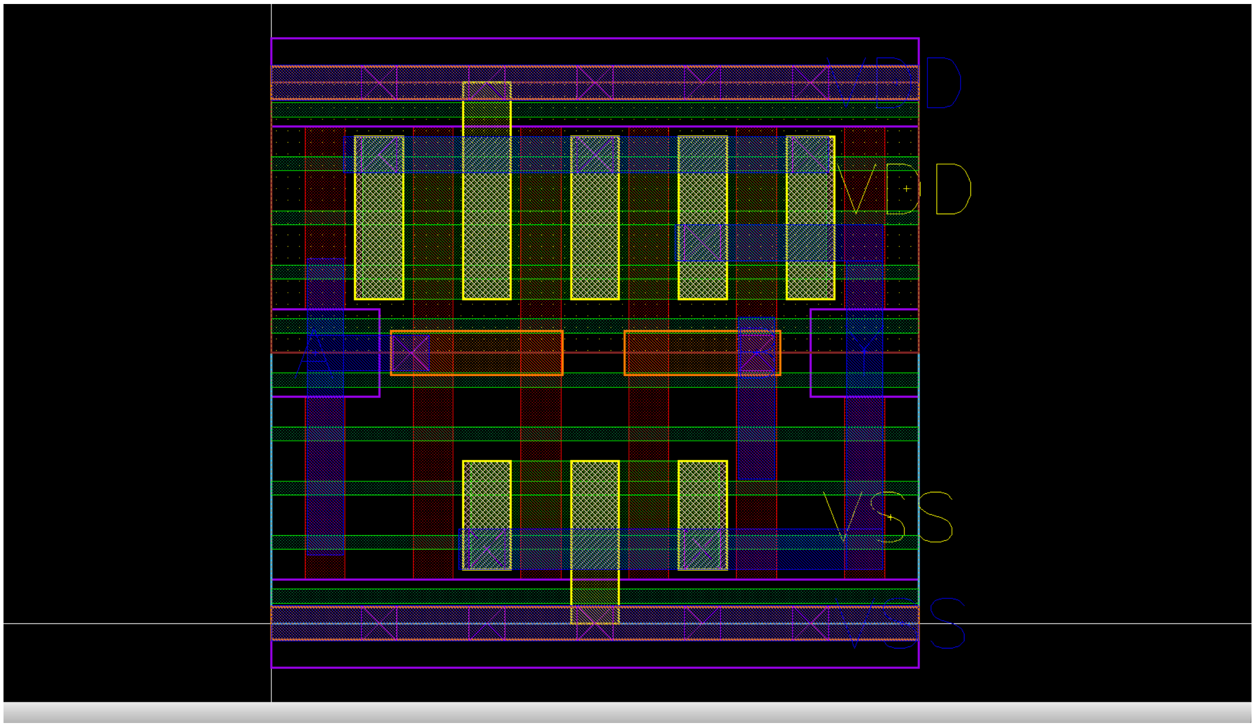


NAND Gate

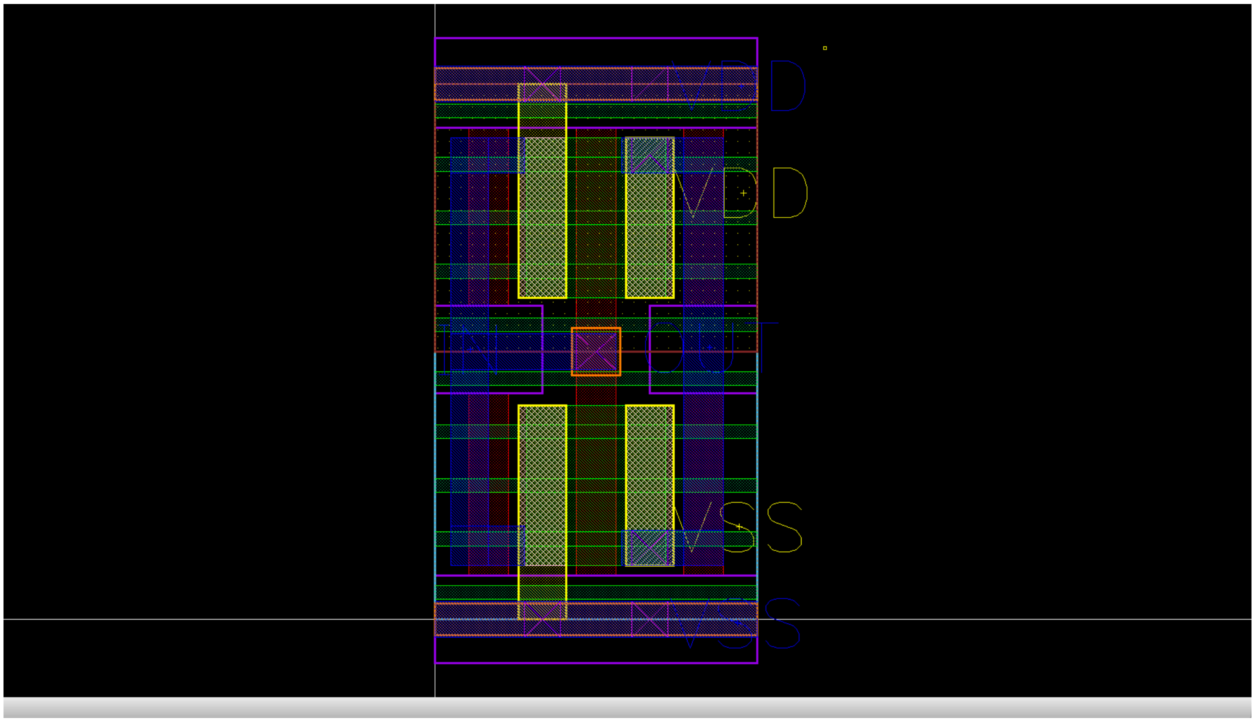


Width(0.1240) Height(0.0810)

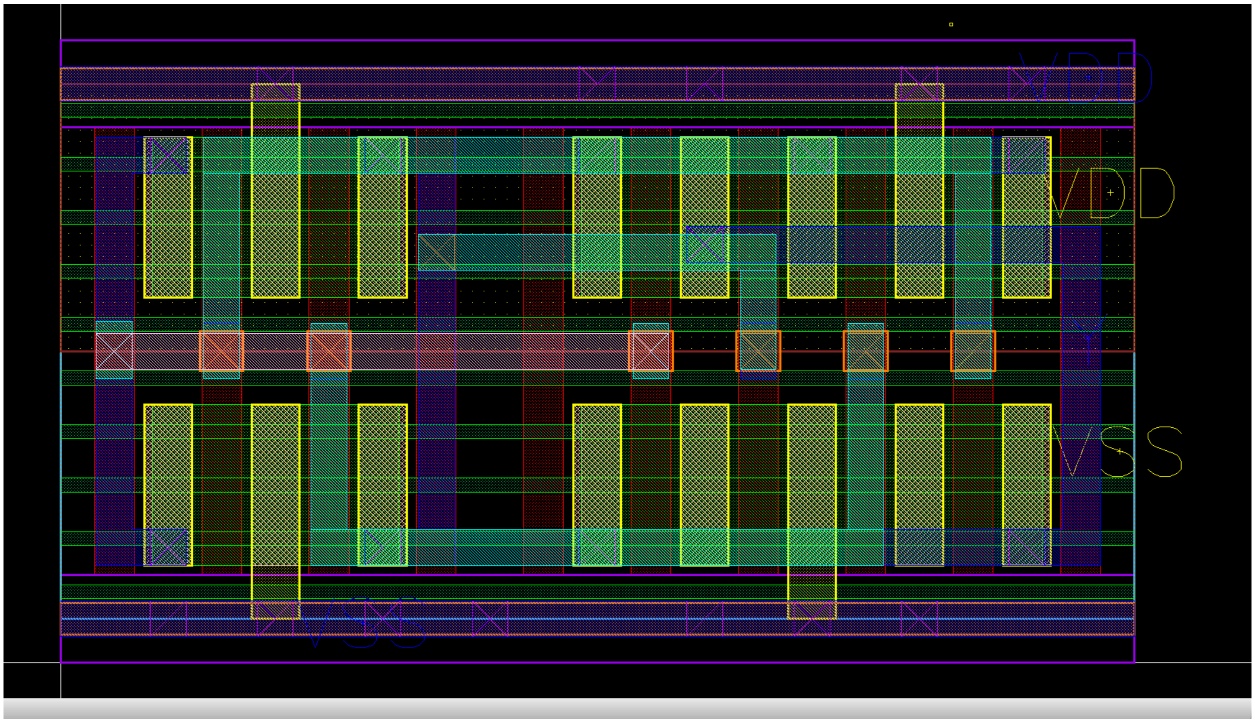
NOR Gate



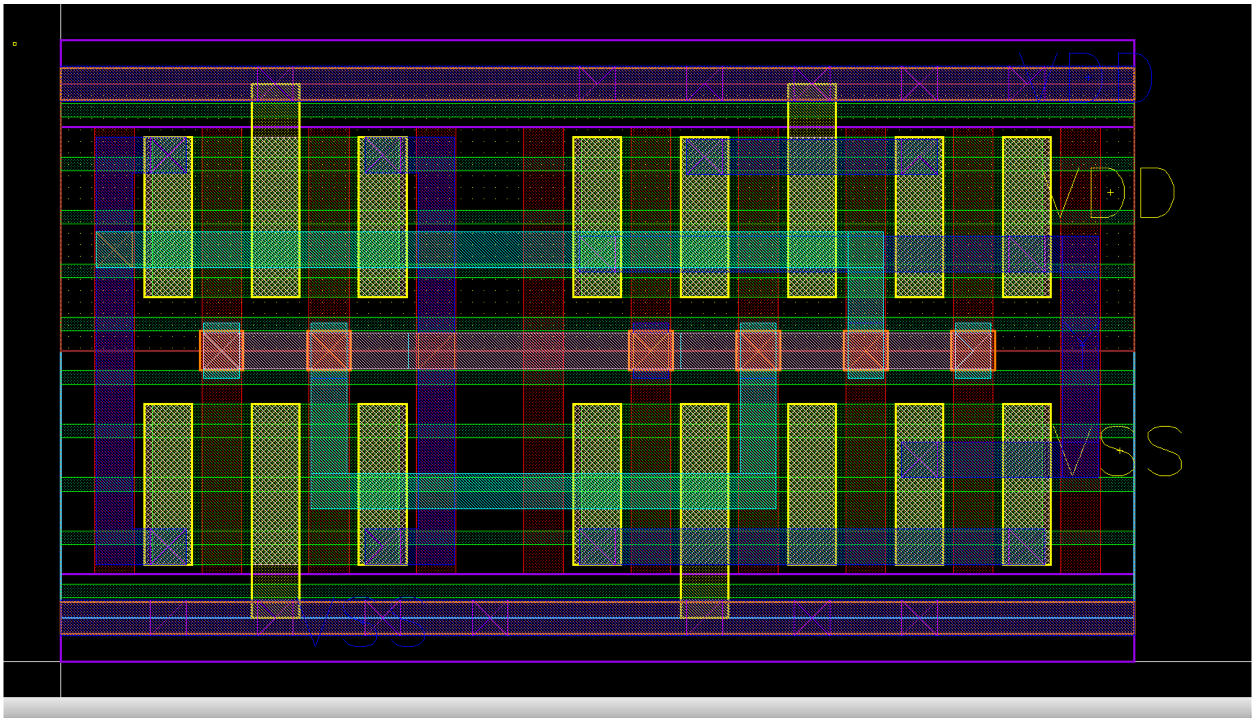
Inverter



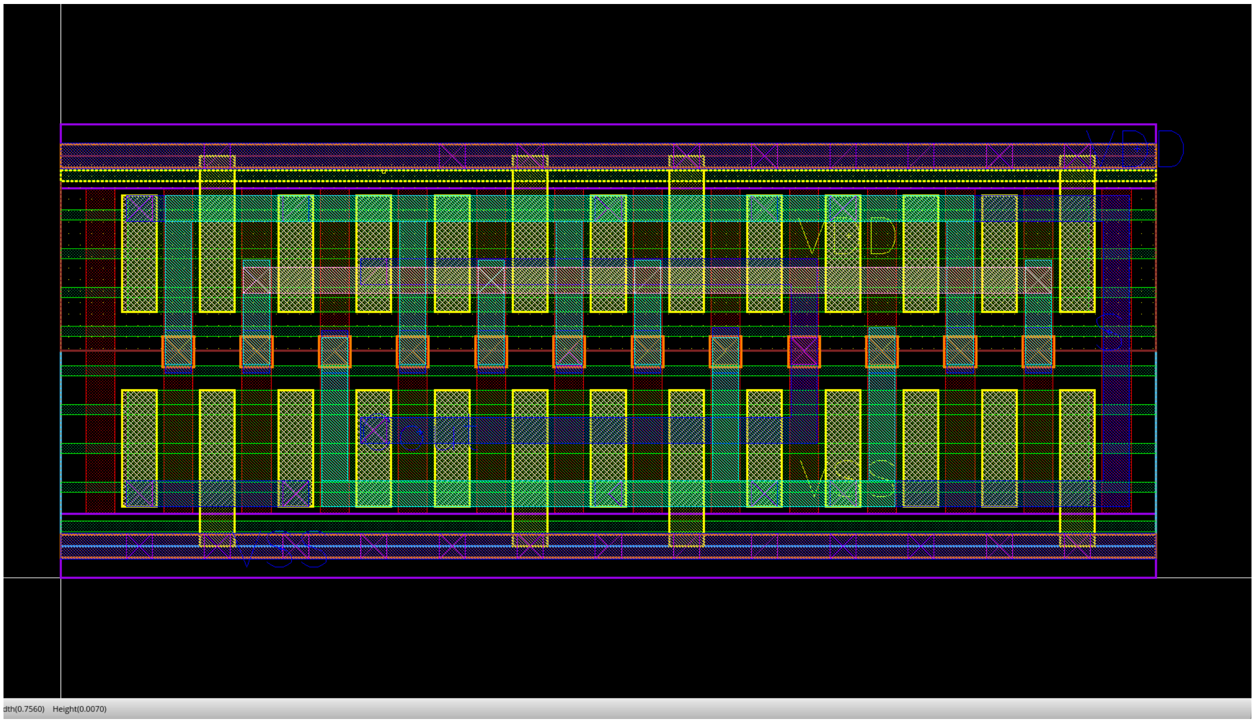
XOR Gate



XNOR Gate



Mirror Adder Cell


VDD
VDD
VSS
VSS
dth(0.7560)   Height(0.0070)