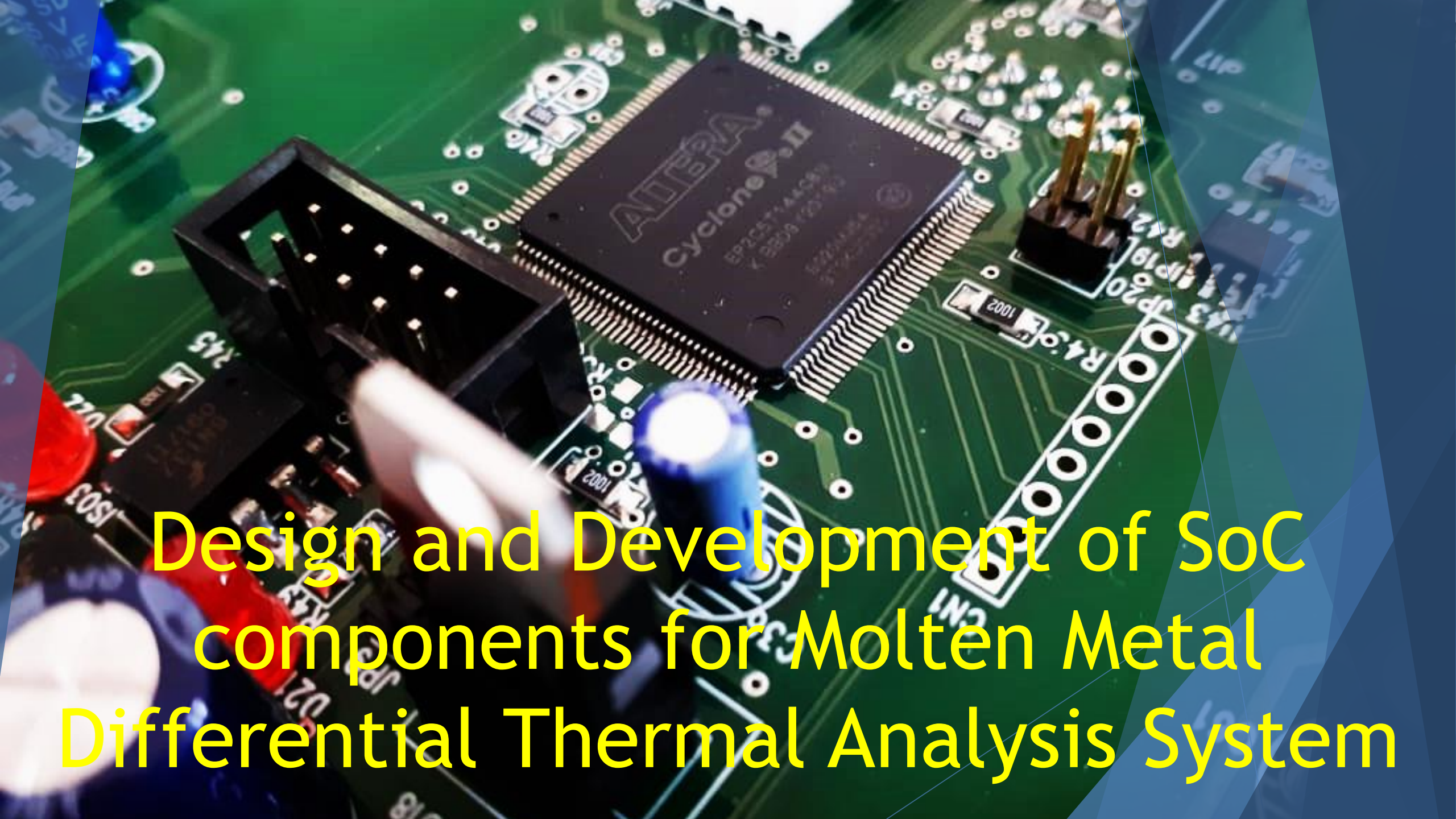


Design and Development of SoC components for Molten Metal Differential Thermal Analysis System

Background:

Thermal analysis systems predict metal properties by calculating the 1st and 2nd derivatives of the cooling curve. The derivative signals are filtered digitally in thermal analysis software. The software filtering misses out on some crucial details in the derivative curves.

Challenges:

The latest models of molten metal thermal analysis systems require a monotonic accuracy of 0.1°C and an absolute accuracy of 0.3°C in measurements of temperatures of the order of 1400°C.This requires a 16-bit ADC with integral linearity better than 2 counts in 65536(2 LSB in 16-bit).

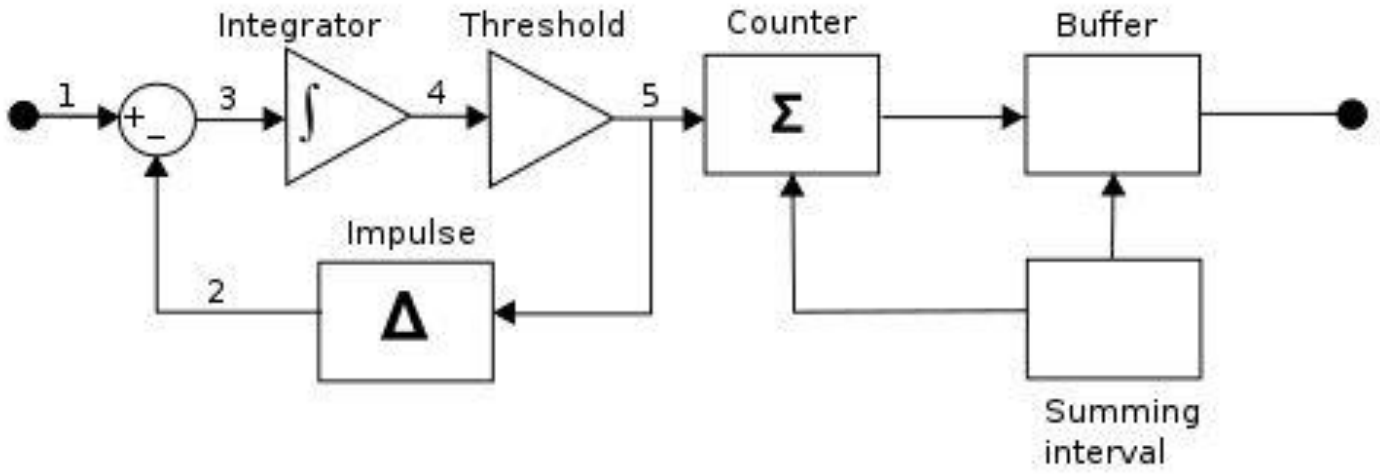
Also, thermal analysis systems are subject to heavy industrial noise requiring only integrating type of ADCs to be employed(for noise cancellation). Conventional integrating ADCs like dual slope ADCs demand unrealistic circuit parameters for 16 bit resolution.

The system must not miss out on sensing minute changes in derivative curves. So there is a need of hardware acceleration. Since the system is subjected to high voltage induction noise, there is a need of Galvanic Isolation.

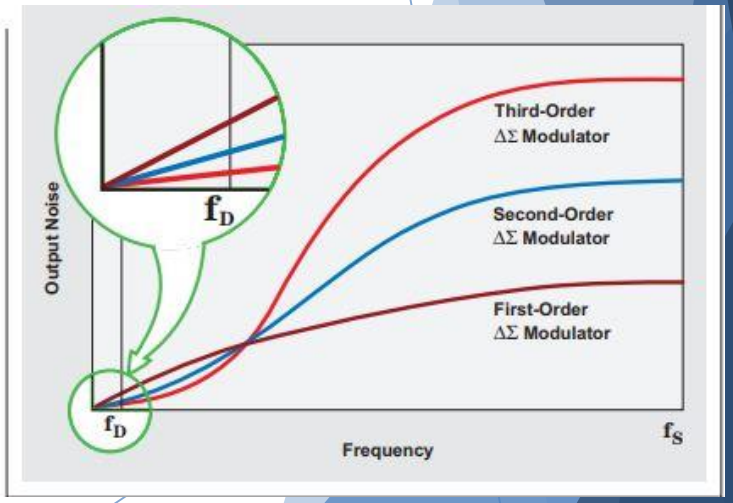
Cooling Curve and Derivatives
(Source: FPS repository)

Solution:

- We need an integrating type ADC that gives 16-Bit resolution at a speed of 25 sps with minimum hardware, and is easy to isolate.
- The perfect solution for this is a Sigma-Delta ADC i.e. an Isolated Sigma-Delta modulator with appropriate digital filtering(using FPGA). It is an oversampling ADC which can get highly accurate ADC readings with the hardware of just a 1-Bit ADC and 1-Bit DAC.
- In a sigma-delta modulator, the “in-band” noise is attenuated and out of band noise is enhanced. The out of band noise is cut off by the digital decimation filter(LPF).This improves in-band SNR.
- Additionally, the output of the modulator is an single bit-stream and hence is easier to isolate.

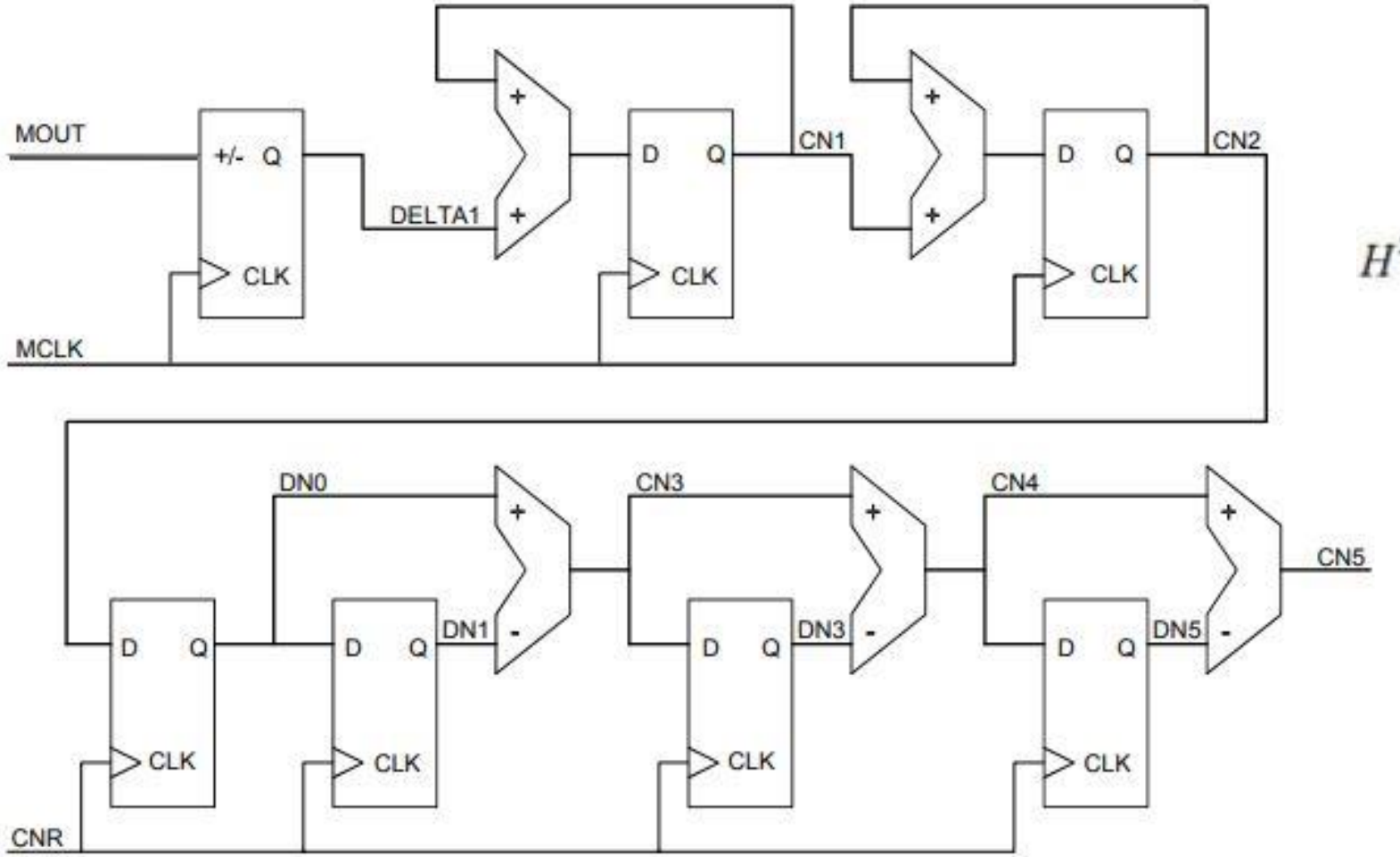


Sigma-Delta ADC scheme(Source: Wikipedia)



Sigma-Delta Modulator Noise shaping (Source: Texas Instruments Paper)

Decimation Filter Design:



$$H(z) = \frac{1 - z^{-262144}}{262144(1 - z^{-1})}$$

$$H^3(z) = \frac{(1 - z^{-262144})^3}{262144^3} \frac{1}{(1 - z^{-1})^3}$$

Since the order of the modulator is 2 the order of decimation filter is at least 2. In this case the order is 3.

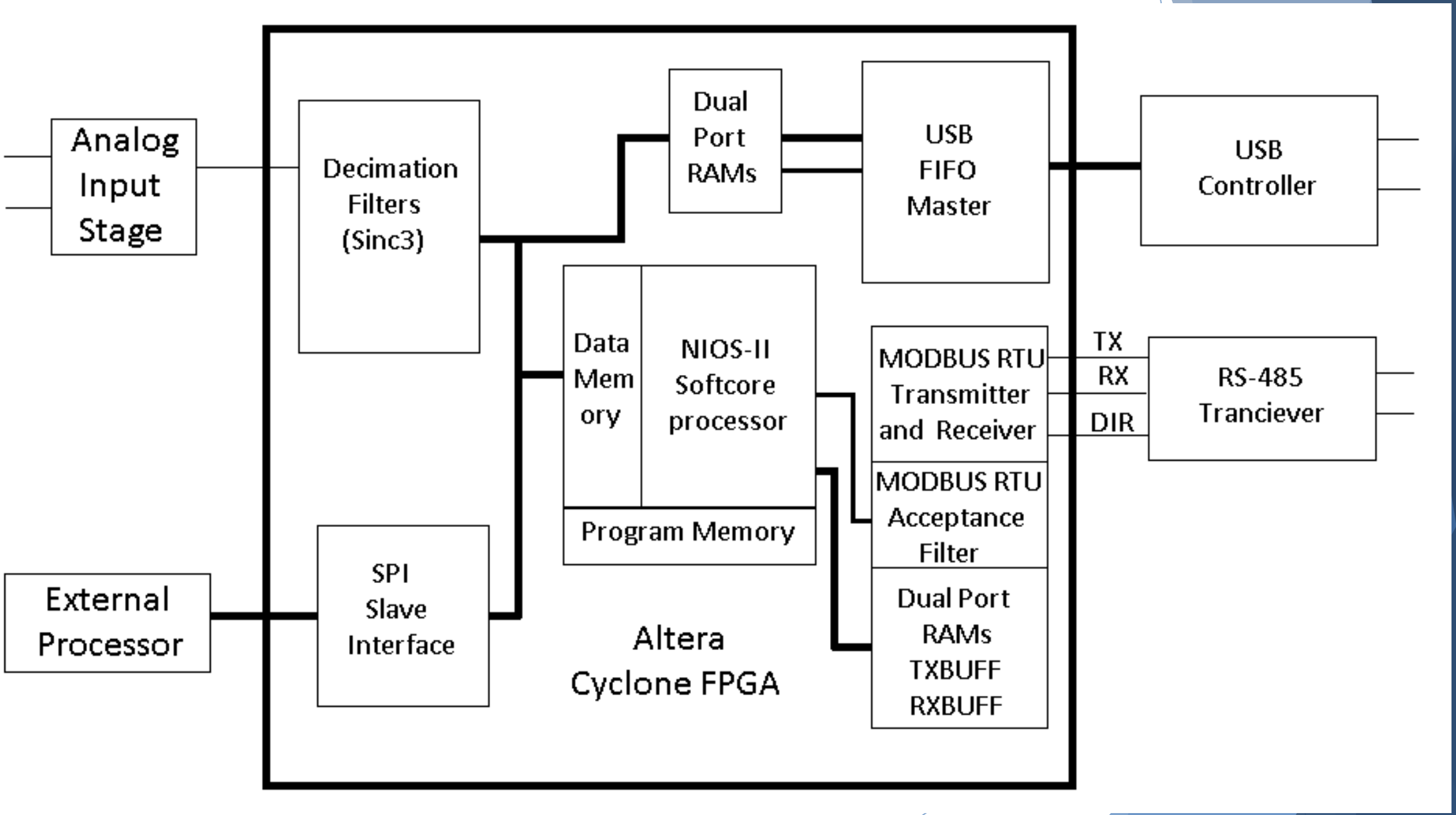
Decimation ratio : 262144

System clock:26.2144 MHz

Decimation Clock = System Clock/4

Integration time has to be integral multiple of power-line Frequency(50 Hz) period 20 ms.

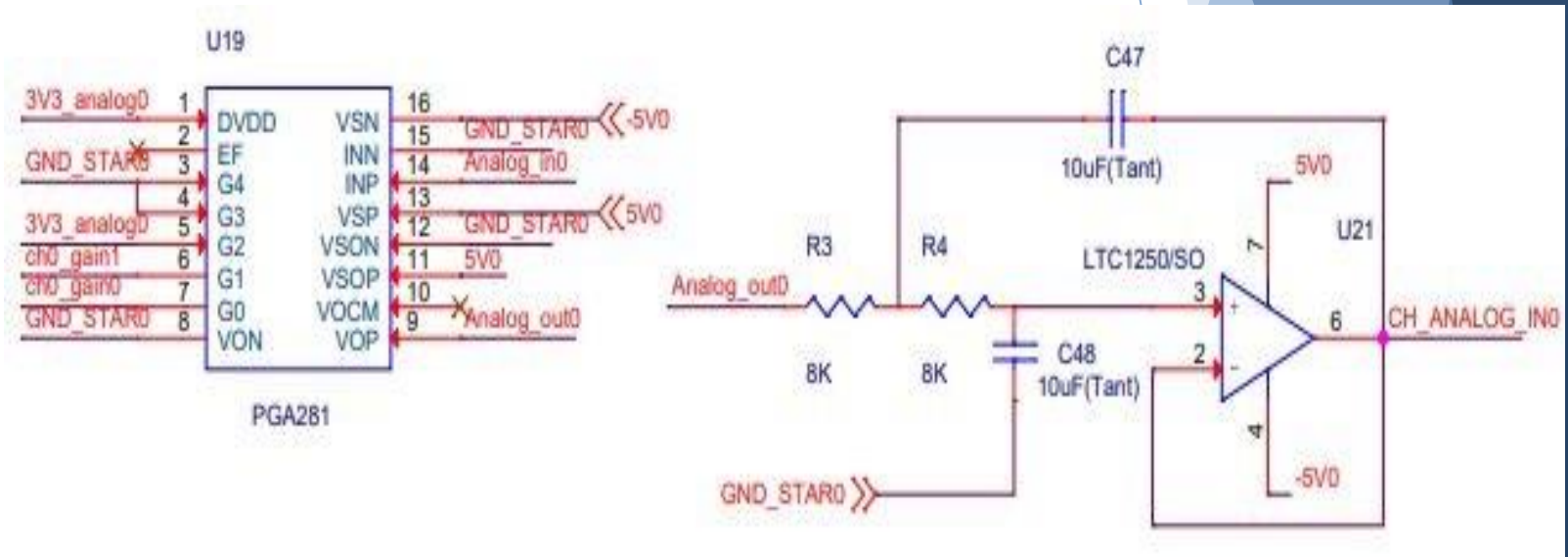
System Block Diagram:



Analog Input Stage Design:

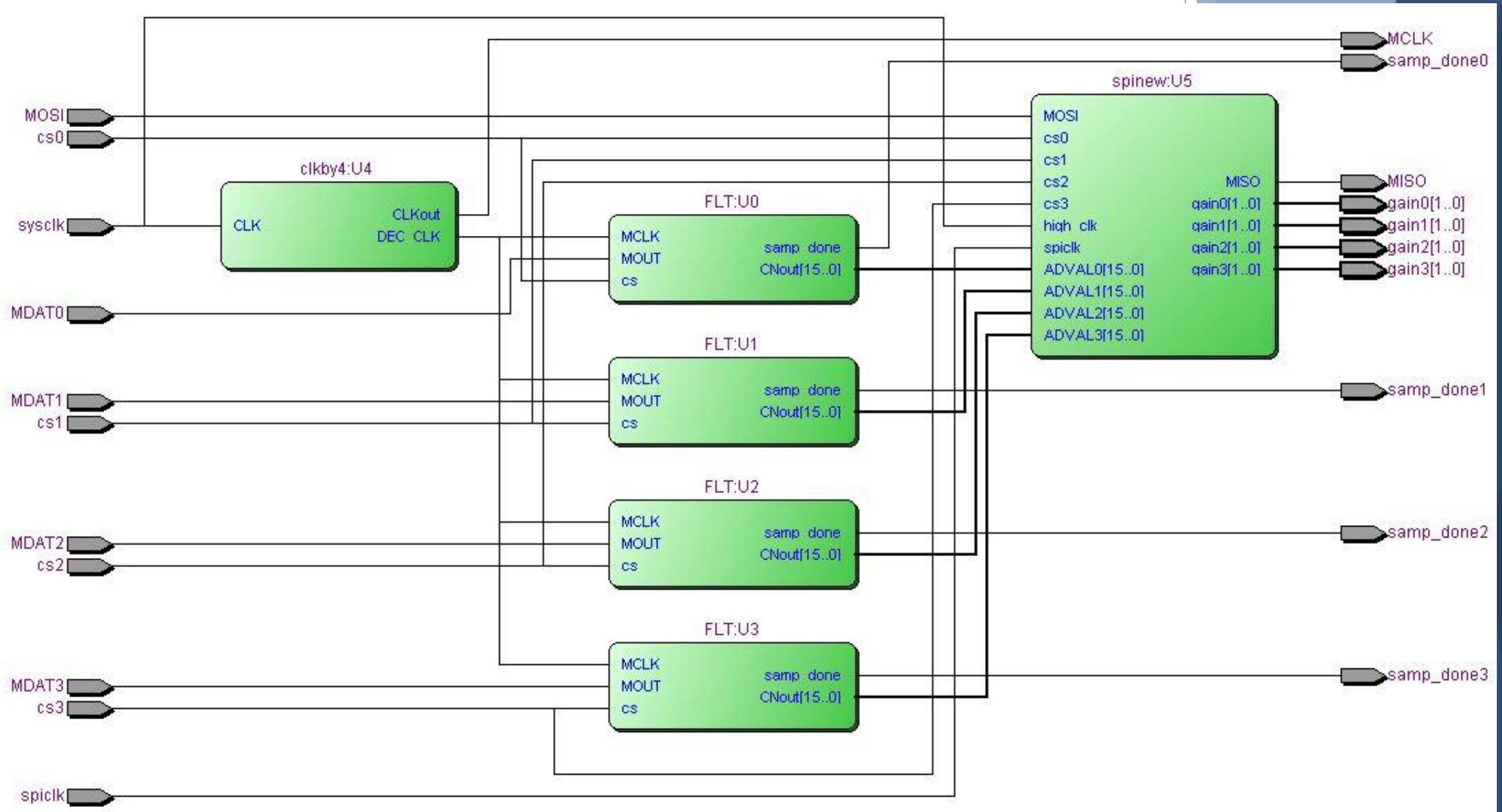
4 independent Analog inputs:
Time multiplexing of inputs is not possible as the Sigma-delta ADC has step input latency.

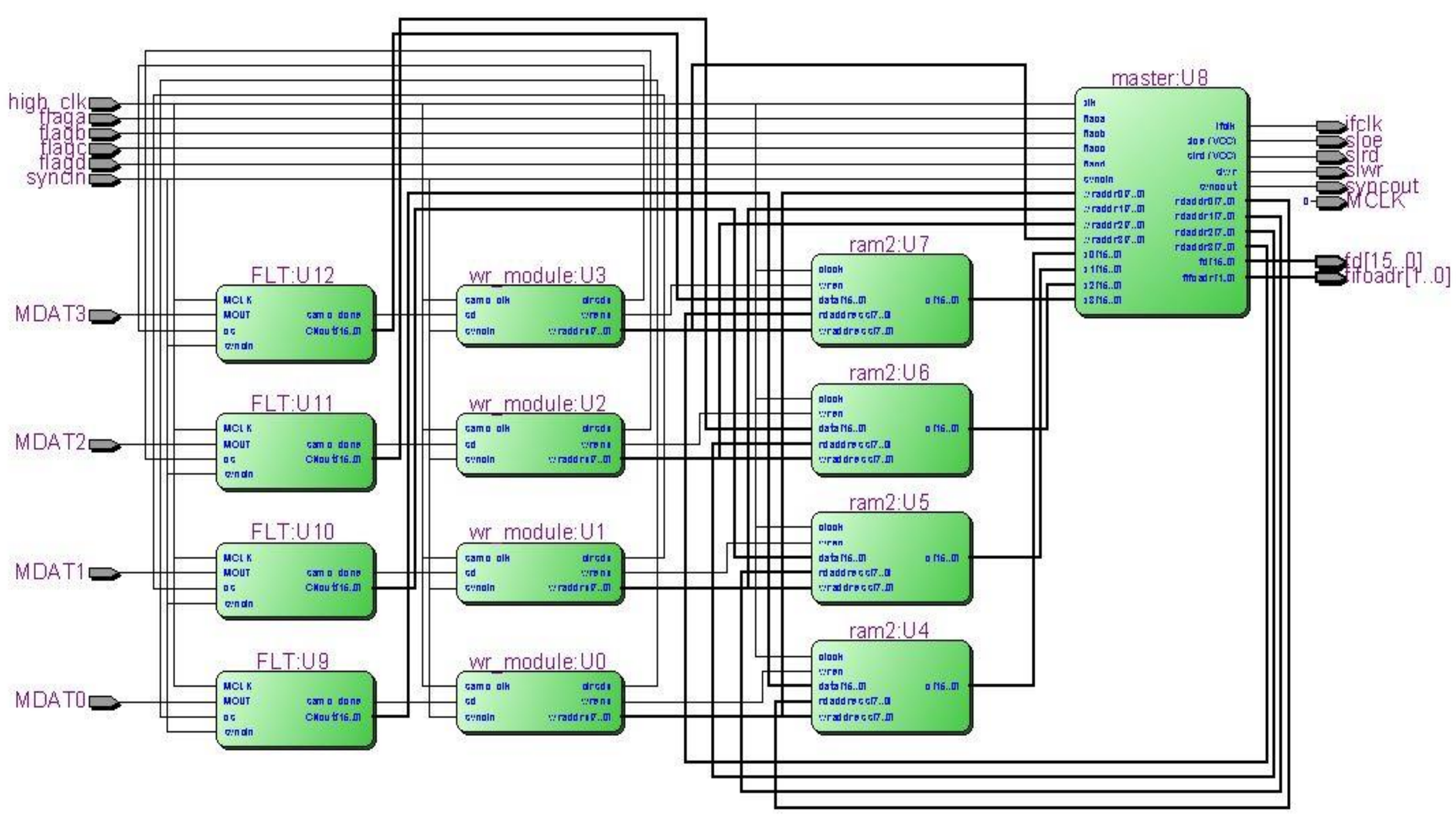
Op-Amp used: LTC1250
Low input-offset current
And ultra-low offset drift



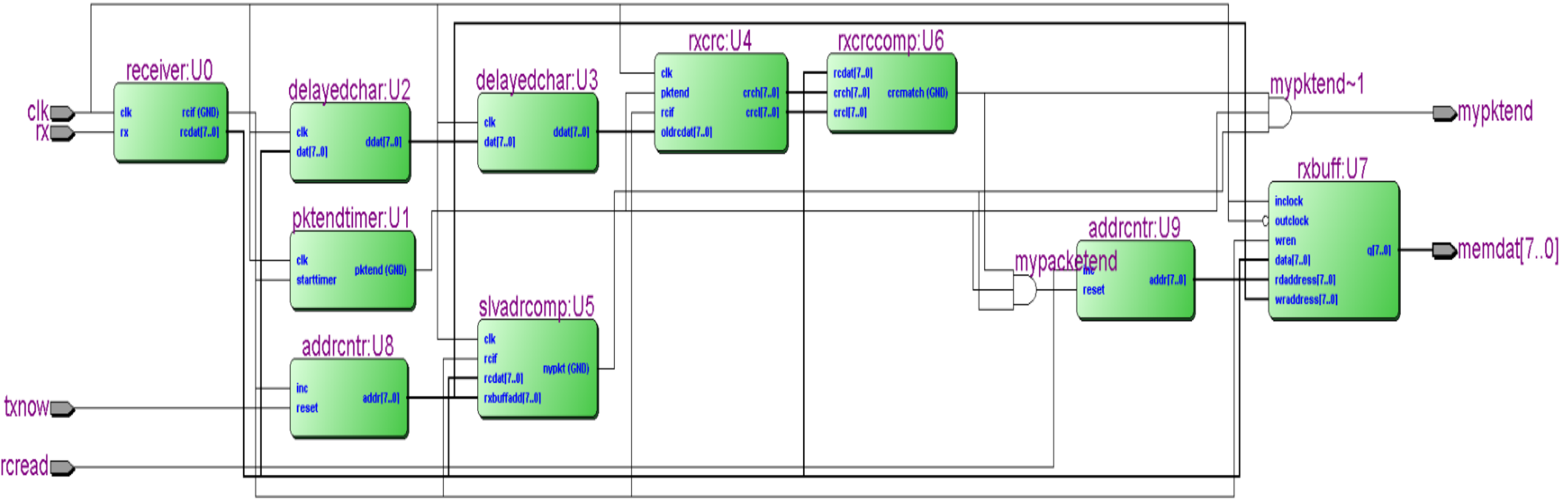
PGA and Active Anti-Aliasing Filter

RTL of Decimation filters and SPI block:

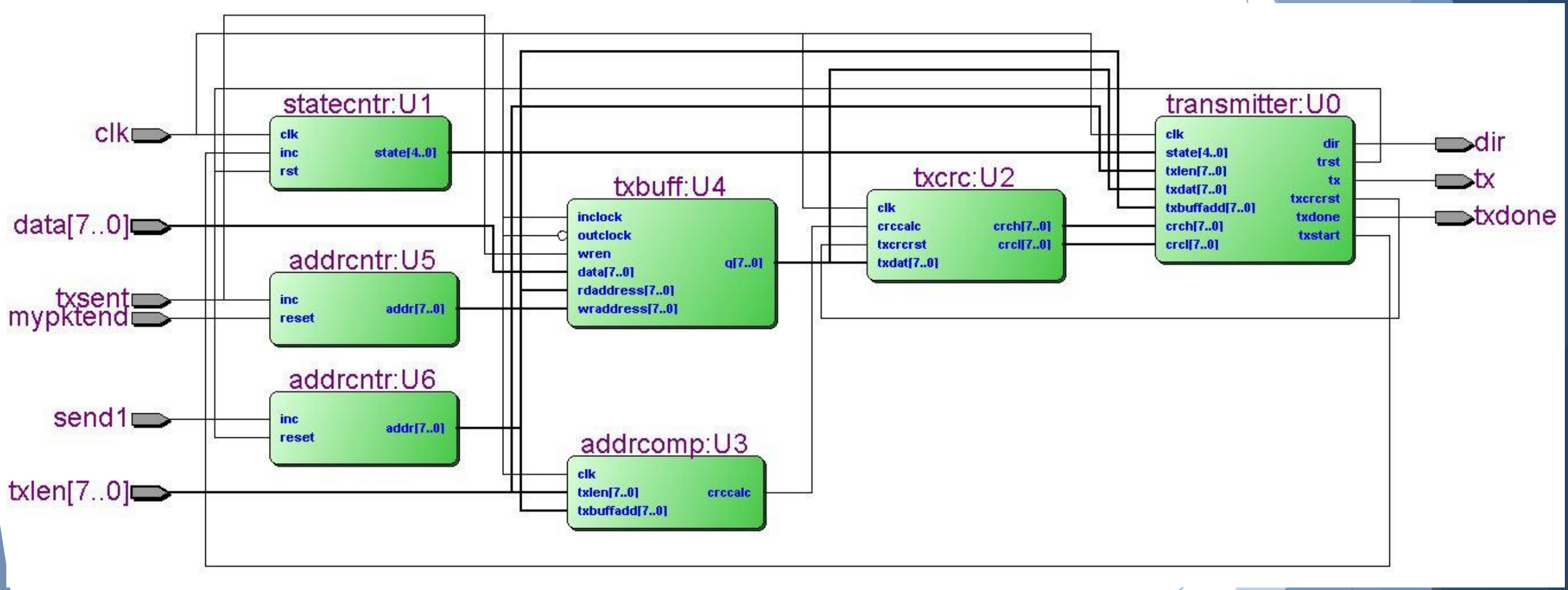



high_clk
flaga
flagb
flagc
flagd
syncin
MDAT3
MDAT2
MDAT1
MDAT0
FLT:U12
FLT:U11
FLT:U10
FLT:U9
wr_module:U3
wr_module:U2
wr_module:U1
wr_module:U0
ram2:U7
ram2:U6
ram2:U5
ram2:U4
master:U8
ifclk
sloe
slrd
slwr
syncout
MCLK
fd[15..0]
fifoadr[1..0]

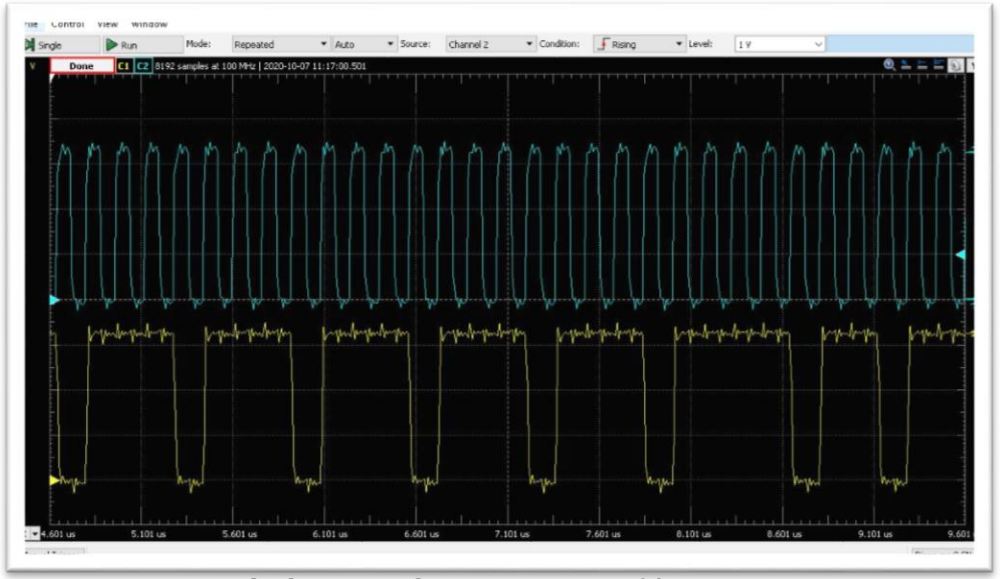
MODBUS receiver RTL



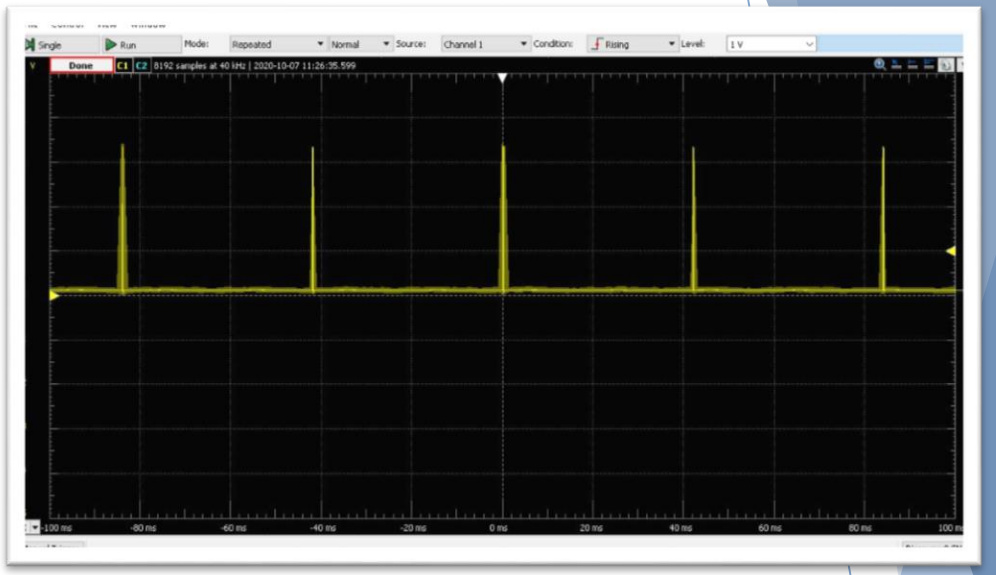
MODBUS transmitter RTL



Results:

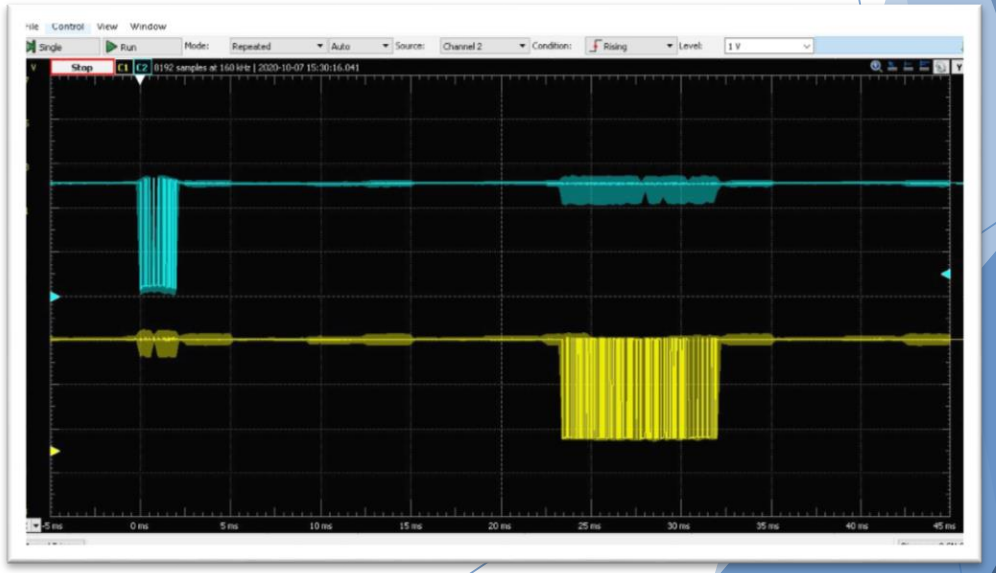


Modulator Output(75 % input)



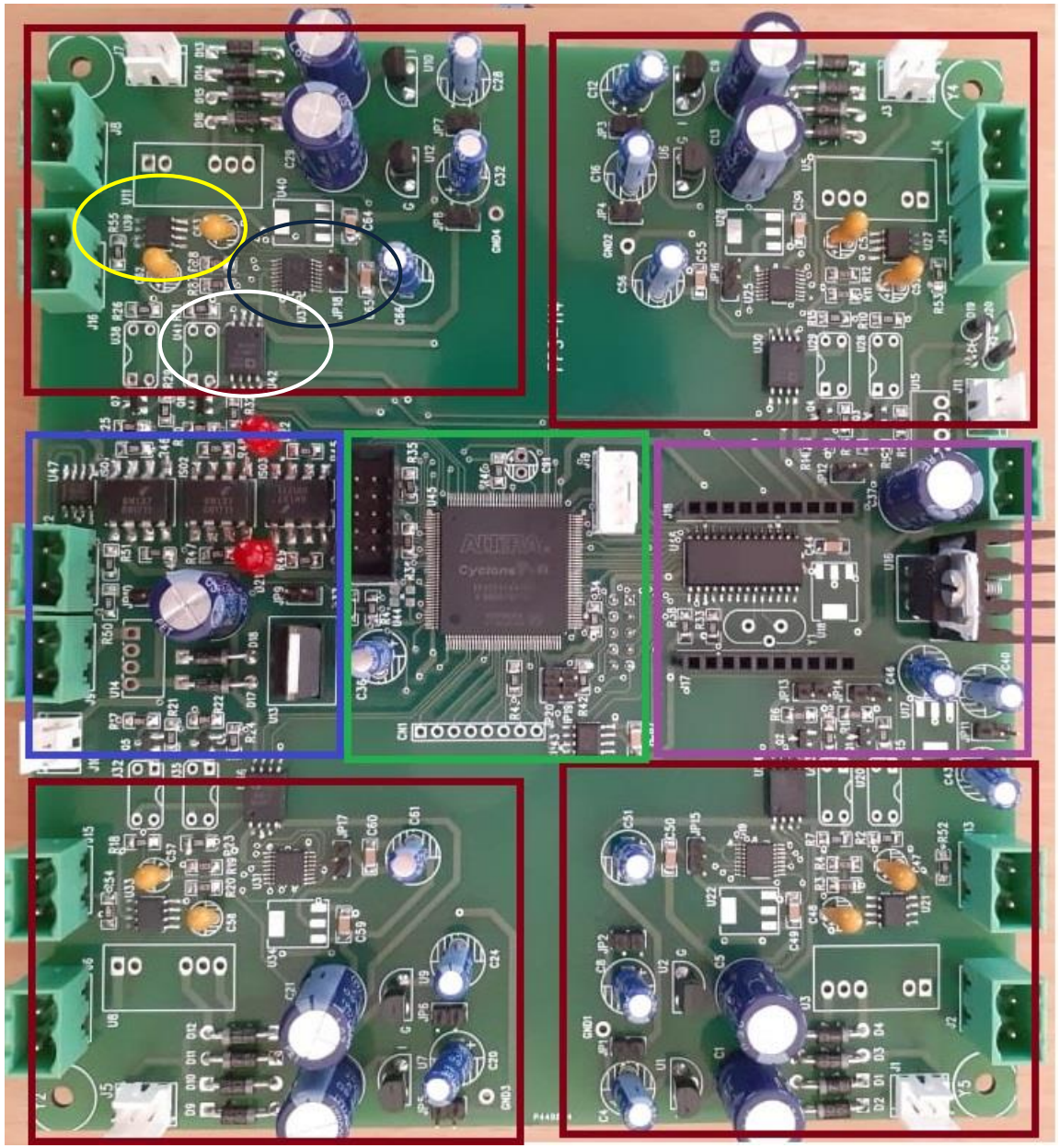
ADC Sample Done Signal(Each 40 ms)

ADC Read Cycle (DATA = BF EB for 75% input)



MODBUS response

Board Layout:



Analog Input Stage

RS-485 circuit

External Processor

FPGA

Active AAF

PGA

Σ-Δ Modulator