The University of Texas at Dallas
Dept. of Electrical Engineering
EECT 6326: Analog IC Design
Final Project

Design of an Operational Amplifier

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1. Introduction

A differential amplifier is an electronic device that amplifies the difference between two input voltages fed to its input terminals while rejecting any noise. It is one of the most common circuits and can be found in a lot of designs. It has various types and different topologies which can be exploited according to the need.

The main aim of this project is to implement the concepts and techniques learnt in class to design a single stage amplifier with differential inputs and single ended output. The design is first done on paper to know the respective currents, voltages and the (W/L) ratios of all the transistors, according to the given specifications. Then, the design is implemented in Cadence software using the 0.35um technology and simulated to check the required specifications and see if they can be achieved as per the given information. In this report, graphs are presented along with the circuits used to calculate the respective parameters. Equations and calculations are also presented wherever required.

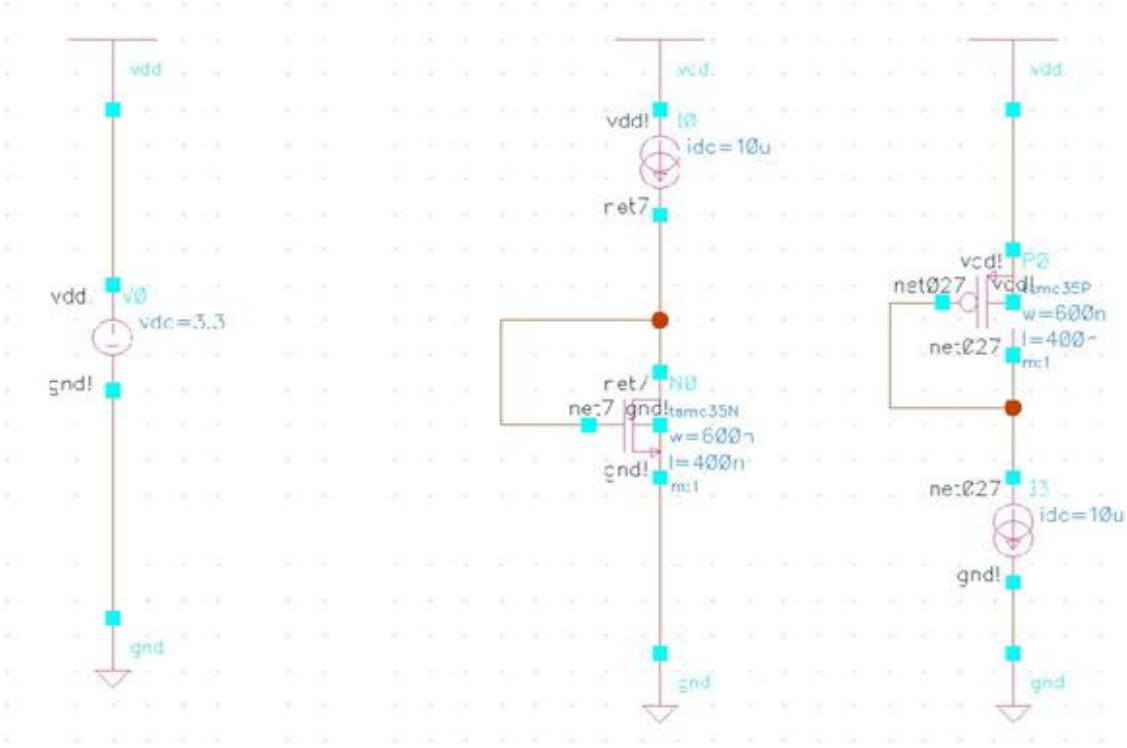
2. Design Specifications

Design a differential-input single-ended output Single-Stage amplifier. The amplifier is to be powered from a 2-V power supply. The amplifier should only have ONE ideal current source. Use CMOS 0.35 µm technology given in this course or other relevant 0.35 µm CMOS to best meet the following specifications:

Parameter	Value
Differential Voltage Gain	>= 65 dB
Output Voltage Swing Range	>= 1.3 V
Average Slew Rate	10 V/µA
Common Mode Rejection Ration	>= 80 dB
Unity-Gain BW	>= 8 MHz
Phase Margin	>= 60°
Power Dissipation	<= 0.5 mW
Capacitive Load	3 pF

3. Essential Parameters Extraction

For essential parameters like $V_{th,}$ µnCox and µpCox, the following configuration was used. The circuit below was simulated in the Cadence software to know the above-mentioned values for the nmos4 and pmos4 devices.



The results obtained are:

- V_{thn} = -756.8 mV
- V_{thp} = 497 mV
- µnCox = 210.8 µ
- µpCox = 70.98 µ

4. Design Procedure

The design was carried out on paper initially to determine the (W/L) ratios of all the transistors, before implementing them in the software. Following points were followed to obtain the specific parameters:

- A high gain of >= 85 dB cannot be obtained using simple common source/common gate or current mirror amplifier. Hence, folded cascode amplifier was chosen.

- A cascode amplifier has a high gain, moderately high input impedance, a high output impedance, and a high bandwidth.

- The I_B was calculated using the values of Slew Rate and capacitance given in the circuit:

  $$SR = I_B/C_L$$

  The value of I_B was found to be 30 µA.

- Gain Calculation:

  $$Gain = g_m \times R_{out}$$

  $$R_{out} = R_p \,||\, R_n$$

- Unity gain frequency:

  $$UGF = g_m/C_L$$

- The ICMR used was 0.8 V to 1.5V

- Then the respective (W/L) values were found out and implemented in the software.

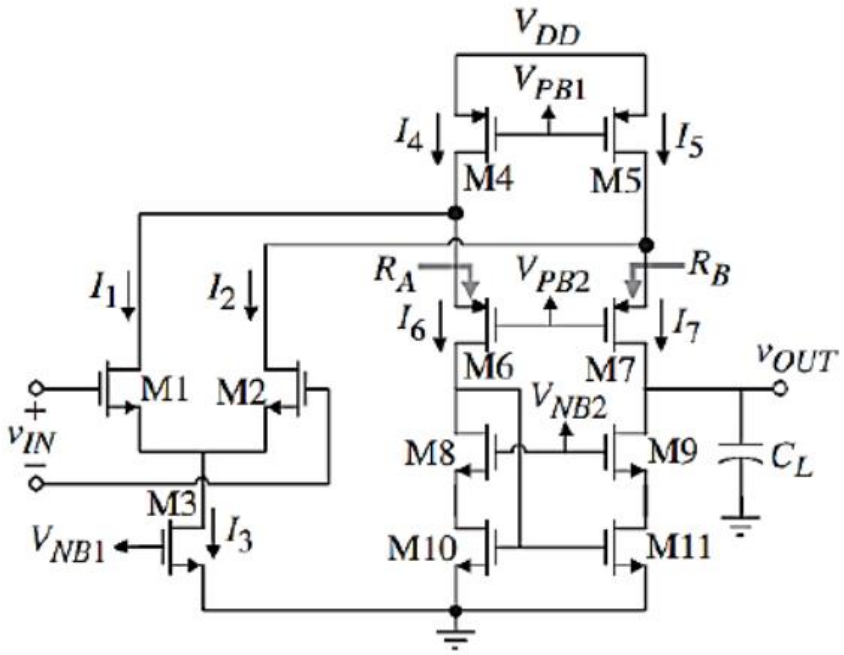


Figure: Basic Folded Cascode Amplifier

5. Schematic and Symbol Views

The following schematic (biasing included) and symbol views were obtained from the Cadence software. Following points can be noted:

- All the MOSFETs can be seen in saturation region (region 2) in the schematic.
- The symbol describes the pins of VDD, GND, INP, INN, OUT, as required.
- The I_B was taken as 30 µA as per the calculations.
- The voltage offset was found to be -172.6 µV (will be utilized later).

(i) Schematic

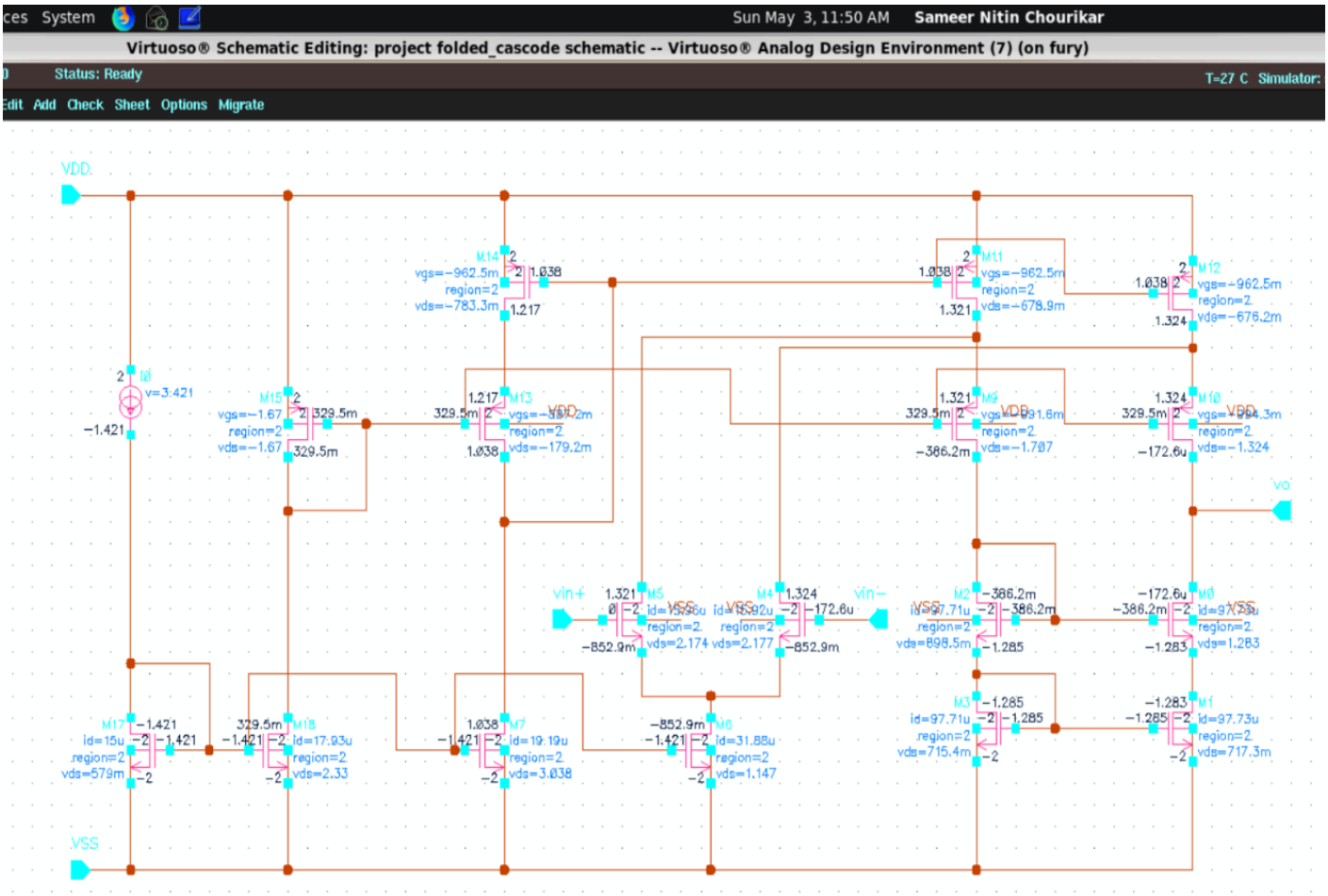


Figure: Schematic of the Folded Cascode Amplifier

(ii) Symbol

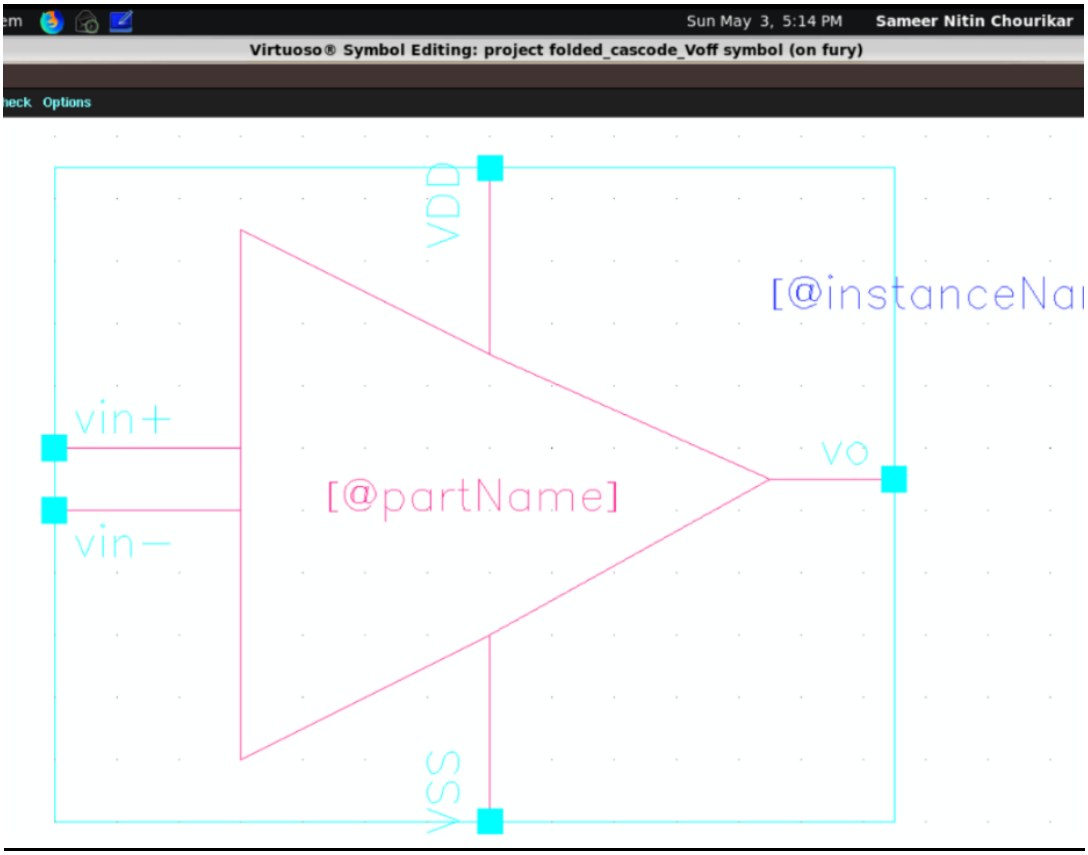


Figure: Symbol of the Amplifier

6. Component Design Parameters

The following (W/L) values were calculated. All the values are in S.I. units: Meter for width and length, Farad for capacitor and Ampere for current (in current source).

Component	(W/L) Value (μm)
M0 (Output v_o)	110/1
M1	40/1
M2	40/1
M3	40/1
M4 (input v_{in}+)	50/1
M5 (input v_{in}-)	50/1
M6 (Base)	80/1
M7 (Bias)	40/1
M9	90/1
M10 (Output v_o)	100/1
M11	50/1
M12	50/1
M13(Bias)	90/1
M14(Bias)	10/1
M15(Bias)	1/1
M17 (Bias)	40/1
M18 (Bias)	40/1
C_0 (Capacitor)	3 pF
I_0 (Current Source)	15 μA

7. Simulation Results: Gain and Unity-Gain BW

The differential voltage gain was found out using the 'Analog Environment' feature of the Cadence software. The circuit was connected in the following manner:

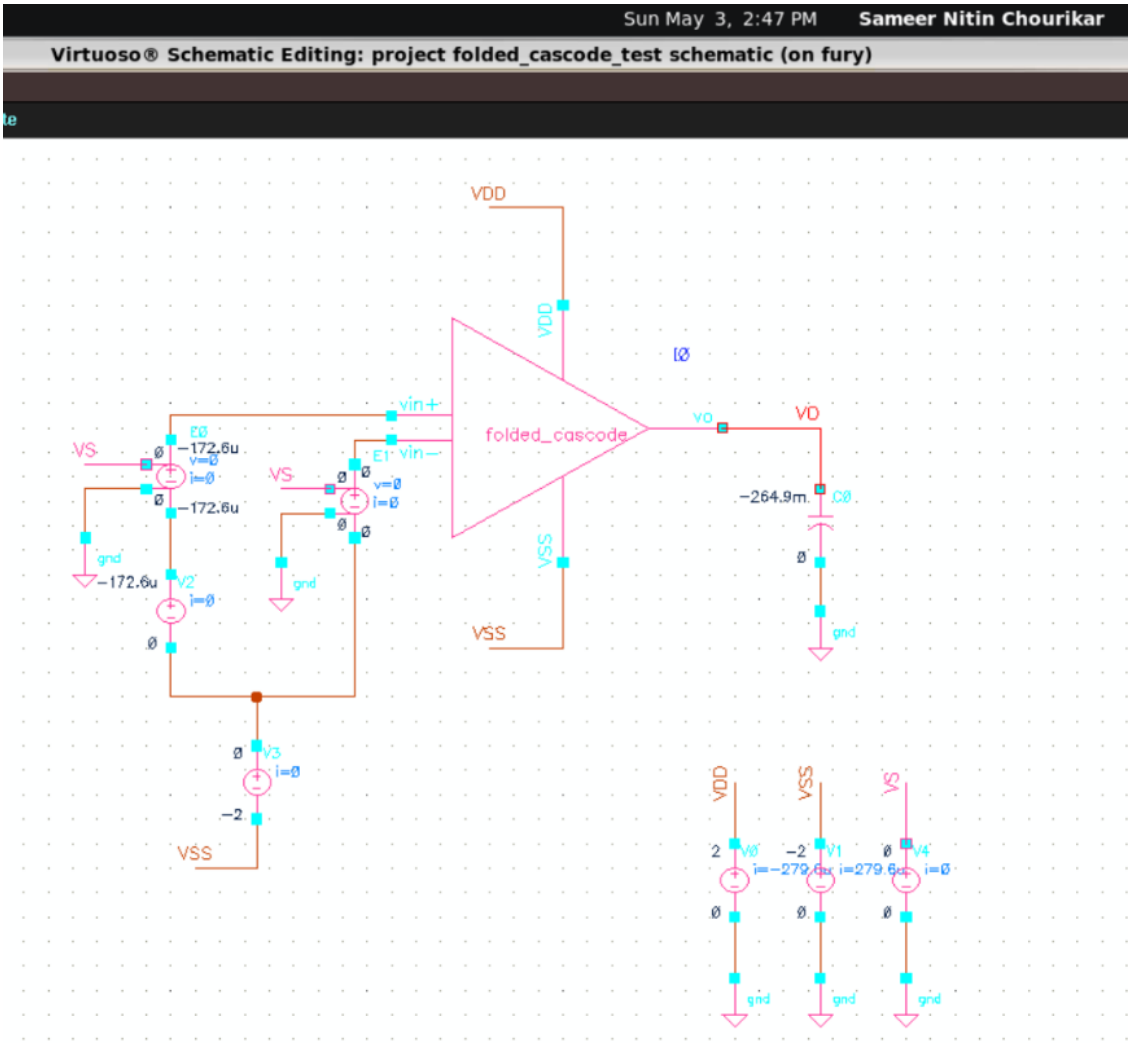


Figure: Circuit for Gain and UGF calculation

- A variable voltage source was connected between the positive and negative terminals of the OPAMP, with an AC magnitude of 1 V.
- The Capacitor of 3 pF is connected at the output.
- The offset voltage (-172.6 µV) is also connected for better results.
- The AC input frequency is swept from 1 mHz to 1GHz and the results are plotted.
- The Gain was found to be 67 dB, with a UGF of 14.106 MHz.

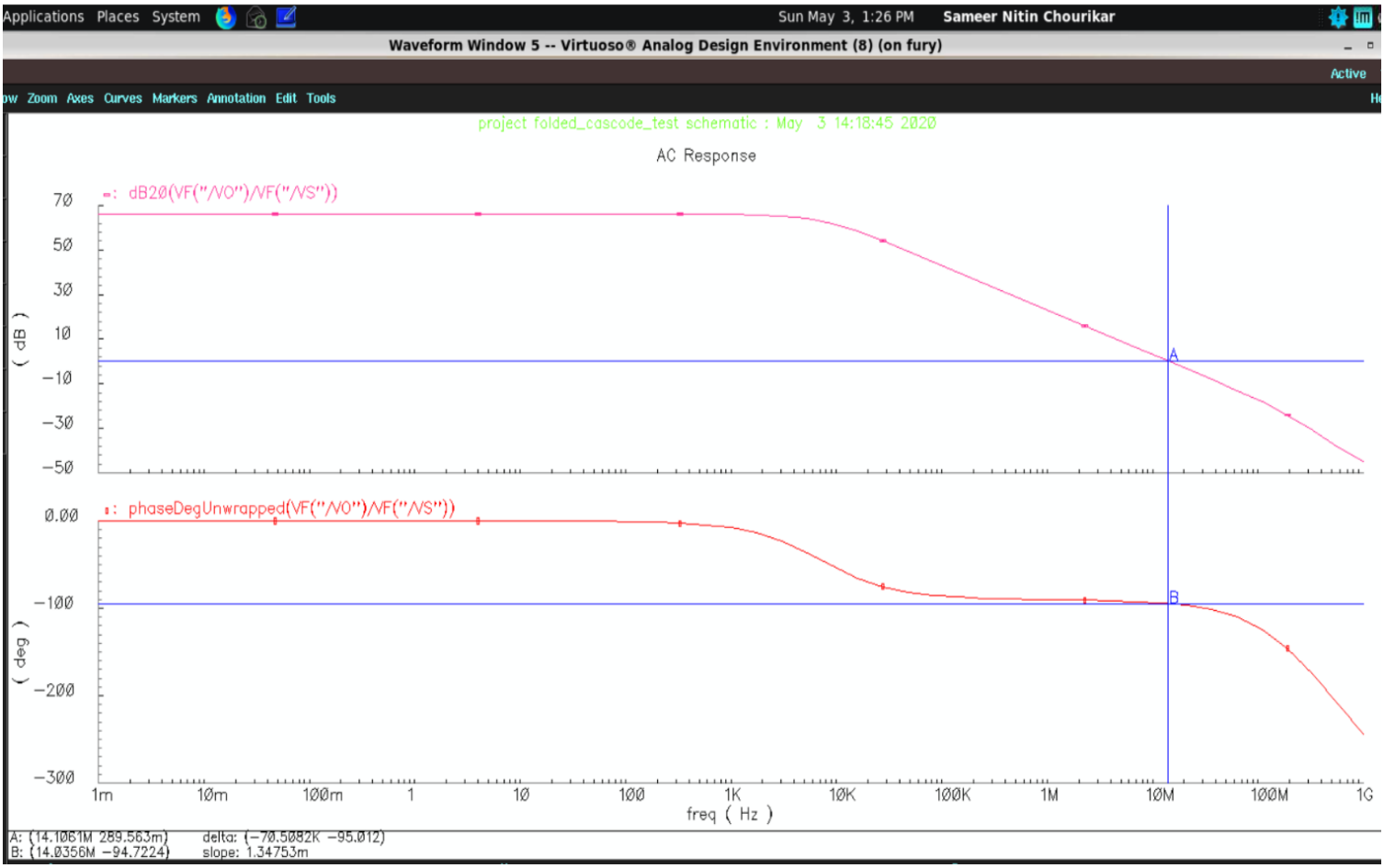


Figure: Gain and Unity-Gain Bandwidth

8. Simulation Results: Output Voltage Swing

The OVSR was found out using the following connection of the OPAMP.

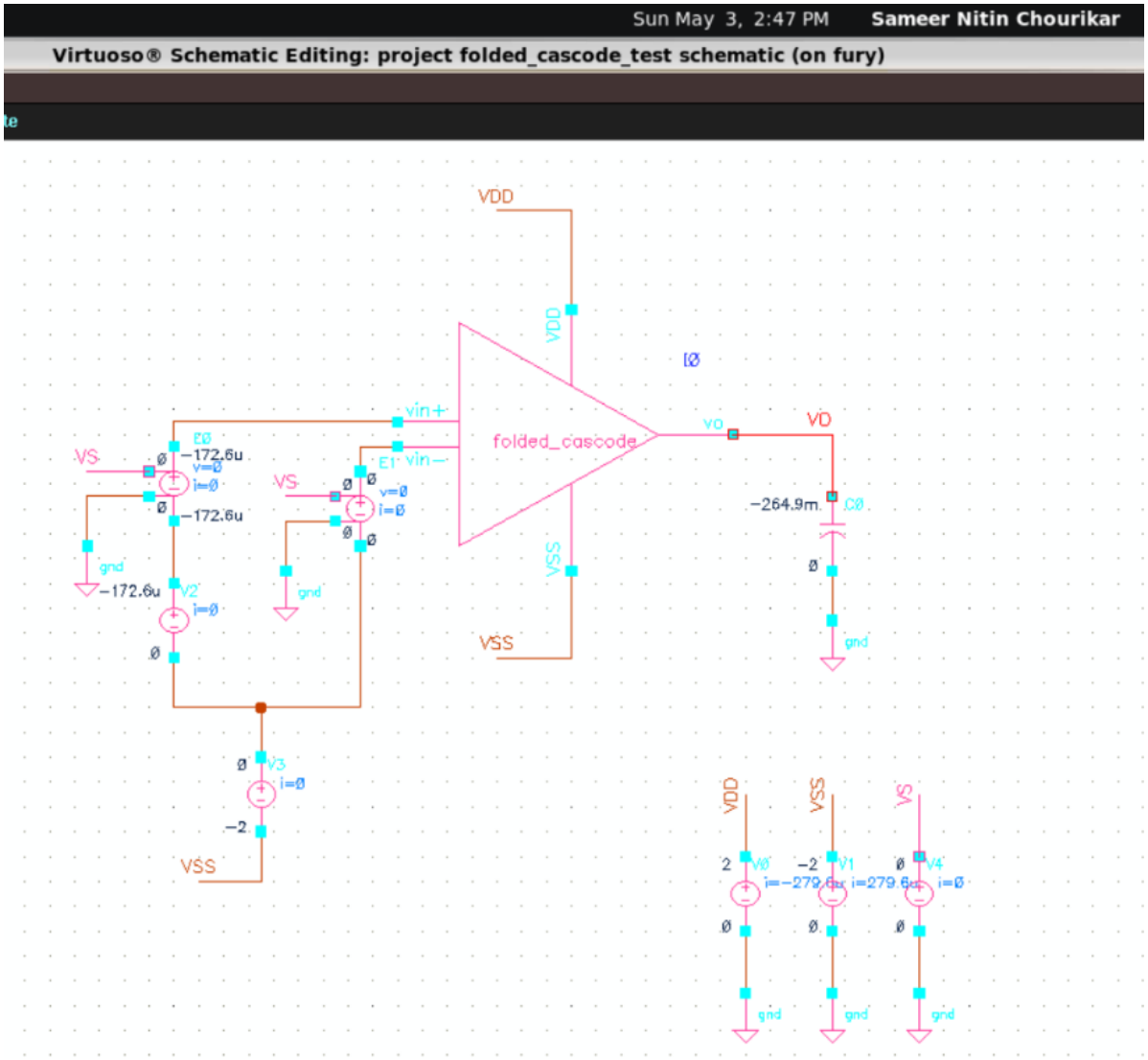


Figure: Circuit for Output Voltage Swing Simulation

- For OVSR, the above circuit is simulated in 'Analog Environment' feature of the Cadence Software.
- A DC sweep from -100 mV to +100 mV was performed on the circuit.
- Two 'Voltage Controlled Voltage Sources' were used at the input.
- The DC voltage was set as: VDD = 2 V and VSS = -2 V in this circuit.
- The Capacitor of 3 pF is connected at the output.
- The OVSR was found to be 3.6814 V.

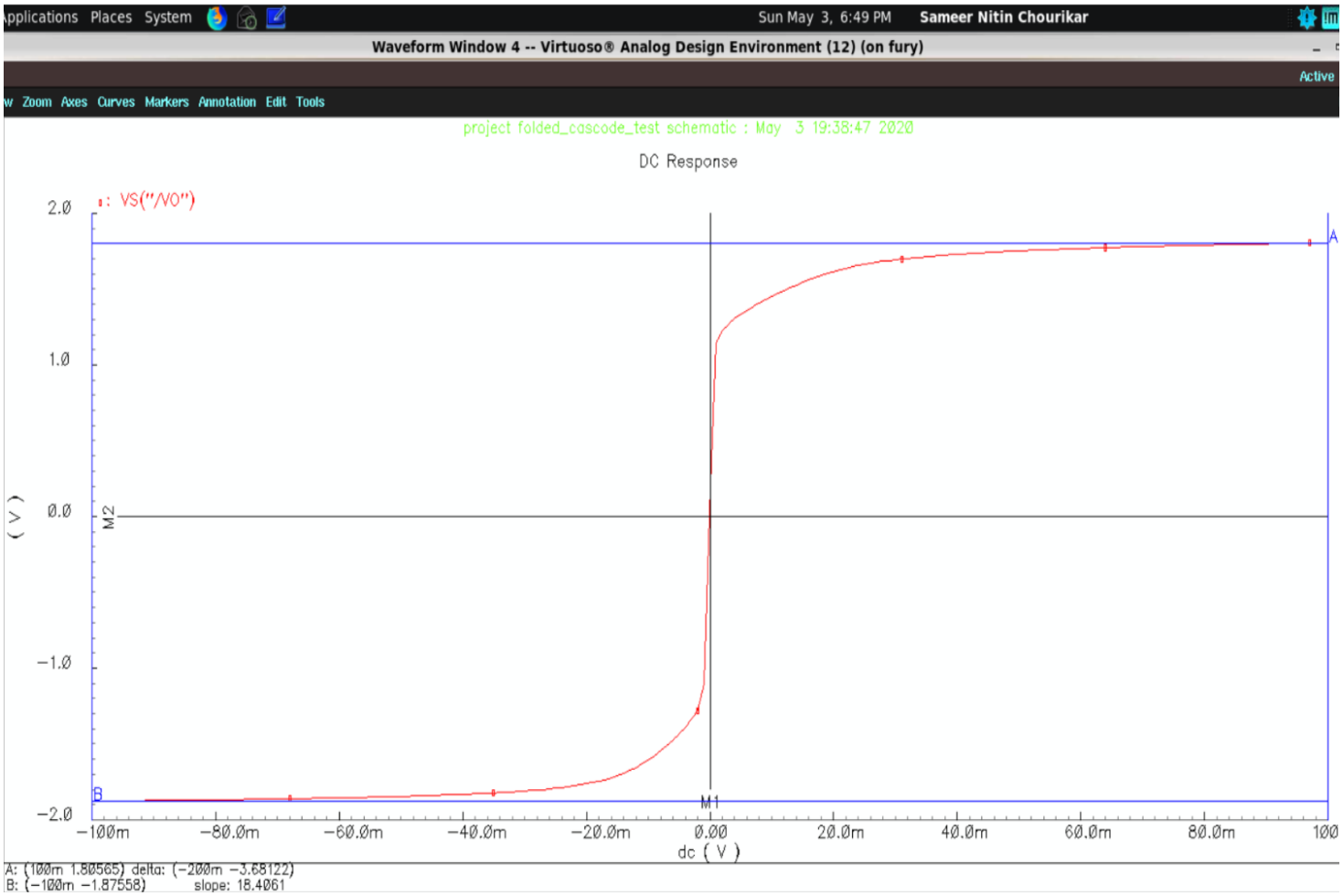


Figure: Response for Output Voltage Swing

OVSR = $(V_o+) – (V_o-)$

= 1.8056 – (-1.8758)

= 3.6814 V

9. Simulation Results: Average Slew-Rate

The Slew rate is the measure of rate of change of voltage with respect to time. The SR- and SR+ are averaged to get the SR of the design. The following circuit is used:

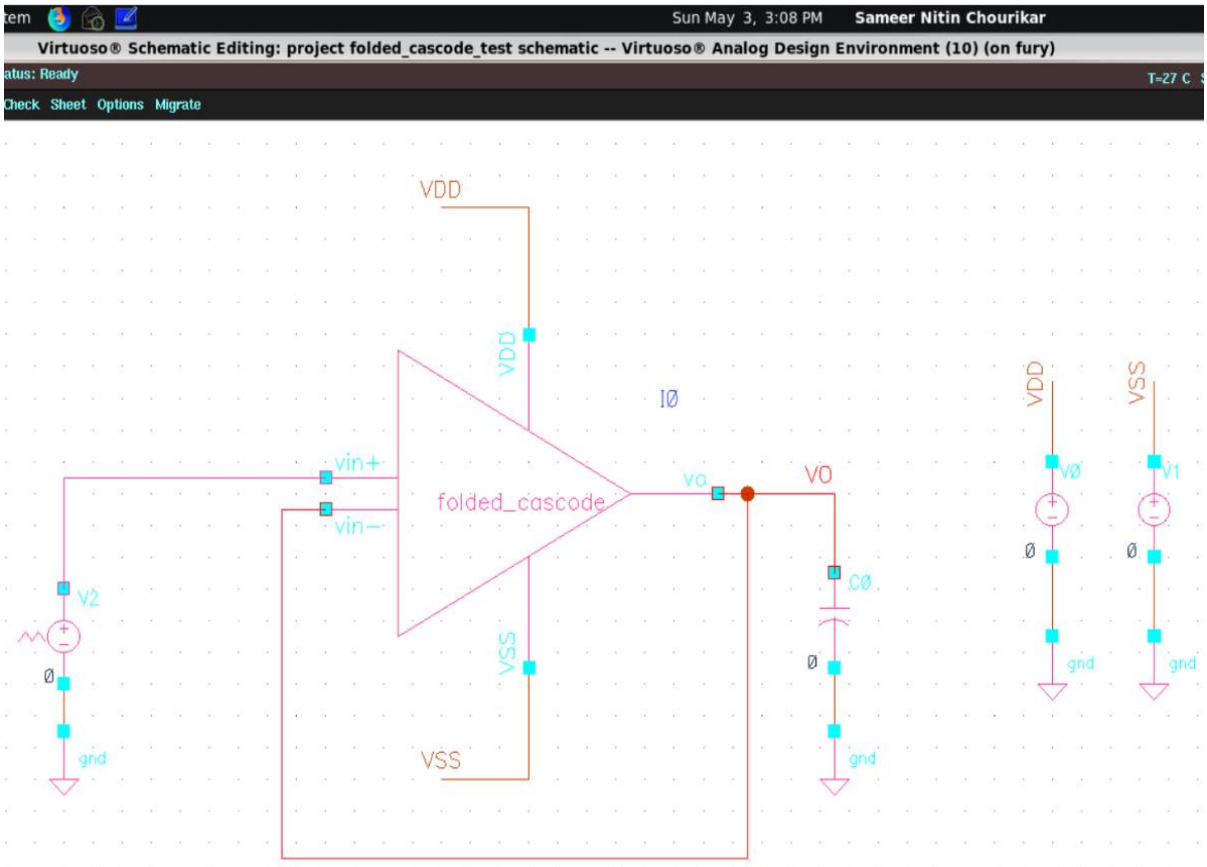


Figure: Circuit for Slew-Rate simulation

- The ‘Analog Environment’ feature has a separate provision for simulation of transient response
- The input is given as a step voltage of 500 mV, which lasts for 500 ns.
- Output is connected to the input and checked how it follows the input.
- The SR+ was calculated on the rising edge of the output waveform.
- Similarly, the SR- was calculated on the falling edge.
- Stop time provided was 1 µs.
- The average SR was found to be 10.379 V/µA.

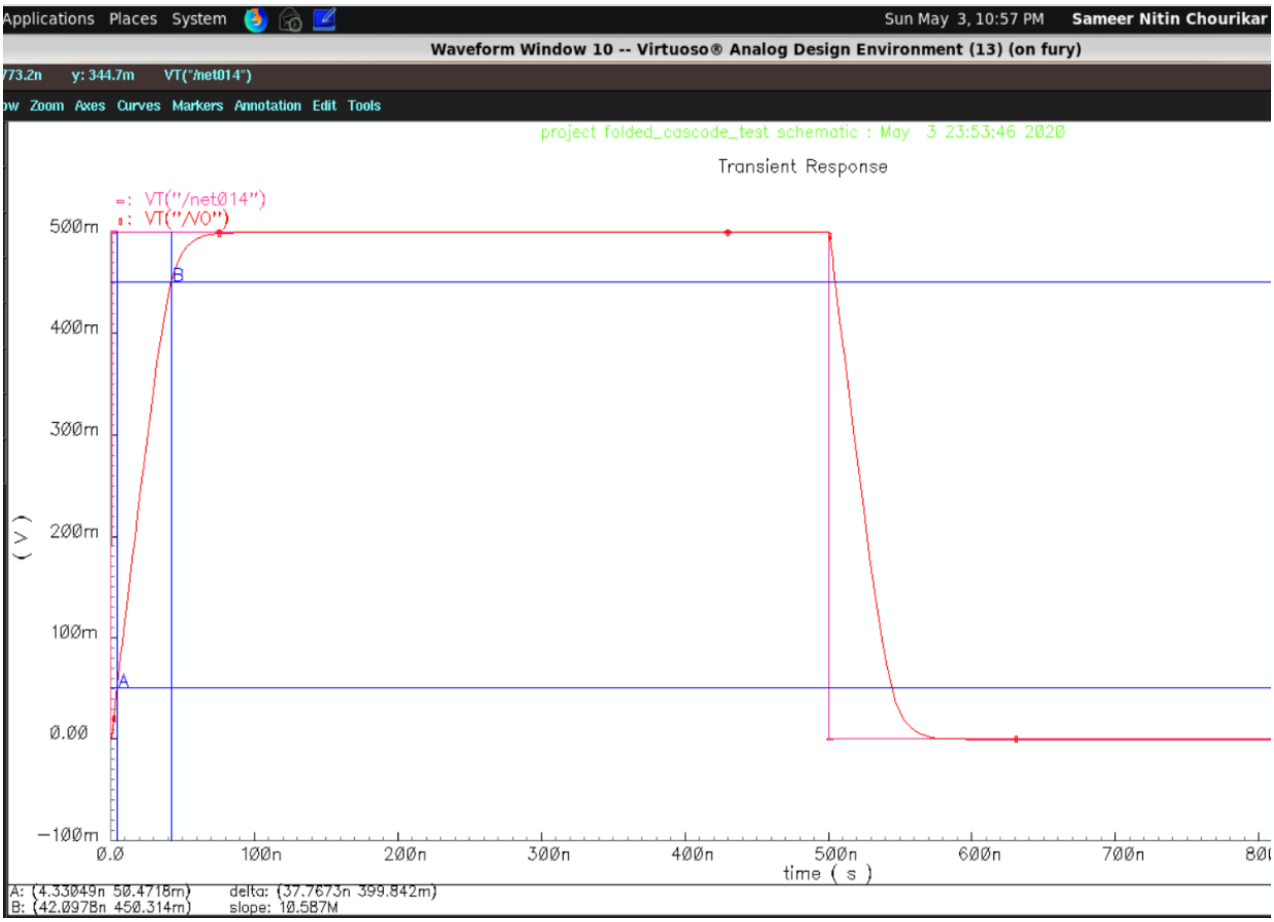


Figure: Waveform for SR+

SR+ = (450.314 – 50.4716) / (42.0978 – 4.3304)

= 10.586 V/µA

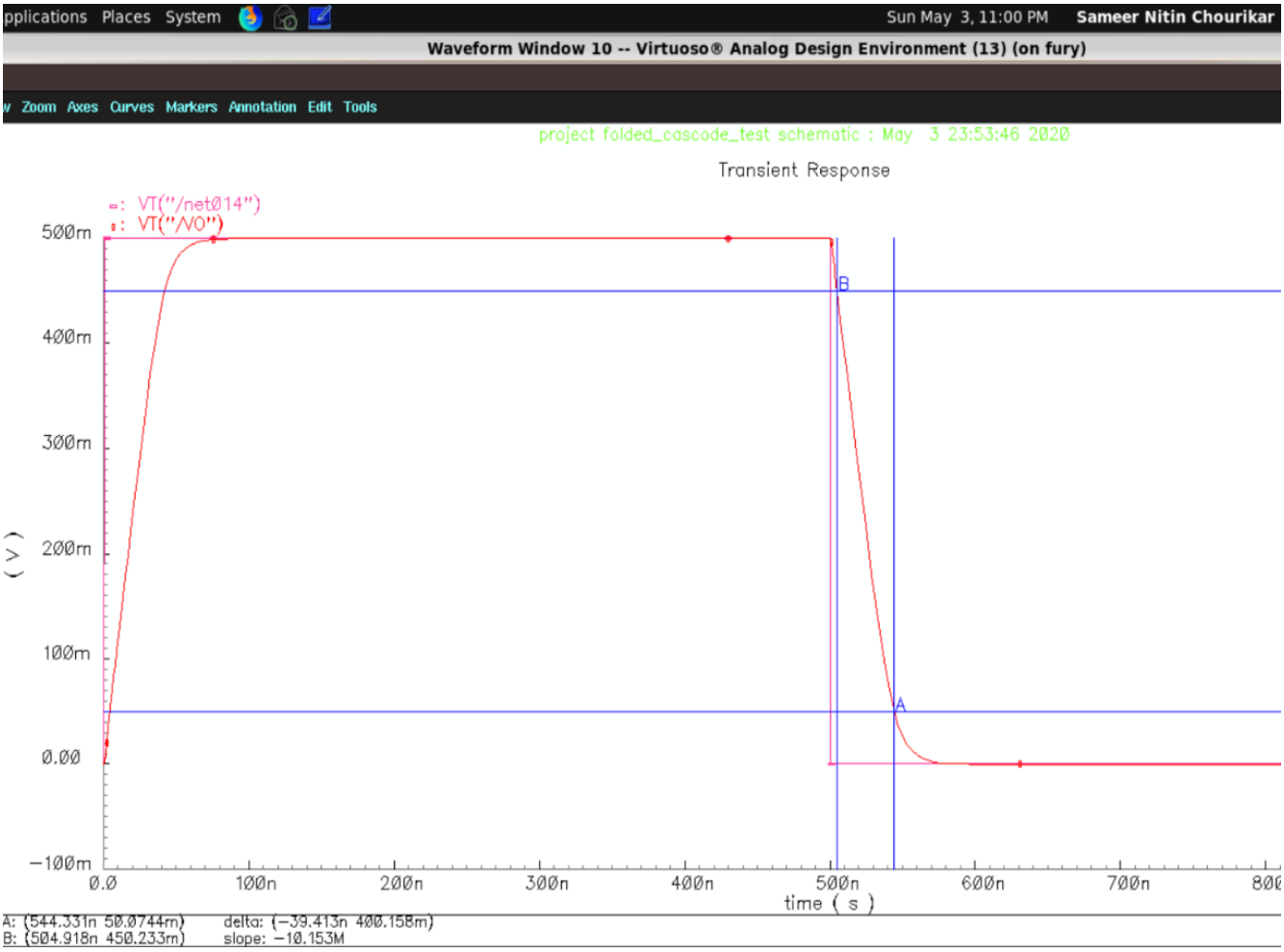


Figure: Waveform for SR-

SR+ = (450.233 – 50.0744) / (544.331 – 504.918)

= 10.152 V/µA

Average Slew-Rate = {(SR+) + (SR-)}/2

= (10.586 + 10.152)/2

= 10.369 V/µA

10. Simulation Results: CMRR

The following circuit was simulated to obtain the Common Mode Gain of the amplifier. As both, the DC gain and the Common Mode Gain, are in dB, they can be subtracted to find the value of CMRR.

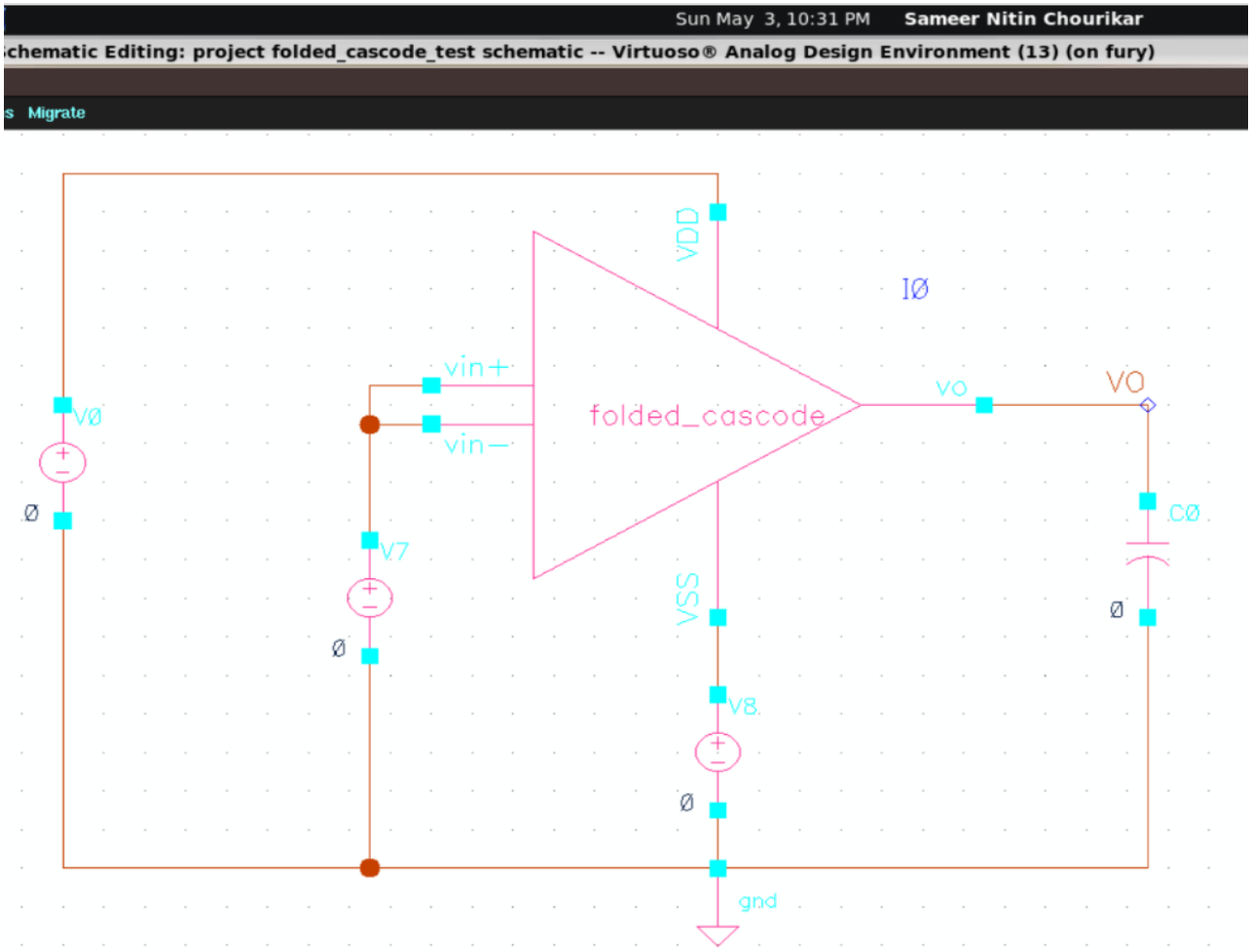


Figure: Circuit to calculate the Common Mode Gain

- A common mode signal of 1 V is applied to both the inputs.
- The capacitor is attached to the output.
- The VDD is 2 V and the VSS is -2 V.
- A Common Mode Gain of -37 dB was acquired.
- The CMRR is found to be 104 dB.

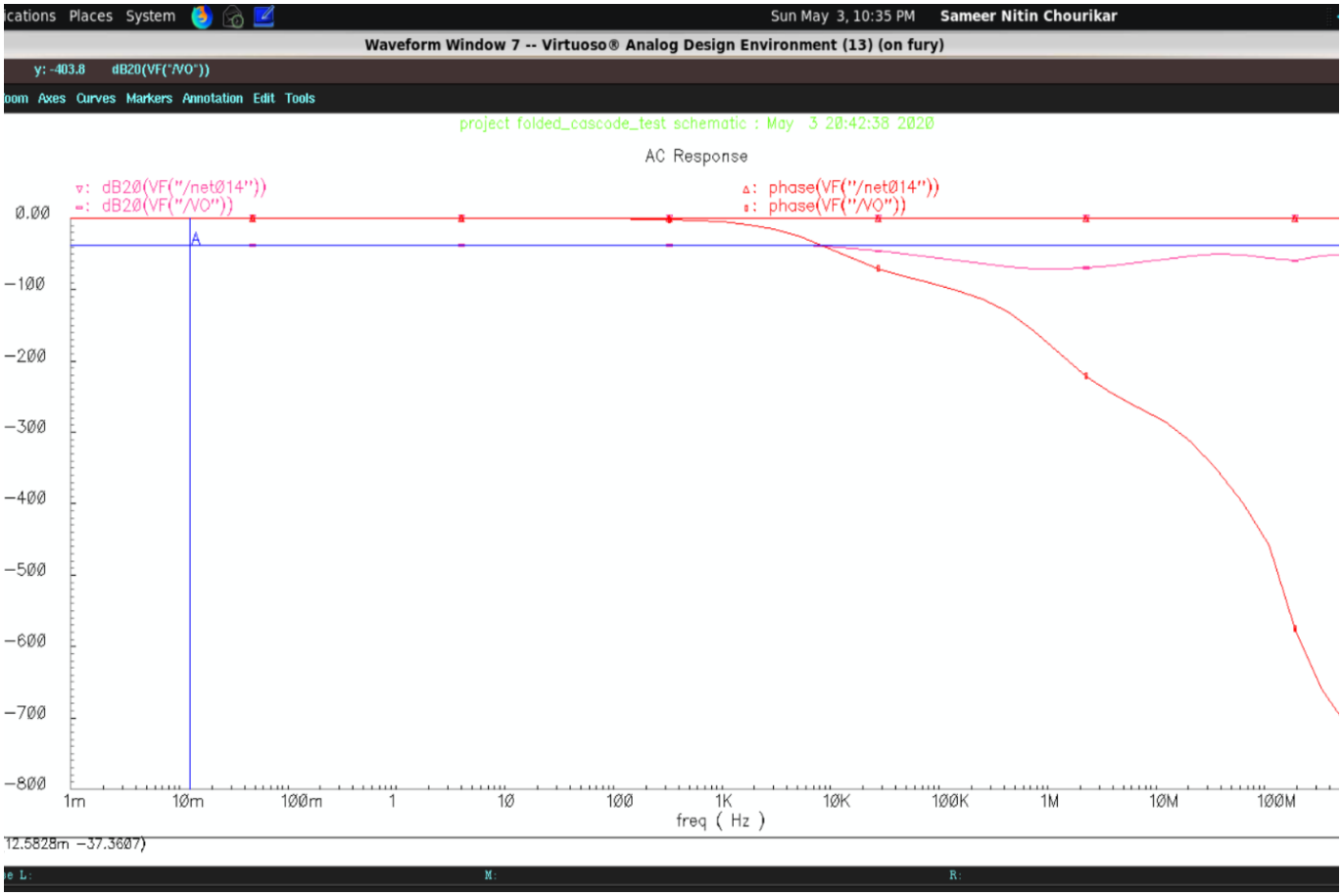


Figure: Response for Common Mode Gain

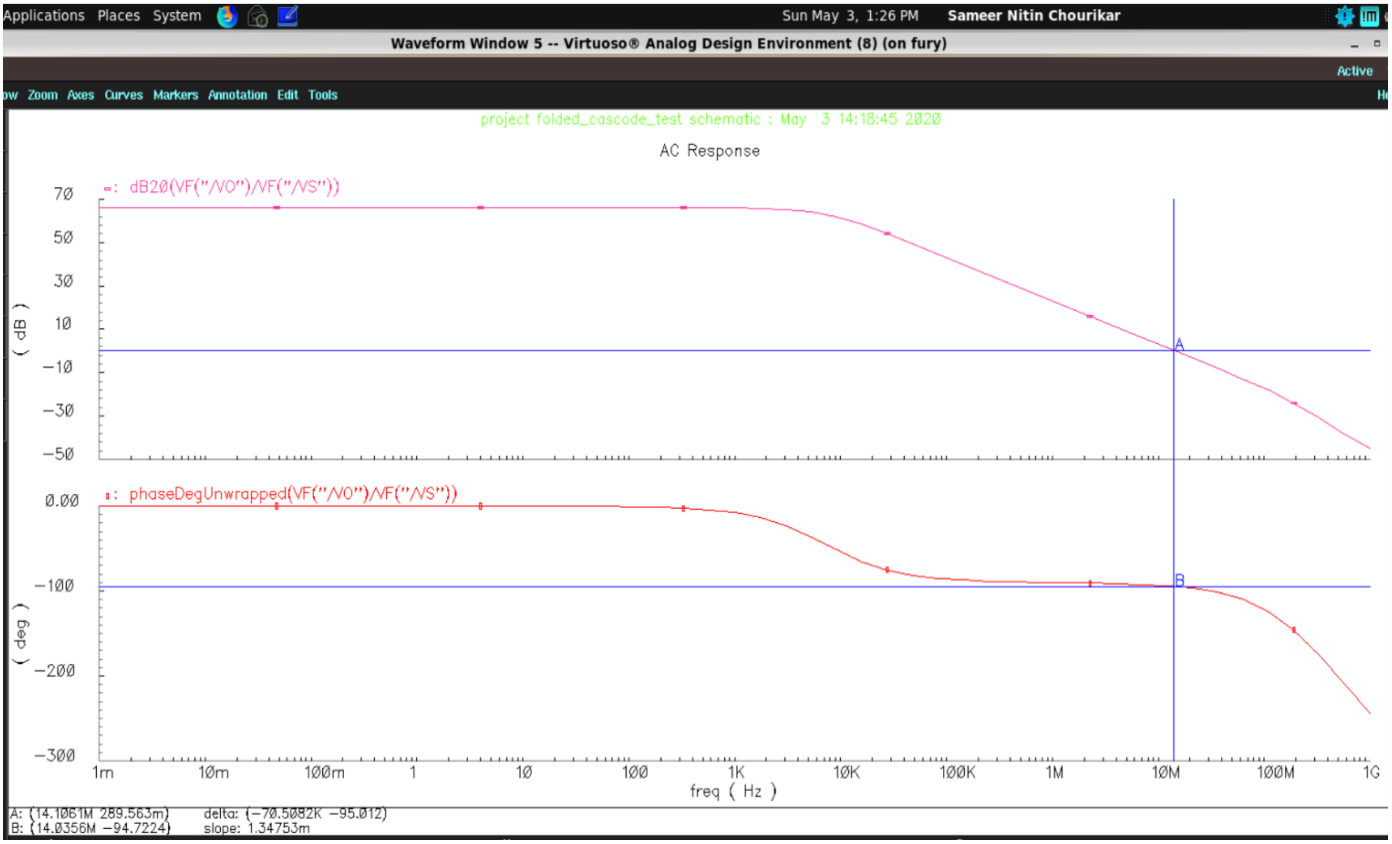
CMRR = DC Gain (dB) – Common Mode Gain (dB)

= 67 – (-37)

= 104 dB

11. Simulation Results: Phase Margin

The Phase Margin can be calculated using the same circuit setup as that of DC gain. The phase margin can be read from the phase plot of the response. The following response is used to determine the phase margin:



The Phase Margin is given by:

PM = 180 – 94.722

= 85.278°

Simulation Results: Power Dissipation

The power dissipation in the circuit can be calculated using the total current utilized multiplied with the voltage at VDD.

The total current utilized is 279.4 µA. The VDD = 2 V.

Hence, Power Dissipation = 279.4 µA x 2 V

= 0.55 mW

12. Results

Specification	Required	Obtained
Gain	>= 65 dB	67 dB
OVSR	>= 1.3 V	3.68 V
SR	>= 10 V/µA	10.369 V/µA
CMRR	>= 80 dB	104 dB
GBW	>= 8 MHz	14 MHz
PM	>= 60°	85.27°
P_{Diss}	<= 0.5 mW	0.55 mW

14. Conclusion

Designing a single stage amplifier with such a high gain was a challenge. I was able to achieve all the requirements according to the specifications. The biggest challenge was posed by the (W/L) ratios of the transistors. Most of the time was utilized in finding the same. Also, after putting those values in the software, other issues such as low voltage across the transistor started to show up. The tuning of the circuit was carried out to see if the 'sweet-spots' could be achieved, where the trade-off between the involved parameters give an optimum solution.

The tradeoff between gain, phase margin and unity-gain bandwidth were studied and implemented to best of my abilities. I learnt a lot about the subtleties of analog design by actually designing an amplifier, rather than just drawing the circuits on paper. I also understood what intricacies a design engineer must go through in order to achieve the requirements. This project and the Analog IC Design course will help me a lot in the VLSI industry in interviews and jobs alike.

References

- Lecture notes of EECT 6326: Analog IC Design course for Spring 2020
- Design of Analog CMOS Integrated Circuits, by Behzad Razavi, McGraw-Hill, 2001.