

# The University of Texas at Dallas

Dept of Electrical Engineering

EECT 6325: VLSI Design

Project 2

## DESIGN AND ANALYSIS OF 16-BIT ALU USING RAM

Done by:

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# **BEHAVIOURAL CODE**

```
`timescale 1ns / 1ps
/////////////////////////////////////////////////////////////////
// Company:
// Engineer:
//
// Create Date: 13:38:37 09/16/2019
// Design Name:
// Module Name: alu
// Project Name:
// Target Devices:
// Tool versions:
// Description:
//
// Dependencies:
//
// Revision:
// Revision 0.01 - File Created
// Additional Comments:
//
/////////////////////////////////////////////////////////////////
module alu( input [15:0] a, input [15:0] b, output reg [15:0] out, input [3:0] fun, input [15:0] cin,
            input write_req,input read_req, input clk, input [15:0] data_in, input [3:0]addr, input rst,
            output reg [15:0] data_out
            );

    reg [15:0] ram [0:15];
    parameter A = 4'b0000; //parameter initialization
    parameter B = 4'b0001;
    parameter C = 4'b0010;
    parameter D = 4'b0011;
    parameter E = 4'b0100;
    parameter F = 4'b0101;
    parameter G = 4'b0110;
    parameter H = 4'b0111;
    parameter I = 4'b1000;
    parameter J = 4'b1001;
    parameter K = 4'b1010;
    parameter L = 4'b1011;
    parameter M = 4'b1100;
    parameter N = 4'b1101;
    parameter O = 4'b1110;
    parameter P = 4'b1111;

    always @ (fun or a or b or cin)
    begin
        case (fun)
            A : out = a + b + cin;
            B : out = a - b;
            C : out = a * b;
            D : out = a / b;
            E : out = a % b;
            F : out = a & b;
            G : out = a | b;
```

```

        H : out = ~(a | b);
        I : out = ~(a & b);
        J : out = a ^ b;
        K : out = ~(a ^ b);
        L : out = a<<1;
        M : out = a>>1;
        N : out = b<<1;
        O : out = b>>1;
        P : out = ~(a);
    endcase
end
/*
always @ (posedge clk)
begin
    if (rst == 1)
    begin
        data_out <= 0;
    end
end
*/
always @ (posedge clk)
begin
    if (write_req == 1)        //If data is available to write,
    begin
        ram [addr] <= data_in;    //Data is written in the RAM at the current location of address
    end
end

always @ (posedge clk)
begin
    if (read_req == 1)        //If data is available to read,
    begin
        data_out <= ram [addr];    //Data is read from the RAM according to the location of the address
    end
end
end
endmodule

```

# TESTBENCH CODE:

```
`timescale 1ns / 1ps
```

```
//////////////////////////////////////////////////////////////////  
// Company:  
// Engineer:  
//  
// Create Date: 15:07:25 09/16/2019  
// Design Name: alu  
// Module Name: /home/eng/v/vxa190000/Desktop/alu/alu_tb.v  
// Project Name: alu  
// Target Device:  
// Tool versions:  
// Description:  
//  
// Verilog Test Fixture created by ISE for module: alu  
//  
// Dependencies:  
//  
// Revision:  
// Revision 0.01 - File Created  
// Additional Comments:  
//  
//////////////////////////////////////////////////////////////////
```

```
module alu_tb;
```

```
    // Inputs  
    reg [15:0] a;  
    reg [15:0] b;  
    reg [3:0] fun;  
    reg [15:0] cin;  
    reg write_req;  
    reg read_req;  
    reg clk;  
    reg [15:0] data_in;  
    reg [3:0] addr;
```

```
    // Outputs  
    wire [15:0] out;  
    wire [7:0] data_out;
```

```
    // Instantiate the Unit Under Test (UUT)  
    alu uut (
```

```
        .a(a),  
        .b(b),  
        .out(out),  
        .fun(fun),  
        .cin(cin),  
        .write_req(write_req),  
        .read_req(read_req),  
        .clk(clk),  
        .data_in(data_in),  
        .data_out(data_out),  
        .addr(addr)
```

```
    );
```

```

initial begin
    // Initialize Inputs
    a = 0;
    b = 0;
    fun = 0;
    cin = 0;
    write_req = 0;    //Initializing all the inputs to zero
    read_req = 0;
    clk = 0;
    data_in = 0;
    //data_out = 0;
    addr = 0;

    // Wait 100 ns for global reset to finish
    #100;

    // Add stimulus here

end
integer i;
initial begin
    forever begin

        #50 clk = ~clk;    //Clock generation
    end
end

```

```

initial begin

    a = 20'b11110000;
    b = 20'b00001111;
    cin = 20'b00000000;

    #50;
    fun = 0000;
    #20;
    fun = 0001;
    #20;
    fun = 0010;
    #20;
    fun = 0011;
    #20;
    fun = 0100;
    #20;
    fun = 0101;
    #20;
    fun = 0110;
    #20;
    fun = 0111;
    #20;
    fun = 1000;
    #20;
    fun = 1001;
    #20;
    fun = 1010;
    #20;
    fun = 1011;
    #20;
    fun = 1100;

```

```
#20;  
fun = 1101;  
#20;  
fun = 1110;  
#20;  
fun = 1111;
```

```
for (i = 0; i <=15 ; i = i +1 )
```

```
begin
```

```
addr = i;           //Counter ti go through all the 16 states of the address
```

```
#10;
```

```
end
```

```
$display ("Writing data:");
```

```
write_req = 1;           //Write enable: ON
```

```
a = 8'b00001111;        //Data to be written
```

```
#100;
```

```
read_req = 1;           //Read enable: ON
```

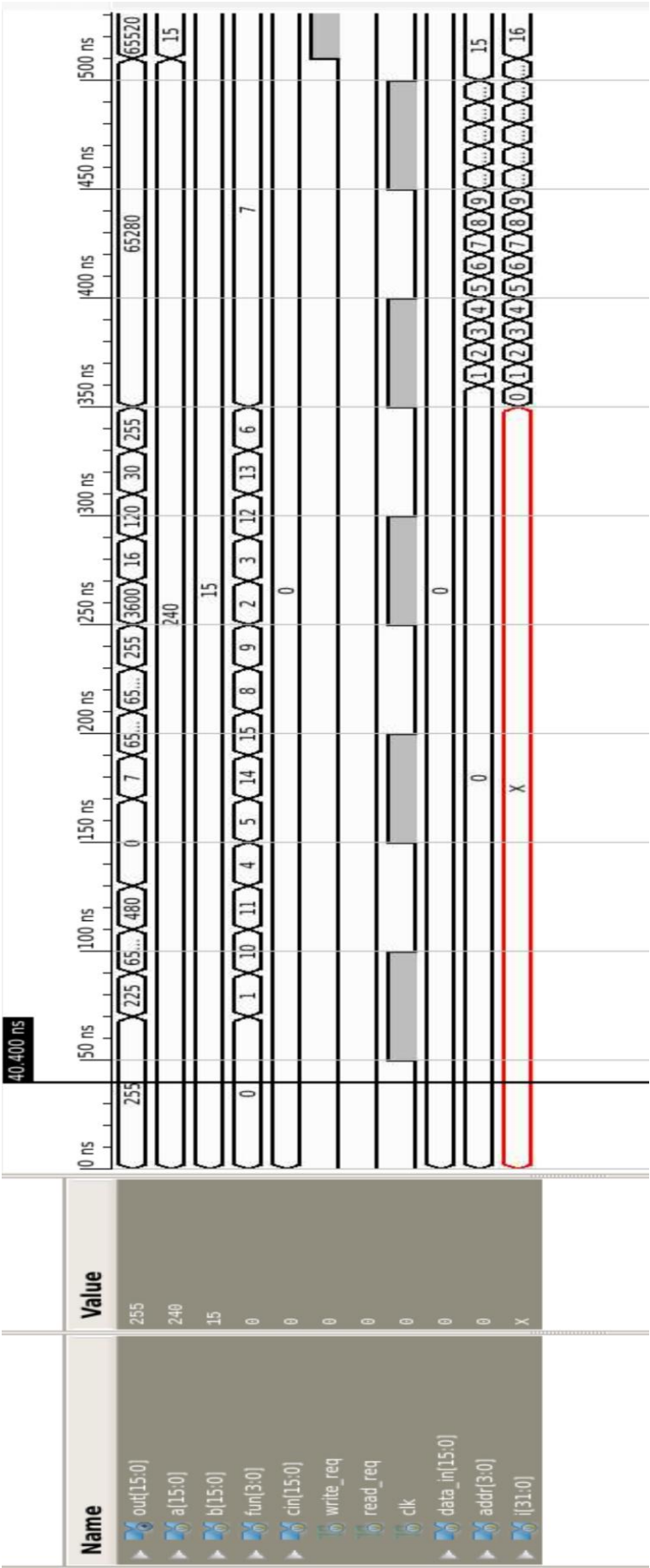
```
$display ("Reading data:",addr,out); //Reading the data currently at the address location in the RAM
```

```
end
```

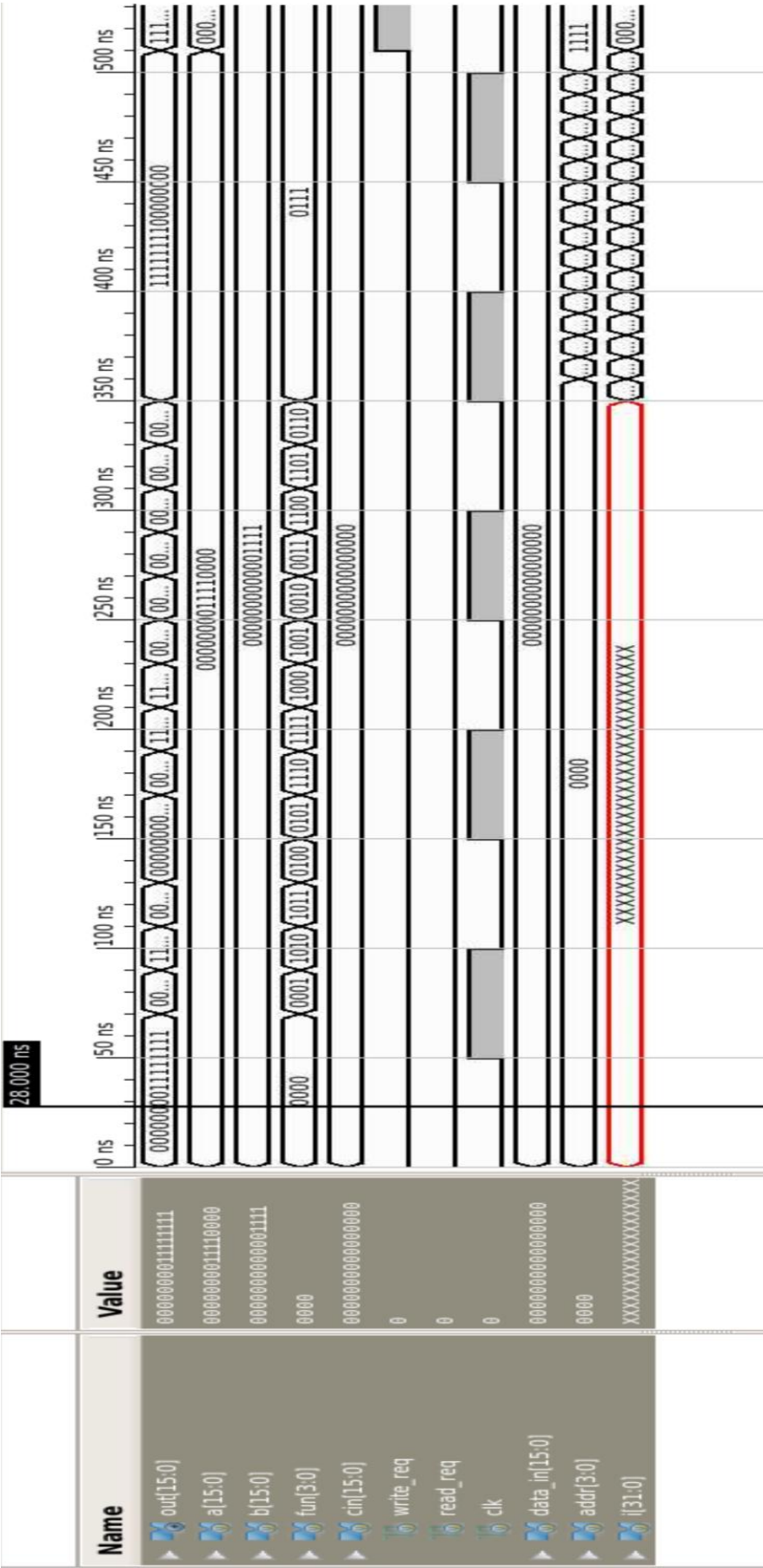
```
endmodule
```

# Output Waveforms:

## 1. BEHAVIOURAL WAVEFORM



2. MAPPED NETLIST WAVEFORM





# CELL REPORT:

\*\*\*\*\*

Report : cell

Design : alu

Version: L-2016.03-SP3

Date : Tue Sep 17 22:07:27 2019

\*\*\*\*\*

## Attributes:

- b - black box (unknown)
- h - hierarchical
- n - noncombinational
- r - removable
- u - contains unmapped logic

Cell	Reference	Library	Area	Attributes
C56	nand2	library	1.000000	
C57	nand2	library	1.000000	
C60	nand2	library	1.000000	
C82	nand2	library	1.000000	
C83	nand2	library	1.000000	
C89	nand2	library	1.000000	
C96	nand2	library	1.000000	
C100	nand2	library	1.000000	
C101	nand2	library	1.000000	
C125	nand2	library	1.000000	
C143	nand2	library	1.000000	
C144	nand2	library	1.000000	
C825	nand2	library	1.000000	
C826	nand2	library	1.000000	
C827	nand2	library	1.000000	
C828	nand2	library	1.000000	
C829	nand2	library	1.000000	
C830	nand2	library	1.000000	
C831	nand2	library	1.000000	
C832	nand2	library	1.000000	
C854	nand2	library	1.000000	
C855	nand2	library	1.000000	
C856	nand2	library	1.000000	
C857	nand2	library	1.000000	
C858	nand2	library	1.000000	
C859	nand2	library	1.000000	
C860	nand2	library	1.000000	
C861	nand2	library	1.000000	
C862	nand2	library	1.000000	
C863	nand2	library	1.000000	
C864	nand2	library	1.000000	
C865	nand2	library	1.000000	
C866	nand2	library	1.000000	
C867	nand2	library	1.000000	
C868	nand2	library	1.000000	
C869	nand2	library	1.000000	
C870	nand2	library	1.000000	
C871	nand2	library	1.000000	
C872	nand2	library	1.000000	
C873	nand2	library	1.000000	
C874	nand2	library	1.000000	
C875	nand2	library	1.000000	
C876	nand2	library	1.000000	

C877	nand2	library	1.000000
C878	nand2	library	1.000000
C879	nand2	library	1.000000
C880	nand2	library	1.000000
C881	nand2	library	1.000000
C882	nand2	library	1.000000
C883	nand2	library	1.000000
C884	nand2	library	1.000000
C885	nand2	library	1.000000
C886	xor2	library	3.000000
C887	xor2	library	3.000000
C888	xor2	library	3.000000
C889	xor2	library	3.000000
C890	xor2	library	3.000000
C891	xor2	library	3.000000
C892	xor2	library	3.000000
C893	xor2	library	3.000000
C894	xor2	library	3.000000
C895	xor2	library	3.000000
C896	xor2	library	3.000000
C897	xor2	library	3.000000
C898	xor2	library	3.000000
C899	xor2	library	3.000000
C900	xor2	library	3.000000
C901	xor2	library	3.000000
I_0	inv	library	1.000000
I_1	inv	library	1.000000
I_2	inv	library	1.000000
I_3	inv	library	1.000000
I_4	inv	library	1.000000
I_5	inv	library	1.000000
I_6	inv	library	1.000000
I_7	inv	library	1.000000
I_8	inv	library	1.000000
I_9	inv	library	1.000000
I_10	inv	library	1.000000
I_11	inv	library	1.000000
I_12	inv	library	1.000000
I_13	inv	library	1.000000
I_14	inv	library	1.000000
I_15	inv	library	1.000000
I_16	inv	library	1.000000
I_17	inv	library	1.000000
I_18	inv	library	1.000000
I_19	inv	library	1.000000
I_20	inv	library	1.000000
I_21	inv	library	1.000000
I_22	inv	library	1.000000
I_23	inv	library	1.000000
I_24	inv	library	1.000000
I_25	inv	library	1.000000
I_74	inv	library	1.000000
I_75	inv	library	1.000000
I_76	inv	library	1.000000
I_77	inv	library	1.000000
I_78	inv	library	1.000000
I_79	inv	library	1.000000
I_80	inv	library	1.000000
I_81	inv	library	1.000000
I_82	inv	library	1.000000
I_83	inv	library	1.000000
I_84	inv	library	1.000000
I_85	inv	library	1.000000
I_86	inv	library	1.000000

I_87	inv	library	1.000000
I_88	inv	library	1.000000
I_89	inv	library	1.000000
U2	oai12	library	2.000000
U3	nand2	library	1.000000
U8	oai12	library	2.000000
U9	nand2	library	1.000000
U10	oai12	library	2.000000
U11	nand2	library	1.000000
U12	oai12	library	2.000000
U13	nand2	library	1.000000
U14	oai12	library	2.000000
U15	nand2	library	1.000000
U16	oai12	library	2.000000
U17	nand2	library	1.000000
U18	oai12	library	2.000000
U19	nand2	library	1.000000
U20	oai12	library	2.000000
U21	nand2	library	1.000000
U22	oai12	library	2.000000
U23	nand2	library	1.000000
U24	oai12	library	2.000000
U25	nand2	library	1.000000
U26	oai12	library	2.000000
U27	nand2	library	1.000000
U28	oai12	library	2.000000
U29	nand2	library	1.000000
U30	oai12	library	2.000000
U31	nand2	library	1.000000
U32	oai12	library	2.000000
U33	nand2	library	1.000000
U34	oai12	library	2.000000
U35	nand2	library	1.000000
U36	oai12	library	2.000000
U37	nand2	library	1.000000
U38	nand2	library	1.000000
U39	oai12	library	2.000000
U40	nand2	library	1.000000
U41	oai12	library	2.000000
U42	nand2	library	1.000000
U43	oai12	library	2.000000
U44	nand2	library	1.000000
U45	oai12	library	2.000000
U46	nand2	library	1.000000
U47	oai12	library	2.000000
U48	nand2	library	1.000000
U49	oai12	library	2.000000
U50	nand2	library	1.000000
U51	oai12	library	2.000000
U52	nand2	library	1.000000
U53	oai12	library	2.000000
U54	nand2	library	1.000000
U55	oai12	library	2.000000
U56	nand2	library	1.000000
U57	oai12	library	2.000000
U58	nand2	library	1.000000
U59	oai12	library	2.000000
U60	nand2	library	1.000000
U61	oai12	library	2.000000
U62	nand2	library	1.000000
U63	oai12	library	2.000000
U64	nand2	library	1.000000
U65	oai12	library	2.000000
U66	nand2	library	1.000000

U67	oai12	library	2.000000
U68	nand2	library	1.000000
U69	oai12	library	2.000000
U70	nand2	library	1.000000
U71	nand2	library	1.000000
U72	oai12	library	2.000000
U73	nand2	library	1.000000
U74	oai12	library	2.000000
U75	nand2	library	1.000000
U76	oai12	library	2.000000
U77	nand2	library	1.000000
U78	oai12	library	2.000000
U79	nand2	library	1.000000
U80	oai12	library	2.000000
U81	nand2	library	1.000000
U82	oai12	library	2.000000
U83	nand2	library	1.000000
U84	oai12	library	2.000000
U85	nand2	library	1.000000
U86	oai12	library	2.000000
U87	nand2	library	1.000000
U88	oai12	library	2.000000
U89	nand2	library	1.000000
U90	oai12	library	2.000000
U91	nand2	library	1.000000
U92	oai12	library	2.000000
U93	nand2	library	1.000000
U94	oai12	library	2.000000
U95	nand2	library	1.000000
U96	oai12	library	2.000000
U97	nand2	library	1.000000
U98	oai12	library	2.000000
U99	nand2	library	1.000000
U100	oai12	library	2.000000
U101	nand2	library	1.000000
U102	oai12	library	2.000000
U103	nand2	library	1.000000
U104	nand2	library	1.000000
U105	oai12	library	2.000000
U106	nand2	library	1.000000
U107	oai12	library	2.000000
U108	nand2	library	1.000000
U109	oai12	library	2.000000
U110	nand2	library	1.000000
U111	oai12	library	2.000000
U112	nand2	library	1.000000
U113	oai12	library	2.000000
U114	nand2	library	1.000000
U115	oai12	library	2.000000
U116	nand2	library	1.000000
U117	oai12	library	2.000000
U118	nand2	library	1.000000
U119	oai12	library	2.000000
U120	nand2	library	1.000000
U121	oai12	library	2.000000
U122	nand2	library	1.000000
U123	oai12	library	2.000000
U124	nand2	library	1.000000
U125	oai12	library	2.000000
U126	nand2	library	1.000000
U127	oai12	library	2.000000
U128	nand2	library	1.000000
U129	oai12	library	2.000000
U130	nand2	library	1.000000

U131	oai12	library	2.000000	
U132	nand2	library	1.000000	
U133	oai12	library	2.000000	
U134	nand2	library	1.000000	
U135	oai12	library	2.000000	
U136	nand2	library	1.000000	
U137	nand2	library	1.000000	
U138	oai12	library	2.000000	
U139	nand2	library	1.000000	
U140	oai12	library	2.000000	
U141	nand2	library	1.000000	
U142	oai12	library	2.000000	
U143	nand2	library	1.000000	
U144	oai12	library	2.000000	
U145	nand2	library	1.000000	
U146	oai12	library	2.000000	
U147	nand2	library	1.000000	
U148	oai12	library	2.000000	
U149	nand2	library	1.000000	
U150	oai12	library	2.000000	
U2881	inv	library	1.000000	
U2882	inv	library	1.000000	
U2883	inv	library	1.000000	
U2884	inv	library	1.000000	
U2885	inv	library	1.000000	
U2886	inv	library	1.000000	
U2887	inv	library	1.000000	
U2888	inv	library	1.000000	
U2889	inv	library	1.000000	
U2890	inv	library	1.000000	
U2891	inv	library	1.000000	
U2892	inv	library	1.000000	
U2893	inv	library	1.000000	
U2894	inv	library	1.000000	
U2895	inv	library	1.000000	
U2896	inv	library	1.000000	
U2897	inv	library	1.000000	
U2898	inv	library	1.000000	
U2899	inv	library	1.000000	
U2900	inv	library	1.000000	
U2901	inv	library	1.000000	
U2902	inv	library	1.000000	
U2903	inv	library	1.000000	
U2904	inv	library	1.000000	
U2905	inv	library	1.000000	
U2906	inv	library	1.000000	
U2907	inv	library	1.000000	
U2908	inv	library	1.000000	
U2909	inv	library	1.000000	
U2910	inv	library	1.000000	
U2911	inv	library	1.000000	
U2912	inv	library	1.000000	
U2913	inv	library	1.000000	
U2914	inv	library	1.000000	
U2915	inv	library	1.000000	
U2916	inv	library	1.000000	
U2917	inv	library	1.000000	
U2918	inv	library	1.000000	
data_out_reg[0]	dff	library	7.000000	n
data_out_reg[1]	dff	library	7.000000	n
data_out_reg[2]	dff	library	7.000000	n
data_out_reg[3]	dff	library	7.000000	n
data_out_reg[4]	dff	library	7.000000	n

data_out_reg[5]	dff	library	7.000000	n
data_out_reg[6]	dff	library	7.000000	n
data_out_reg[7]	dff	library	7.000000	n
data_out_reg[8]	dff	library	7.000000	n
data_out_reg[9]	dff	library	7.000000	n
data_out_reg[10]	dff	library	7.000000	n
data_out_reg[11]	dff	library	7.000000	n
data_out_reg[12]	dff	library	7.000000	n
data_out_reg[13]	dff	library	7.000000	n
data_out_reg[14]	dff	library	7.000000	n
data_out_reg[15]	dff	library	7.000000	n
mult_50/AN1_0	inv	library	1.000000	
mult_50/AN1_0_0	inv	library	1.000000	
mult_50/AN1_0_0_0	nor2	library	1.000000	
mult_50/AN1_0_1	nor2	library	1.000000	
mult_50/AN1_0_2	nor2	library	1.000000	
mult_50/AN1_0_3	nor2	library	1.000000	
mult_50/AN1_0_4	nor2	library	1.000000	
mult_50/AN1_0_5	nor2	library	1.000000	
mult_50/AN1_0_6	nor2	library	1.000000	
mult_50/AN1_0_7	nor2	library	1.000000	
mult_50/AN1_0_8	nor2	library	1.000000	
mult_50/AN1_0_9	nor2	library	1.000000	
mult_50/AN1_0_10	nor2	library	1.000000	
mult_50/AN1_0_11	nor2	library	1.000000	
mult_50/AN1_0_12	nor2	library	1.000000	
mult_50/AN1_0_13	nor2	library	1.000000	
mult_50/AN1_0_14	nor2	library	1.000000	
mult_50/AN1_1	inv	library	1.000000	
mult_50/AN1_1_0	inv	library	1.000000	
mult_50/AN1_1_0_0	nor2	library	1.000000	
mult_50/AN1_1_1	nor2	library	1.000000	
mult_50/AN1_1_2	nor2	library	1.000000	
mult_50/AN1_1_3	nor2	library	1.000000	
mult_50/AN1_1_4	nor2	library	1.000000	
mult_50/AN1_1_5	nor2	library	1.000000	
mult_50/AN1_1_6	nor2	library	1.000000	
mult_50/AN1_1_7	nor2	library	1.000000	
mult_50/AN1_1_8	nor2	library	1.000000	
mult_50/AN1_1_9	nor2	library	1.000000	
mult_50/AN1_1_10	nor2	library	1.000000	
mult_50/AN1_1_11	nor2	library	1.000000	
mult_50/AN1_1_12	nor2	library	1.000000	
mult_50/AN1_1_13	nor2	library	1.000000	
mult_50/AN1_1_14	nor2	library	1.000000	
mult_50/AN1_2	inv	library	1.000000	
mult_50/AN1_2_0	inv	library	1.000000	
mult_50/AN1_2_0_0	nor2	library	1.000000	
mult_50/AN1_2_1	nor2	library	1.000000	
mult_50/AN1_2_2	nor2	library	1.000000	
mult_50/AN1_2_3	nor2	library	1.000000	
mult_50/AN1_2_4	nor2	library	1.000000	
mult_50/AN1_2_5	nor2	library	1.000000	
mult_50/AN1_2_6	nor2	library	1.000000	
mult_50/AN1_2_7	nor2	library	1.000000	
mult_50/AN1_2_8	nor2	library	1.000000	
mult_50/AN1_2_9	nor2	library	1.000000	
mult_50/AN1_2_10	nor2	library	1.000000	
mult_50/AN1_2_11	nor2	library	1.000000	
mult_50/AN1_2_12	nor2	library	1.000000	
mult_50/AN1_2_13	nor2	library	1.000000	
mult_50/AN1_3	inv	library	1.000000	
mult_50/AN1_3_0	inv	library	1.000000	
mult_50/AN1_3_0_0	nor2	library	1.000000	

mult_50/AN1_3_1	nor2	library	1.000000
mult_50/AN1_3_2	nor2	library	1.000000
ram_reg[2][3]	dff	library	7.000000
ram_reg[2][4]	dff	library	7.000000
ram_reg[2][5]	dff	library	7.000000
ram_reg[2][6]	dff	library	7.000000
ram_reg[2][7]	dff	library	7.000000
ram_reg[2][8]	dff	library	7.000000
ram_reg[2][9]	dff	library	7.000000
ram_reg[2][10]	dff	library	7.000000
ram_reg[2][11]	dff	library	7.000000
ram_reg[2][12]	dff	library	7.000000
ram_reg[2][13]	dff	library	7.000000
ram_reg[2][14]	dff	library	7.000000
ram_reg[2][15]	dff	library	7.000000
ram_reg[3][0]	dff	library	7.000000
ram_reg[3][1]	dff	library	7.000000
ram_reg[3][2]	dff	library	7.000000
ram_reg[3][3]	dff	library	7.000000
ram_reg[3][4]	dff	library	7.000000
ram_reg[3][5]	dff	library	7.000000
ram_reg[3][6]	dff	library	7.000000
ram_reg[3][7]	dff	library	7.000000
ram_reg[3][8]	dff	library	7.000000
ram_reg[3][9]	dff	library	7.000000
ram_reg[3][10]	dff	library	7.000000
ram_reg[3][11]	dff	library	7.000000
ram_reg[3][12]	dff	library	7.000000
ram_reg[3][13]	dff	library	7.000000
ram_reg[3][14]	dff	library	7.000000
ram_reg[3][15]	dff	library	7.000000
ram_reg[4][0]	dff	library	7.000000
ram_reg[4][1]	dff	library	7.000000
ram_reg[4][2]	dff	library	7.000000
ram_reg[4][3]	dff	library	7.000000
ram_reg[4][4]	dff	library	7.000000
ram_reg[4][5]	dff	library	7.000000
ram_reg[4][6]	dff	library	7.000000
ram_reg[4][7]	dff	library	7.000000
ram_reg[4][8]	dff	library	7.000000
ram_reg[4][9]	dff	library	7.000000
ram_reg[4][10]	dff	library	7.000000
ram_reg[4][11]	dff	library	7.000000
ram_reg[4][12]	dff	library	7.000000
ram_reg[4][13]	dff	library	7.000000
ram_reg[4][14]	dff	library	7.000000
ram_reg[4][15]	dff	library	7.000000
ram_reg[5][0]	dff	library	7.000000
ram_reg[5][1]	dff	library	7.000000
ram_reg[5][2]	dff	library	7.000000
ram_reg[5][3]	dff	library	7.000000
ram_reg[5][4]	dff	library	7.000000
ram_reg[5][5]	dff	library	7.000000
ram_reg[5][6]	dff	library	7.000000
ram_reg[5][7]	dff	library	7.000000
ram_reg[5][8]	dff	library	7.000000
ram_reg[5][9]	dff	library	7.000000
ram_reg[5][10]	dff	library	7.000000
ram_reg[5][11]	dff	library	7.000000
ram_reg[5][12]	dff	library	7.000000
ram_reg[5][13]	dff	library	7.000000
ram_reg[5][14]	dff	library	7.000000
ram_reg[5][15]	dff	library	7.000000
ram_reg[6][0]	dff	library	7.000000

[illegible]



[illegible]

ram_reg[14][1]	dff	library	7.000000	n
ram_reg[14][2]	dff	library	7.000000	n
ram_reg[14][3]	dff	library	7.000000	n
ram_reg[14][4]	dff	library	7.000000	n
ram_reg[14][5]	dff	library	7.000000	n
ram_reg[14][6]	dff	library	7.000000	n
ram_reg[14][7]	dff	library	7.000000	n
ram_reg[14][8]	dff	library	7.000000	n
ram_reg[14][9]	dff	library	7.000000	n
ram_reg[14][10]	dff	library	7.000000	n
ram_reg[14][11]	dff	library	7.000000	n
ram_reg[14][12]	dff	library	7.000000	n
ram_reg[14][13]	dff	library	7.000000	n
ram_reg[14][14]	dff	library	7.000000	n
ram_reg[14][15]	dff	library	7.000000	n
ram_reg[15][0]	dff	library	7.000000	n
ram_reg[15][1]	dff	library	7.000000	n
ram_reg[15][2]	dff	library	7.000000	n
ram_reg[15][3]	dff	library	7.000000	n
ram_reg[15][4]	dff	library	7.000000	n
ram_reg[15][5]	dff	library	7.000000	n
ram_reg[15][6]	dff	library	7.000000	n
ram_reg[15][7]	dff	library	7.000000	n
ram_reg[15][8]	dff	library	7.000000	n
ram_reg[15][9]	dff	library	7.000000	n
ram_reg[15][10]	dff	library	7.000000	n
ram_reg[15][11]	dff	library	7.000000	n
ram_reg[15][12]	dff	library	7.000000	n
ram_reg[15][13]	dff	library	7.000000	n
ram_reg[15][14]	dff	library	7.000000	n
ram_reg[15][15]	dff	library	7.000000	n
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<b>Total 3506 cells</b>			<b>7092.000000</b>	