The University of Texas at Dallas

Dept of Electrical Engineering

EECT 6325: VLSI Design

Project 5

D Flip-Flop Design

Done by:

Names
Sameer Nitin Chourikar
Akilesh Sashank Akondi
Niket Kedarnath Ramani

Design Parameters

Parameter	Passing 0	Passing 1
Tsu _dd	27ps	10.5ps
Tsu _opt	47.5ps	39ps
T_hold	11.5ps	27.5ps
Tclk -> Q	325.6ps	331ps
TD	352ps	341.5ps

Width = 3.974 um

Length = 11.7 um

Area = 46.495 pm2

D Flip – Flop :

A D-Flip Flop is designed using two NOR gates, Tri state inverters in the design with an asynchronous Reset, the flip flop is made sensitive to the Negative edge of the clock cycle.

The Schematic of the Design which was discussed in class is done as below.

Measurement of D Flip-Flop times:

We need to find Tsu_dd, Tsu_opt, tD, Tclk-Q, Thold for passing 0 as well as passing 1 that is falling edge and rising edge respectively.

Tsu is the setup time defined as how long before capturing edge that D must be stable. Optimum setup time(Tsu_opt) is the set-up time for which Td is minimum is called optimum setup time.

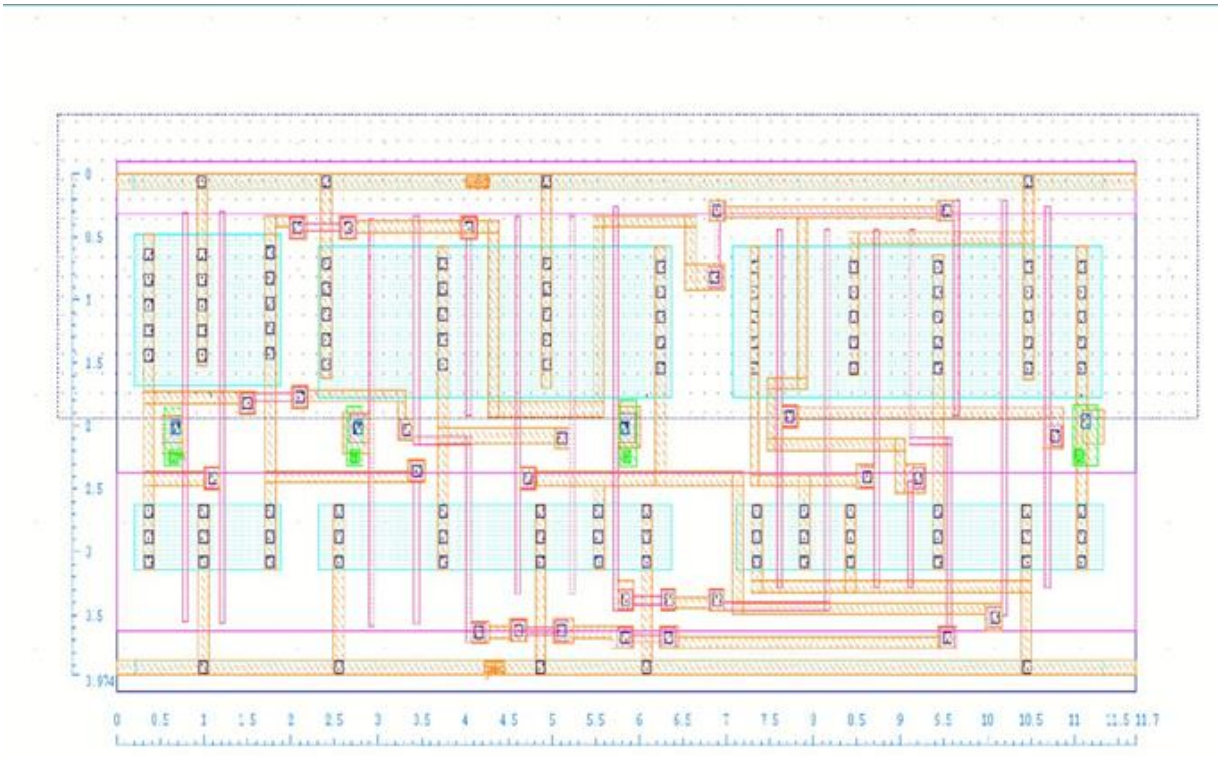
Thold is the time for indicating how long after capturing edge D must be maintained.

Tclk-Q is the time indicating how long after the capturing edge does new Q arrives. tD is the time required for the input signal to come at the output that is expressed as = Tsu + Tclk-Q

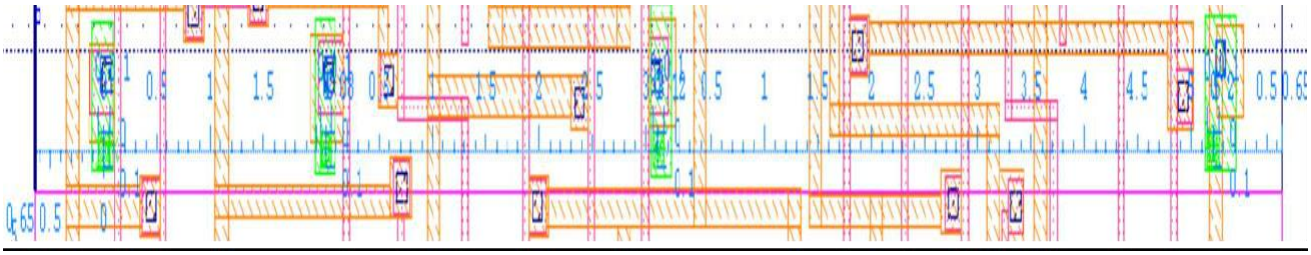
Tsu_dd is the drop-dead setup time defined as the minimum time required for the input signal to arrive before active clock edge so that the input signal can be correctly encountered at the output. It has been found that the values are different for both the edges. Also, Tsu_dd for falling edge is Thold for rising edge and vice versa.

Layout:

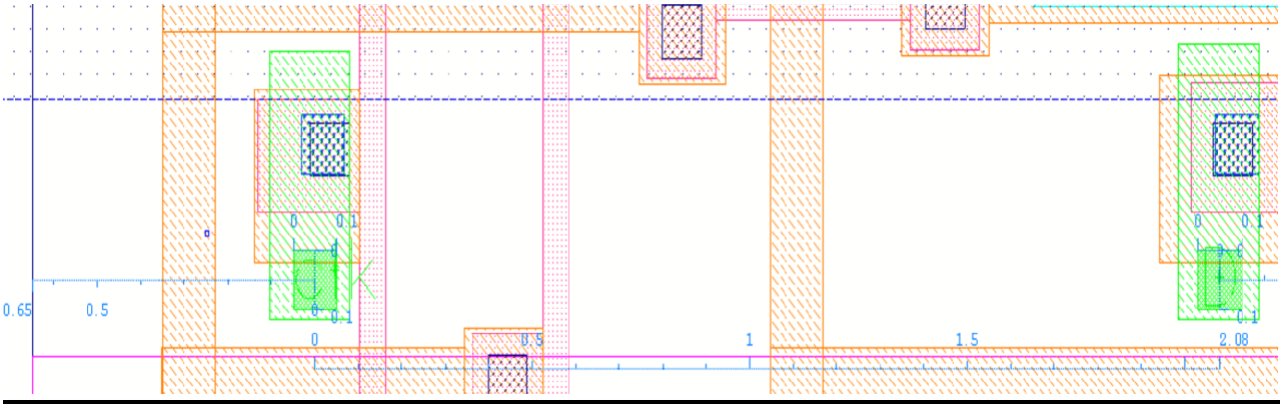
We designed the layout as per the design discussed by the Professor in the class. We got the schematic and to get the layout we had 2 diffusion breaks. We made sure that the width of our layout matches with the one in our previous project. Hence the design was such that our Wp=1.2um and Wn=0.52um. We discarded the use of metal 2. Hence out design has 0 vertical or 0 horizontal metal 2.



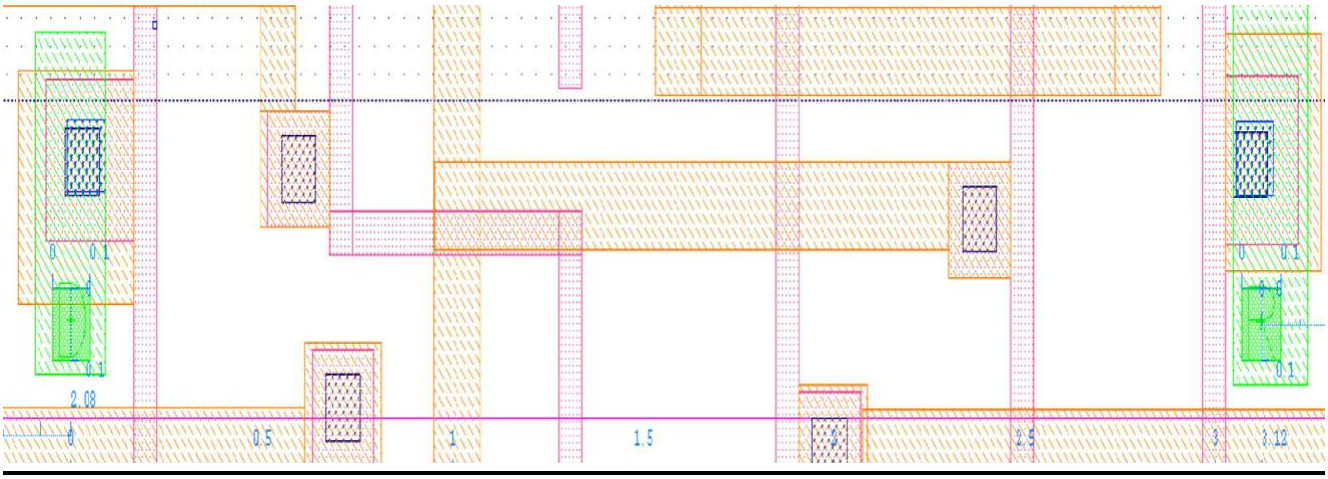
Distance between pins:



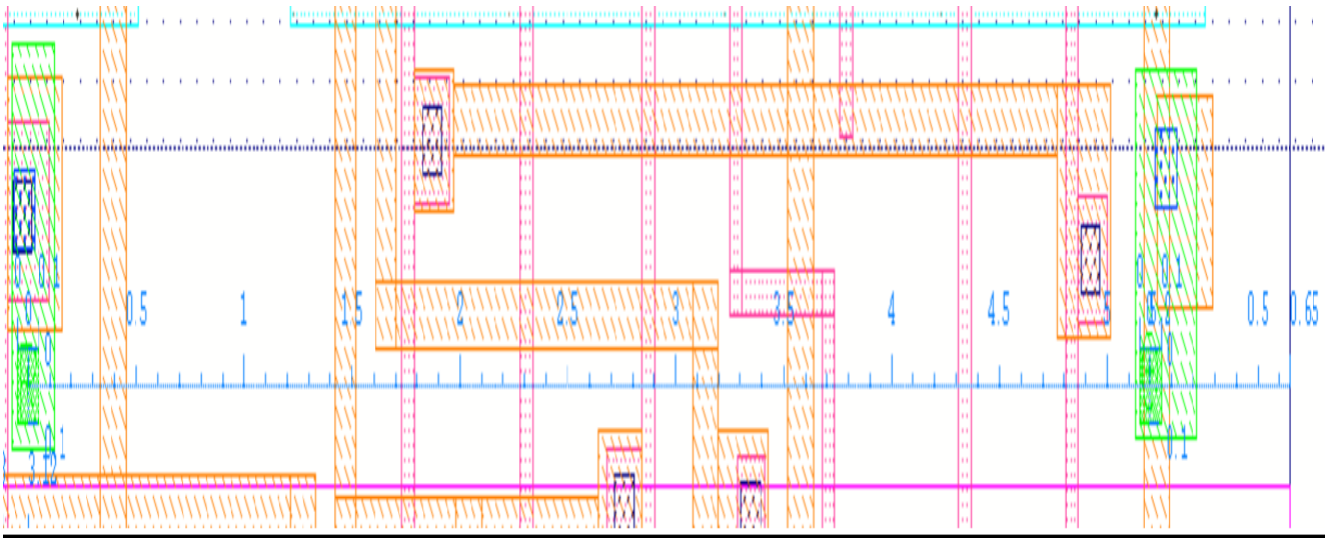
Distance between clk and input pin D :



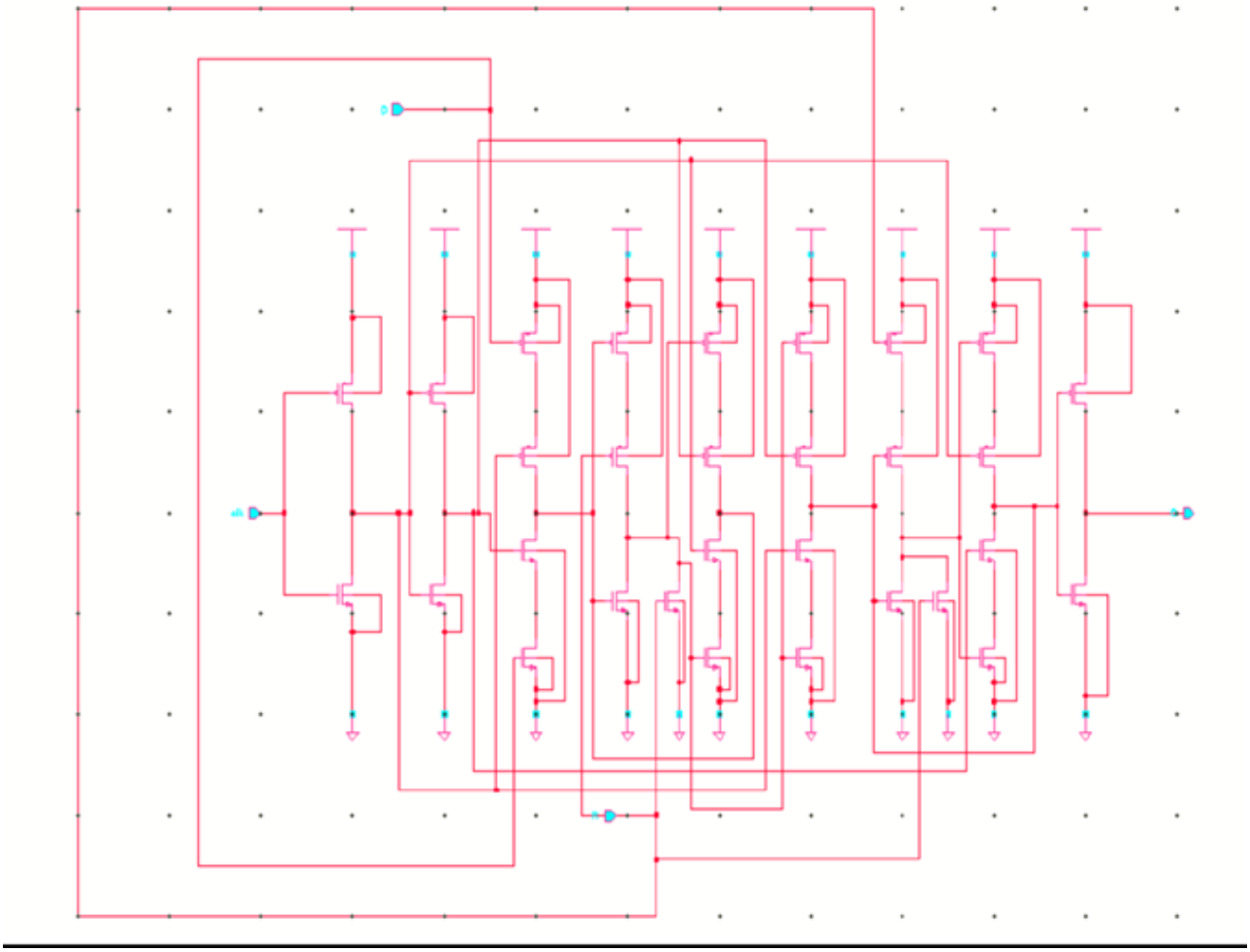
Distance between input pin D and input pin R :



Distance between input pin R and output pin Q :

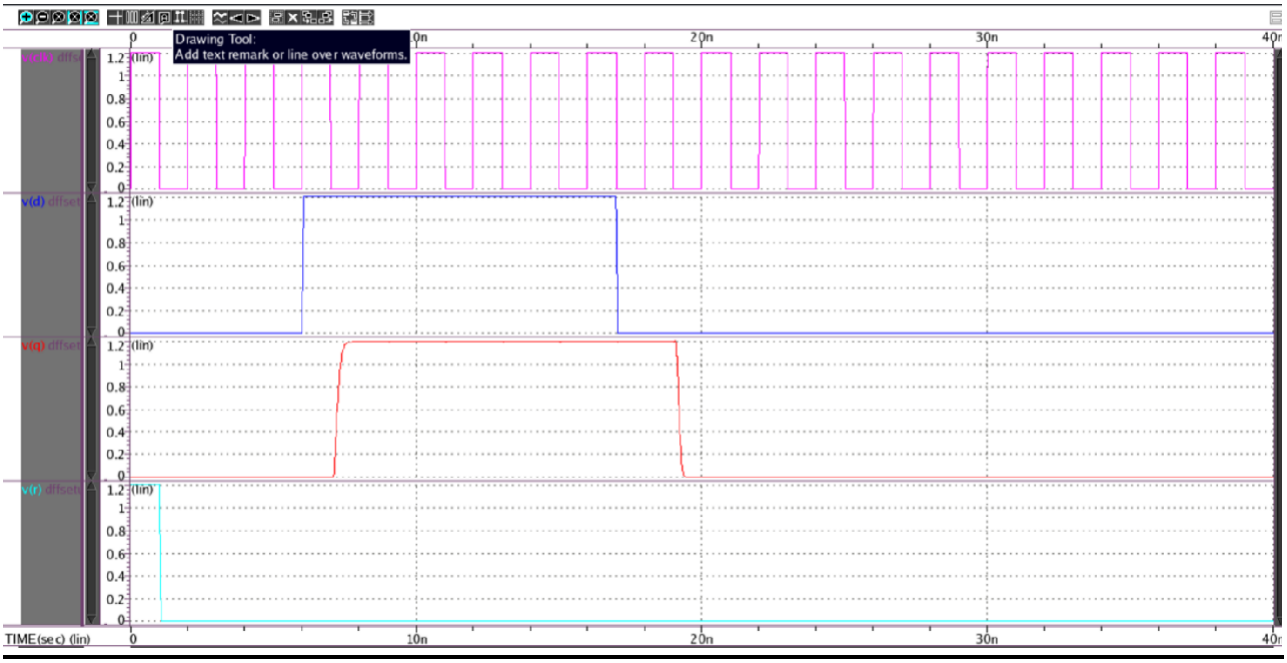


Schematic :

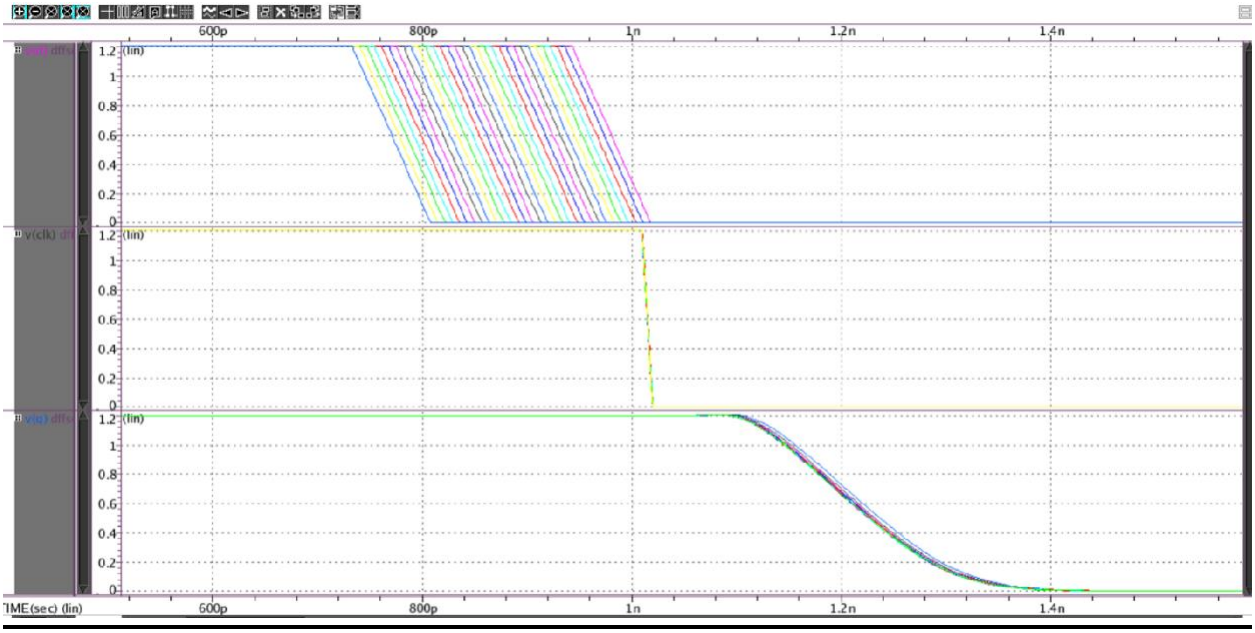


Waveforms:

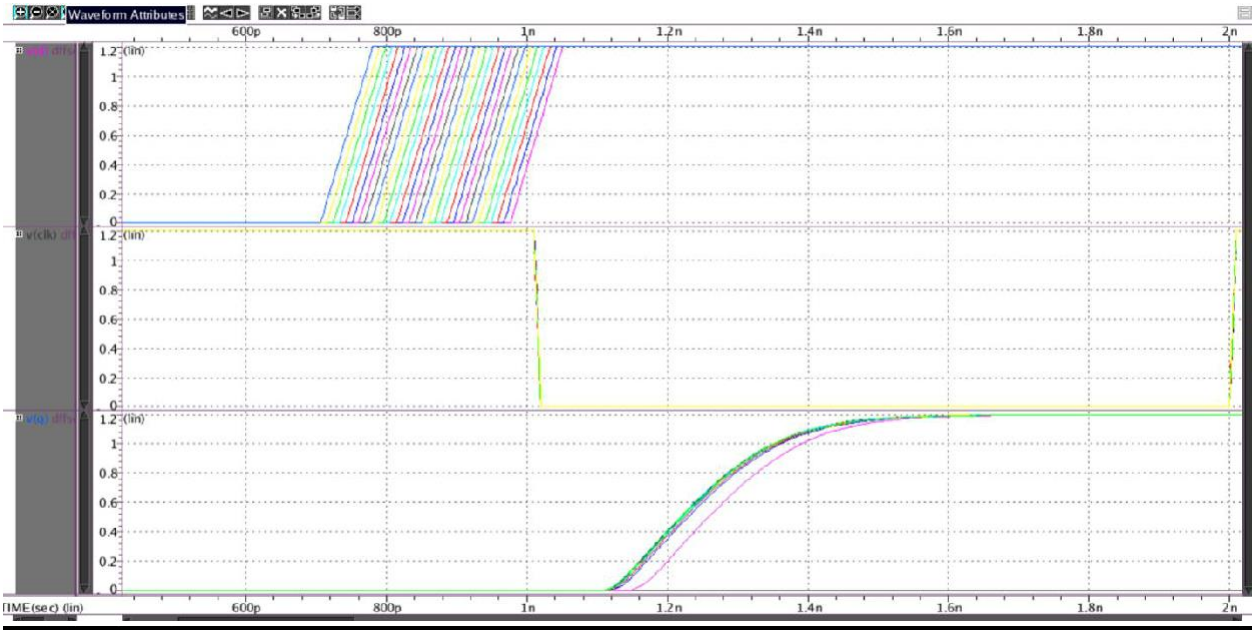
D Flipflop :



Passing 0:



Passing 1:



We observed the minimum delay from the graph plotting the values and the corresponding Tclk-Q and Tsu_opt was found. The graph was plotted is Tsu vs Td.

Passing 0 :

The setup time is calculated by making the input D from 1 to 0. The T delay is found by taking the sum of Tclk to q and Tsu which are the values that are swept and plotted on the graph.

Passing 1 :

The setup time is calculated by making the input D from 0 to 1. The T delay is found by taking the sum of Tclk to q and Tsu which are the values that are swept and plotted on the graph.

Spice netlist for D Flip flop :

$example HSPICE setup file

$transistor model

.include

"/proj/cad/library/mosis/GF65_LPe/cmos10lpe_CDS_oa_dl064_11_20160415/models/YI-SM00030/Hspice/models/design.inc"

.include DFF.pex.sp

.global vdd! gnd!

.option post runlvl=5

xi Q GND! VDD! clk D R DFF

vdd vdd! gnd! 1.2v

vclk clk gnd! pulse(0v 1.2v 0ps 0ps 0ps 1000ps 2000ps)

vD D gnd! pwl(0ns 0v 1ns 0v 1.075ns 0v 6ns 0v 6.075ns 1.2v 12ns 1.2v 12.075ns 1.2v 17ns 1.2v 17.075ns 0v 22ns 0v 22.075ns 0v 27ns 0v)

vR R gnd! pwl(0ns 1.2v 1000ps 1.2v 1075ps 0v 10ns 0v)

cout Q gnd! 90f

$transient analysis

.tr 10ps 40ns

.end

Spice netlist for passing 0:

$example HSPICE setup file

$transistor model

.include

"/proj/cad/library/mosis/GF65_LPe/cmos10lpe_CDS_oa_dl064_11_20160415/models/YI-SM00030/Hspice/models/design.inc"

.include DFF.pex.sp

.global vdd! gnd!

.option post runlvl=5

xi Q GND! VDD! clk D R DFF

vdd vdd! gnd! 1.2v

vclk clk gnd! pulse(0v 1.2v 0ps 0ps 0ps 1000ps

2000ps) vD D gnd! pwl(0ns 1.2v d 1.2v 'd+75ps' 0v)

vR R gnd! pwl(0ns 0v 100ps 0v 175ps 0v 10ns 0v)

cout Q gnd! 90f

$transient analysis

.trans 10ps 10ns sweep d 943ps 733ps -7ps

.MEAS tclktoq TRIG v(clk) VAL=0.6v FALL=1 TARG v(q) VAL=0.6v FALL=1

.MEAS tsetup TRIG v(d) VAL=.6v FALL=1 TARG v(clk) VAL=0.6v FALL=1

.MEAS tran tdelay param = 'tsetup+tclktoq'

.end

Spice netlist for passing 1:

$example HSPICE setup file

$transistor model

.include

"/proj/cad/library/mosis/GF65_LPe/cmos10lpe_CDS_oa_dl064_11_20160415/models/YI-SM00030/Hspice/models/design.inc"

.include DFF.pex.sp

.global vdd! gnd!

.option post runlvl=5

xi Q GND! VDD! clk D R DFF

vdd vdd! gnd! 1.2v

vclk clk gnd! pulse(0v 1.2v 0ps 0ps 0ps 1000ps

2000ps) vD D gnd! pwl(0ns 1.2v d 1.2v 'd+75ps' 1.2v)

vR R gnd! pwl(0ns 1.2v 100ps 1.2v 175ps 0v 10ns 0v)

cout Q gnd! 90f

$transient analysis

.trans 10ps 10ns sweep d 976ps 706ps -9ps

.MEAS tclktoq TRIG v(clk) VAL=0.6v FALL=1 TARG v(q) VAL=0.6v RISE=1

.MEAS tsetup TRIG v(d) VAL=.6v RISE=1 TARG v(clk) VAL=0.6v FALL=1

.MEAS tran tdelay param = 'tsetup+tclktoq'

.end