The University of Texas at Dallas

Dept of Electrical Engineering

EECT 6325: VLSI Design

Project 6

Final Layout and Verification

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Introduction

An Arithmetic Logic Unit (ALU) is a digital circuit that carries out arithmetic and logic operations on the operands in computer instruction words. It represents the fundamental building block of the processor of a computer and serves as the computational hub of the central processing unit (CPU) of a computer. Generally, an ALU is connected to the control unit and to the memory unit in a processor. The instruction word consists of an operation code (opcode), operands and/or memory locations. This opcode tells what operation to perform with the given operands in ALU. Since it has become one of the most important blocks of any processor, efforts are continuously made to increase the speed so that CPUs could contain very powerful and complex ALUs.

In this project, we have done 16 bit ALU with 16 operations including all the arithmetic operations like addition, subtraction, multiplication & division and logic operations like nand, nor, xor, left shift & right shift operations etc. 4 select lines are used to select these operations. Finally, the results are stored in a RAM. The RAM has its read and write operations to perform in the ALU.

Mode Selection Input	Operation
1	Addition
2	Subtraction
3	Multiplication
4	Division
5	Modulo 2 division
6	Logical and
7	Logical or
8	Logical nor
9	Logical nand
10	Logical xor
11	Logical xnor
12	Right shift input a
13	Left shift input a
14	Right shift input b
15	Left shift input b
16	Logical not

Tradeoffs:

- We had to increase the height of the cells – Inverter, NAND2, NOR2, XOR2, MUX2:1, OAI211, OAI21 and AOI22 in accordance to the height of the DFF, to generate the standard cell library of same heights (for proper fitting while performing Nano route in Innovus).

- We had designed filler so that the design meets all rules of 65nm technology when laid out using innovus tool.

- The DFF laid out had zero Metal 2 and to achieve that, we had to use some horizontal polys.

Inputs and Outputs of Design

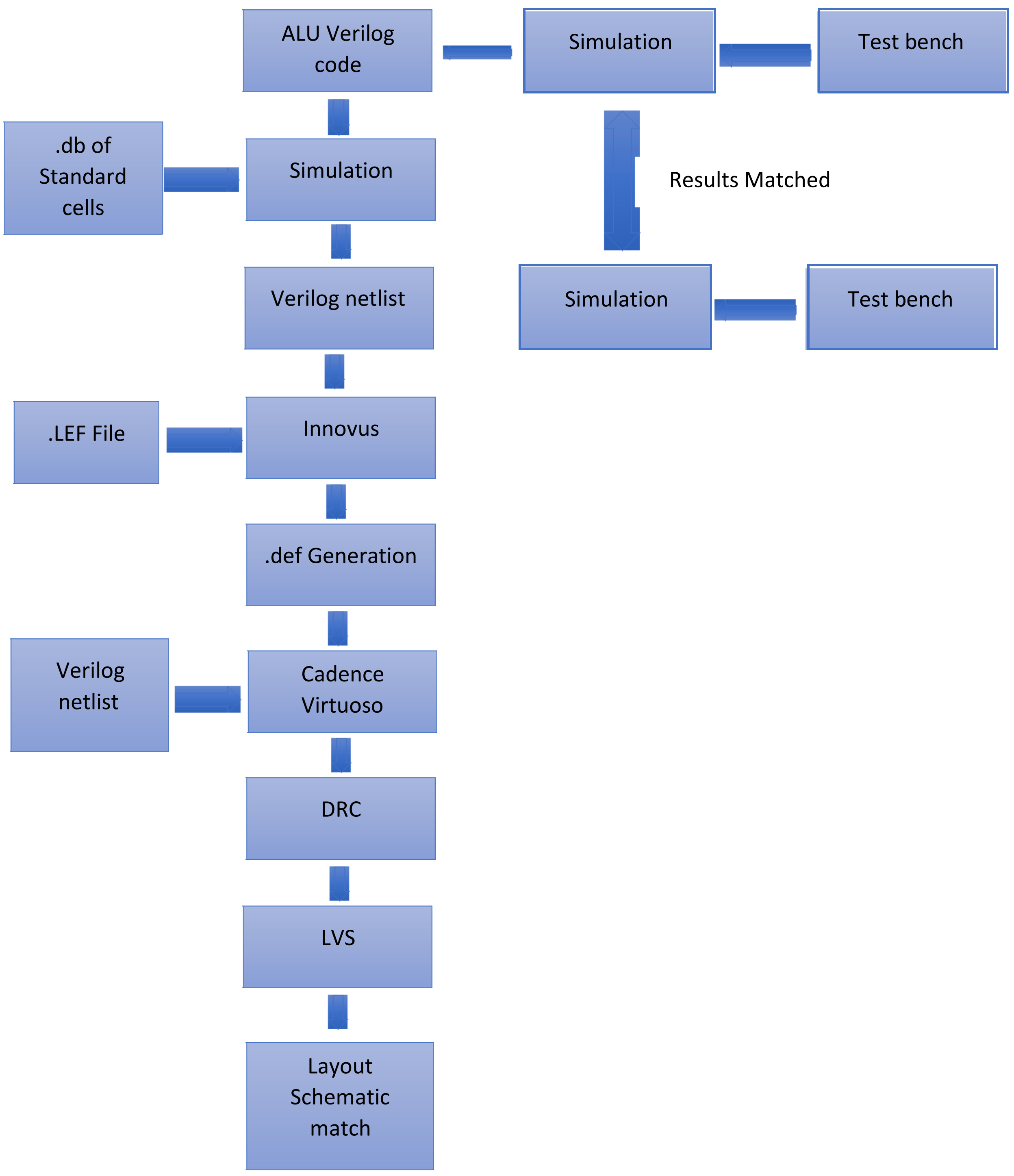
- The design contains 16-bit vector inputs ‘a’ and ‘b’ to the ALU.
- The select input is a 4-bit vector. This input controls the operation of the ALU.
- The output is a 32-bit vector, to accommodate the multiplication operation output.
- The ALU output is stored in a RAM. The RAM has the read and write operations for reading and writing into it respectively.
- The data can be restored from the RAM as per the need.

Design Flow

Project Design Flow

The procedure which was carried out in-order to obtain the same function as the second project’s Verilog code is as explained below. The flow chart is the outline work of all the major work transitions carried out for the project.

Tools used are: Cadence Virtuoso, Cadence Innovus, Synopsys Design Vision, Synopsys HSPICE, LC Shell, Synopsys Primetime, Wave view and Synopsys Silicon Smart (not necessarily in that order).


ALU Verilog code
Simulation
Test bench
.db of Standard cells
Simulation
Results Matched
Verilog netlist
Simulation
Test bench
.LEF File
Innovus
.def Generation
Verilog netlist
Cadence Virtuoso
DRC
LVS
Layout Schematic match

Creation of Standard Cell Library

Here, we laid out 9 cells in Cadence, which are then used to generate a standard library of cells. We also generated *.lef* file and the mapped Verilog netlist file.

The following cells are created using the Cadence Virtuoso tool which will in turn form the standard cell library –

1. Inverter
2. NAND2
3. NOR2
4. XOR2
5. MUX2:1
6. DFF
7. OAI211
8. AOI22
9. OAI21

- All the cells were laid out so that there are NO DRC errors.
- Height of all cells – 4.42 um and the pin pitch is 0.52 um.
- The width of pMOS is such that it has minimum of 5 contacts – 1.2 um and that of nMOS is such that it has minimum of 3 contacts – 0.52um.
- Schematic view of all these cells are created and we made sure that there are NO LVS errors, i.e., schematic views and layout views are matched.
- Abstract views were generated for all the cells and PEX generation is performed on all these cells in order to obtain the spice (*.sp*) files for all the cells.
- Using the extracted netlist, the functionality of each cell is checked by simulating in HSPICE and waveform generation using Wave view.

Generation of the Library and characterization of the design

- Using the. sp files generated from Cadence Virtuoso, we generated the *.lib* file using Siliconsmart for each standard cell.
- We combined the .lib files of all the cells into one .lib file and converted it into *.db* file using the Synopsys LC Shell tool. Then we extract the synthesized netlist using Synopsys Design Vision from the verilog file.
- The Design Vision tool also gives out the number of cells present in the design.

Generation of *.LEF* file

- Using Cadence Virtuoso tool, *.lef* file is generated by using the abstract views of all the standard cells.
- This file and the synthesized Verilog file are the inputs to the Cadence Innovus software, which is used for placement and routing.

Automatic Placement and Routing

The Auto-placement and routing of the design is done using the Cadence Innovus tool. Innovus takes in the mapped Verilog netlist and the generated *.lef* file. The *lef* format contains pin connectivity and cell size information of our library.

Filler design:

Before we proceed with innovus to perform auto-placement and routing we designed filler that will be used by the innovus to fill the space between the cells in each row. We designed the filler such that the width of the filler is 1 pitch size (0.26 um) and the height of the filler matched with all the other cells in our standard cell library. It is added in the library as mentioned earlier.

Floor Planning:

Floor planning is done by setting the aspect ratio to 1 and by setting the IO to core distance as 0.7 microns. The row spacing is set to 5 um per one row.

Placement and adding fillers between cells:

After floor planning IO ports and cells are placed in the allotted rows and the fillers are added between the cells using the related options in the innovus design environment tool.

Power/Ground:

Power planning of the layout is done by setting vdd & gnd. Later the metal layer is changed to M1 and the width and spacing between the vdd and gnd pins is changed accordingly so that they match with all the cells in our library. The width of the power rail is 0.2um.

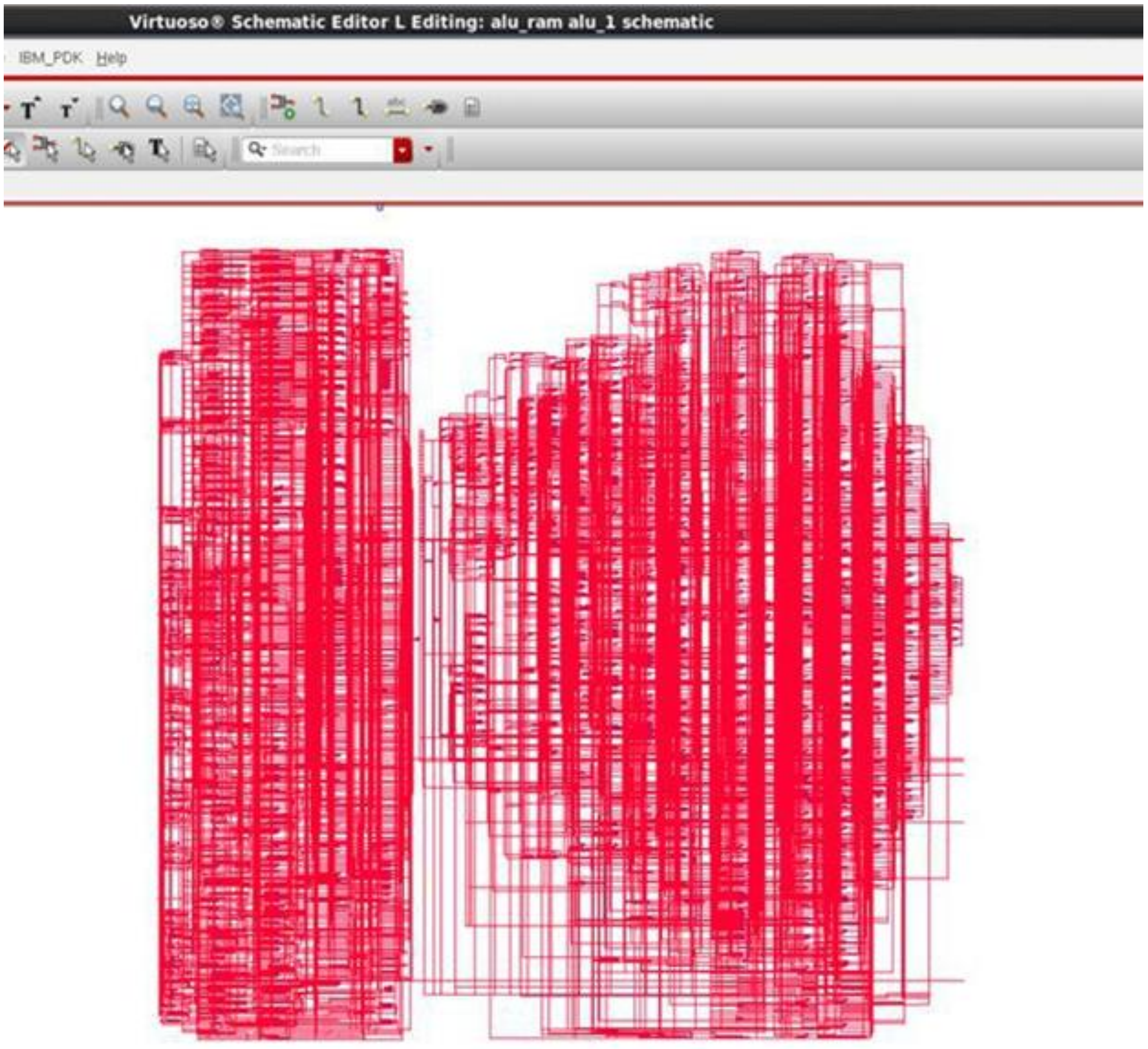
Routing:

We will connect the cells together and to the I/O pins by routing the circuit nets. Routing is done by selecting the ‘Nano Route’ option in the tool. Finally, a layout of our design is generated with wires connected to our pins.

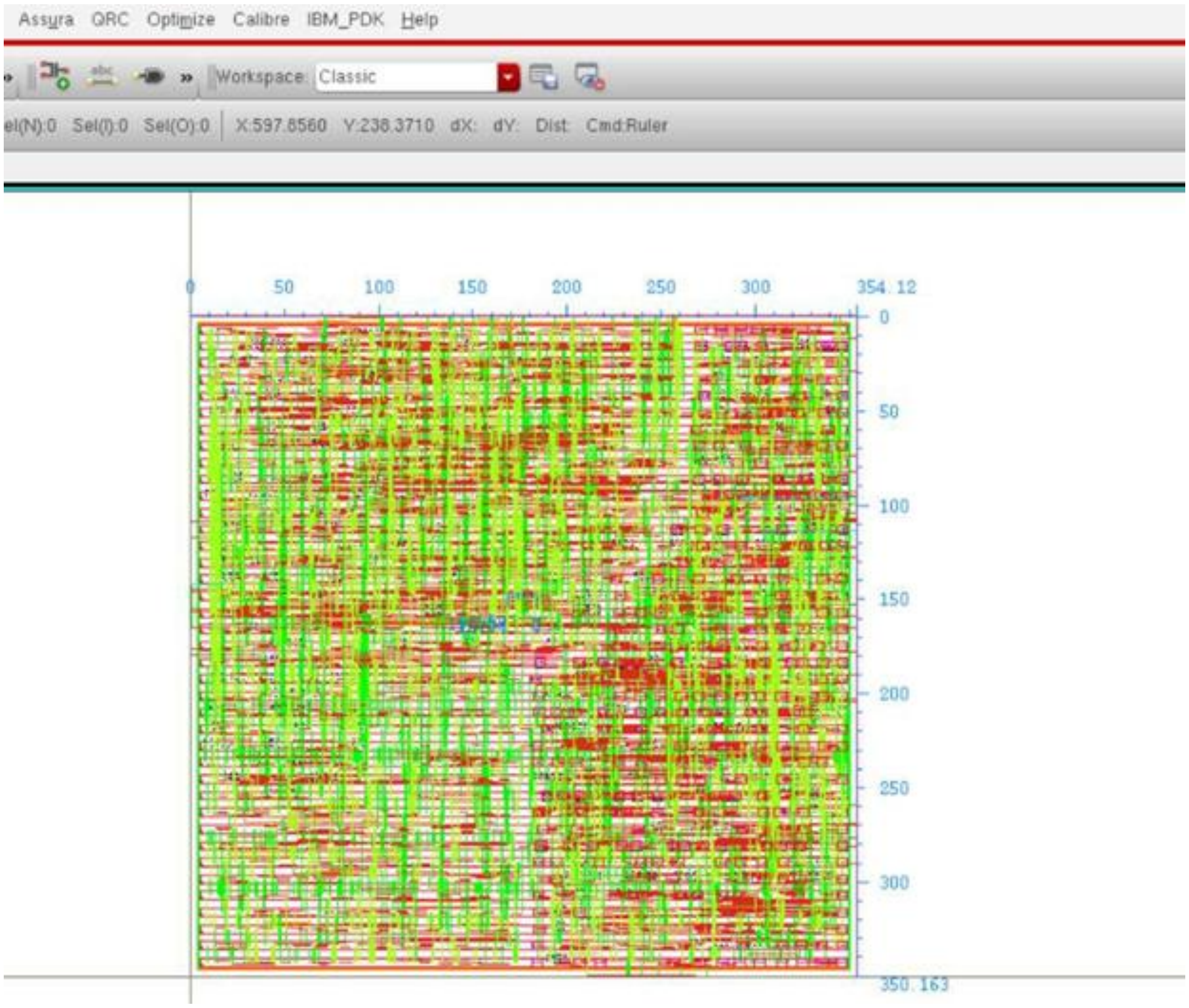
Exporting DEF format file and Importing into Cadence:

After the completion of the layout design we export a DEF file format into Virtuoso that contains physical cell placement and automatic routing information as well as electrical net information. This is imported to Cadence to create the layout view of the design. On creating the layout, DRC and LVS check is done and is ensured to pass.

Final Schematic :


Virtuoso® Schematic Editor L Editing: alu_ram alu_1 schematic
IBM_PDK
Help
Search

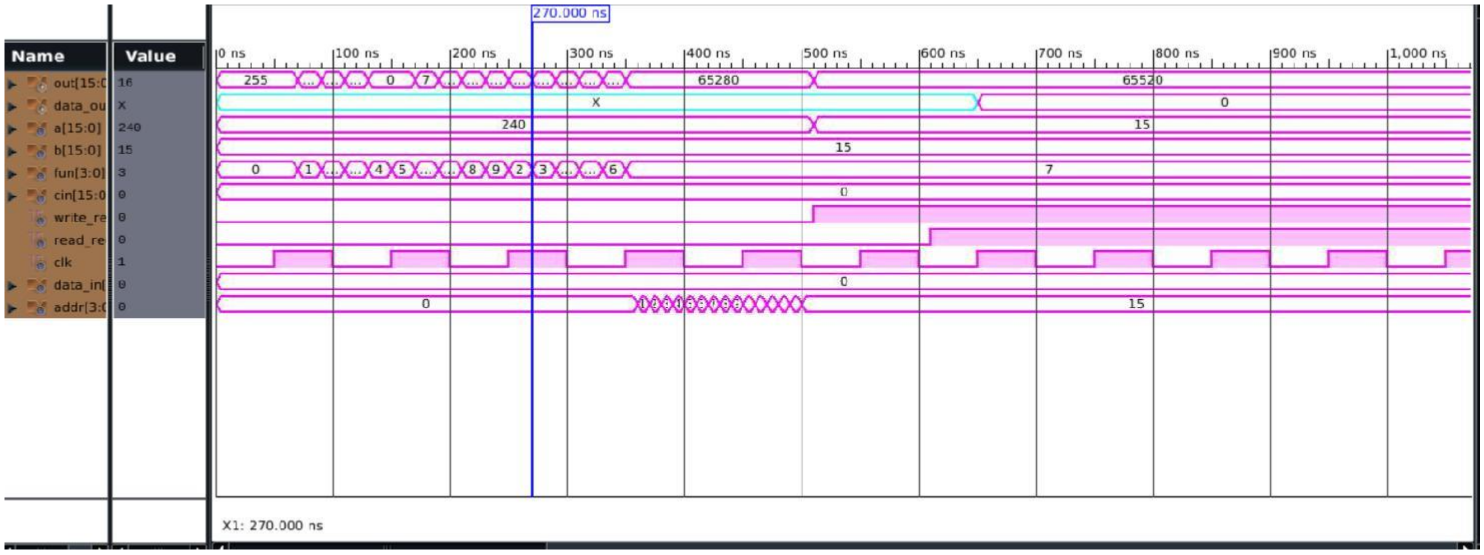
Final Layout :


Assura QRC Optimize Calibre IBM_PDK Help
Workspace: Classic
el(N):0 Sel(I):0 Sel(O):0 X:597.8560 Y:238.3710 dX: dY: Dist: Cmd:Ruler
0 50 100 150 200 250 300 354.12
0 50 100 150 200 250 300 350.163

OUTPUT WAVEFORM GENERATION

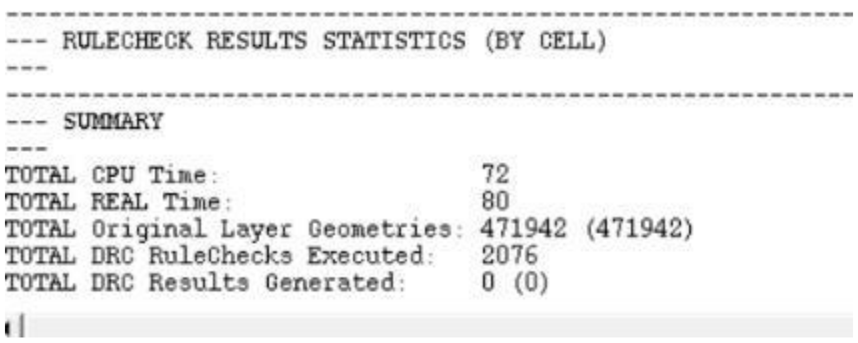
Steps for verification:

1) The library.db file is linked with the verilog file and the corresponding gate level netlist is obtained.
2) Modified the header.v file so that it contains only the cells we designed and concatenated with the mapped Verilog file.
3) The generated netlist is them simulated on ISim tool using the same testbench which we had used for simulating Behavioral code. It was observed that the Mapped Synthesized netlist has same behavior as that of the Behavioral netlist.

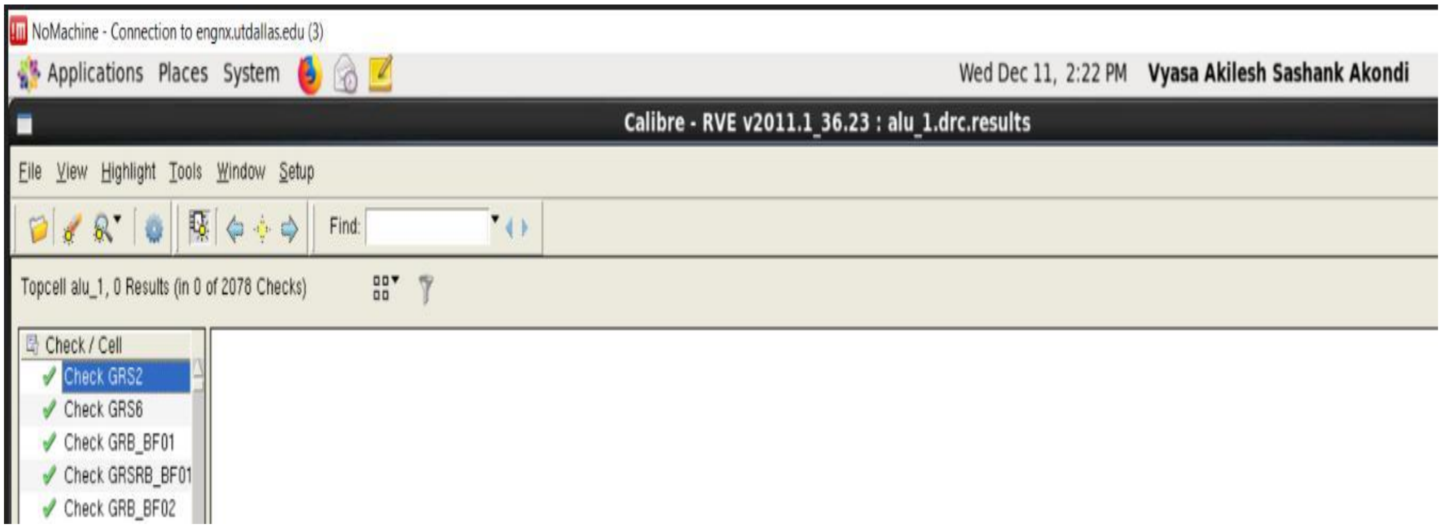


The Design Rule Check (DRC)

The following images contain the DRC check performed on the design. It can be seen that the design is free of any DRC errors!



```
--------------------------------------------------------------
--- RULECHECK RESULTS STATISTICS (BY CELL)
---
--------------------------------------------------------------
--- SUMMARY
---
TOTAL CPU Time:                  72
TOTAL REAL Time:                 80
TOTAL Original Layer Geometries: 471942 (471942)
TOTAL DRC RuleChecks Executed:   2076
TOTAL DRC Results Generated:     0 (0)
```



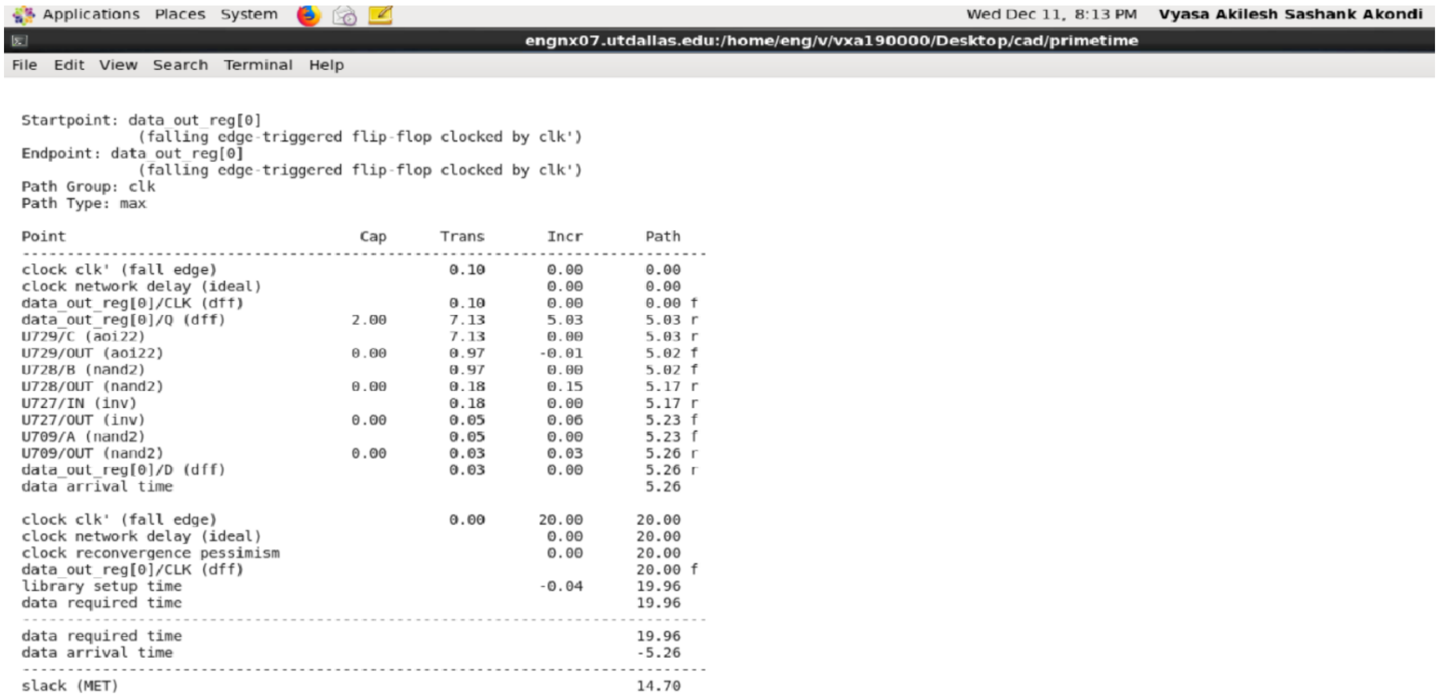
Topcell alu_1, 0 Results (in 0 of 2078 Checks)

NoMachine - Connection to engnx.utdallas.edu (3)
Applications Places System
Wed Dec 11, 2:22 PM Vyasa Akilesh Sashank Akondi
Calibre - RVE v2011.1_36.23 : alu_1.drc.results
File View Highlight Tools Window Setup
Find:
Check / Cell
Check GRS2
Check GRS6
Check GRB_BF01
Check GRSRB_BF01
Check GRB_BF02

Primetime Report

The following images contain the information about the best possible clock period and total power consumed.

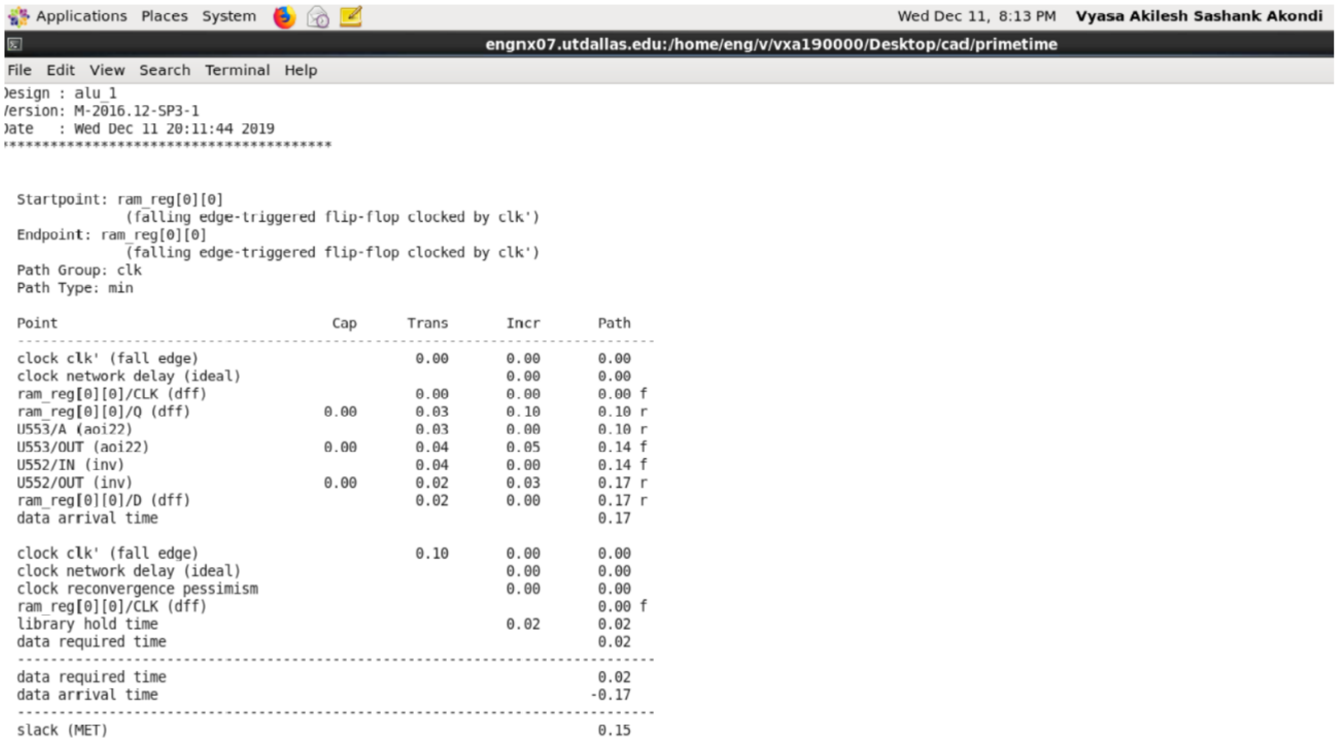
i) Slack Times


Applications Places System
Wed Dec 11, 8:13 PM Vyasa Akilesh Sashank Akondi
engnx07.utdallas.edu:/home/eng/v/vxa190000/Desktop/cad/primetime
File Edit View Search Terminal Help

```
Startpoint: data_out_reg[0]
              (falling edge-triggered flip-flop clocked by clk')
Endpoint: data_out_reg[0]
              (falling edge-triggered flip-flop clocked by clk')
Path Group: clk
Path Type: max

Point                                    Cap      Trans       Incr        Path
-----------------------------------------------------------------------------
clock clk' (fall edge)                             0.10       0.00        0.00
clock network delay (ideal)                                   0.00        0.00
data_out_reg[0]/CLK (dff)                          0.10       0.00        0.00 f
data_out_reg[0]/Q (dff)                 2.00       7.13       5.03        5.03 r
U729/C (aoi22)                                     7.13       0.00        5.03 r
U729/OUT (aoi22)                        0.00       0.97      -0.01        5.02 f
U728/B (nand2)                                     0.97       0.00        5.02 f
U728/OUT (nand2)                        0.00       0.18       0.15        5.17 r
U727/IN (inv)                                      0.18       0.00        5.17 r
U727/OUT (inv)                          0.00       0.05       0.06        5.23 f
U709/A (nand2)                                     0.05       0.00        5.23 f
U709/OUT (nand2)                        0.00       0.03       0.03        5.26 r
data_out_reg[0]/D (dff)                            0.03       0.00        5.26 r
data arrival time                                                         5.26

clock clk' (fall edge)                             0.00      20.00       20.00
clock network delay (ideal)                                   0.00       20.00
clock reconvergence pessimism                                 0.00       20.00
data_out_reg[0]/CLK (dff)                                                20.00 f
library setup time                                           -0.04       19.96
data required time                                                       19.96
-----------------------------------------------------------------------------
data required time                                                       19.96
data arrival time                                                        -5.26
-----------------------------------------------------------------------------
slack (MET)                                                              14.70
```


Applications Places System
Wed Dec 11, 8:13 PM Vyasa Akilesh Sashank Akondi
engnx07.utdallas.edu:/home/eng/v/vxa190000/Desktop/cad/primetime
File Edit View Search Terminal Help

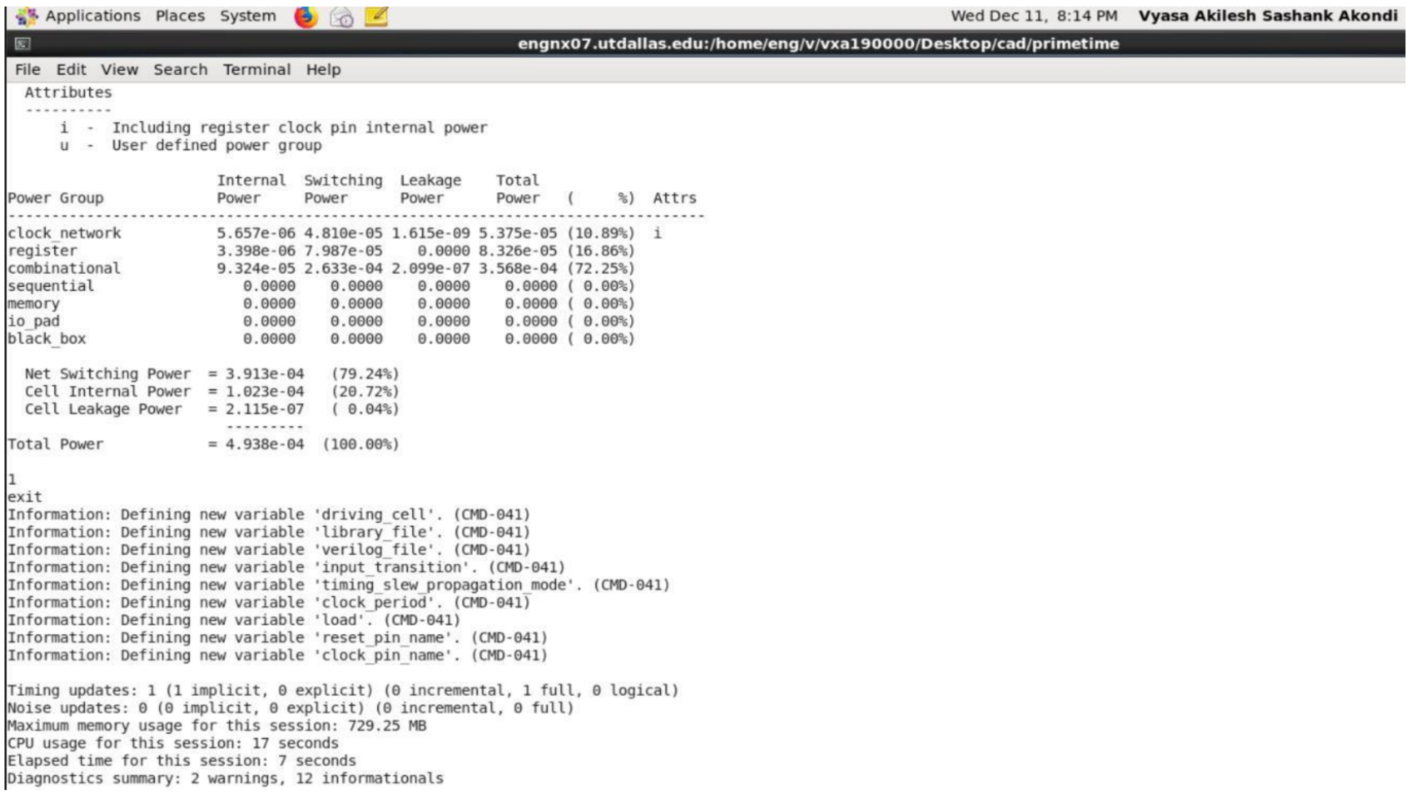
```
)esign : alu_1
/ersion: M-2016.12-SP3-1
)ate   : Wed Dec 11 20:11:44 2019
****************************************


 Startpoint: ram_reg[0][0]
               (falling edge-triggered flip-flop clocked by clk')
 Endpoint: ram_reg[0][0]
               (falling edge-triggered flip-flop clocked by clk')
 Path Group: clk
 Path Type: min

 Point                                  Cap      Trans      Incr       Path
 ---------------------------------------------------------------------------
 clock clk' (fall edge)                           0.00      0.00       0.00
 clock network delay (ideal)                                0.00       0.00
 ram_reg[0][0]/CLK (dff)                          0.00      0.00       0.00 f
 ram_reg[0][0]/Q (dff)                 0.00       0.03      0.10       0.10 r
 U553/A (aoi22)                                   0.03      0.00       0.10 r
 U553/OUT (aoi22)                      0.00       0.04      0.05       0.14 f
 U552/IN (inv)                                    0.04      0.00       0.14 f
 U552/OUT (inv)                        0.00       0.02      0.03       0.17 r
 ram_reg[0][0]/D (dff)                            0.02      0.00       0.17 r
 data arrival time                                                     0.17

 clock clk' (fall edge)                           0.10      0.00       0.00
 clock network delay (ideal)                                0.00       0.00
 clock reconvergence pessimism                              0.00       0.00
 ram_reg[0][0]/CLK (dff)                                               0.00 f
 library hold time                                          0.02       0.02
 data required time                                                    0.02
 ---------------------------------------------------------------------------
 data required time                                                    0.02
 data arrival time                                                    -0.17
 ---------------------------------------------------------------------------
 slack (MET)                                                           0.15
```

ii) Total Power Consumed


Applications Places System
Wed Dec 11, 8:14 PM Vyasa Akilesh Sashank Akondi
engnx07.utdallas.edu:/home/eng/v/vxa190000/Desktop/cad/primetime
File Edit View Search Terminal Help

```
  Attributes
  ----------
      i  -  Including register clock pin internal power
      u  -  User defined power group

                        Internal  Switching  Leakage    Total
Power Group             Power     Power      Power      Power   (     %)  Attrs
--------------------------------------------------------------------------------
clock_network           5.657e-06 4.810e-05 1.615e-09 5.375e-05 (10.89%)  i
register                3.398e-06 7.987e-05    0.0000 8.326e-05 (16.86%)
combinational           9.324e-05 2.633e-04 2.099e-07 3.568e-04 (72.25%)
sequential                 0.0000    0.0000    0.0000    0.0000 ( 0.00%)
memory                     0.0000    0.0000    0.0000    0.0000 ( 0.00%)
io_pad                     0.0000    0.0000    0.0000    0.0000 ( 0.00%)
black_box                  0.0000    0.0000    0.0000    0.0000 ( 0.00%)

  Net Switching Power  = 3.913e-04   (79.24%)
  Cell Internal Power  = 1.023e-04   (20.72%)
  Cell Leakage Power   = 2.115e-07   ( 0.04%)
                         ---------
Total Power            = 4.938e-04  (100.00%)

1
exit
Information: Defining new variable 'driving_cell'. (CMD-041)
Information: Defining new variable 'library_file'. (CMD-041)
Information: Defining new variable 'verilog_file'. (CMD-041)
Information: Defining new variable 'input_transition'. (CMD-041)
Information: Defining new variable 'timing_slew_propagation_mode'. (CMD-041)
Information: Defining new variable 'clock_period'. (CMD-041)
Information: Defining new variable 'load'. (CMD-041)
Information: Defining new variable 'reset_pin_name'. (CMD-041)
Information: Defining new variable 'clock_pin_name'. (CMD-041)

Timing updates: 1 (1 implicit, 0 explicit) (0 incremental, 1 full, 0 logical)
Noise updates: 0 (0 implicit, 0 explicit) (0 incremental, 0 full)
Maximum memory usage for this session: 729.25 MB
CPU usage for this session: 17 seconds
Elapsed time for this session: 7 seconds
Diagnostics summary: 2 warnings, 12 informationals
```

Conclusion:

- Verilog HDL: A 16 bit ALU with the following functionalities: (Arithmetic: Addition, Subtraction, Multiplication, Division, Modulo 2 division; Logical: AND, OR, XOR, NOR, NAND, XNOR, NOT; Relational: Left shift, right shift) was implemented. A RAM was created to read and write the ALU information.

- Using tools such as Innovus, Virtuoso and Synopsys, we have laid out the ALU and RAM design. These tools helped to understand what the Semiconductor Industry actually uses to design the chips.

- Use of tools such as HSPICE, Siliconsmart, etc made us appreciate the importance of testing the design of the circuit.

- Overall, this project will always be very useful for us because it will serve to be a steppingstone towards a career in VLSI Design.