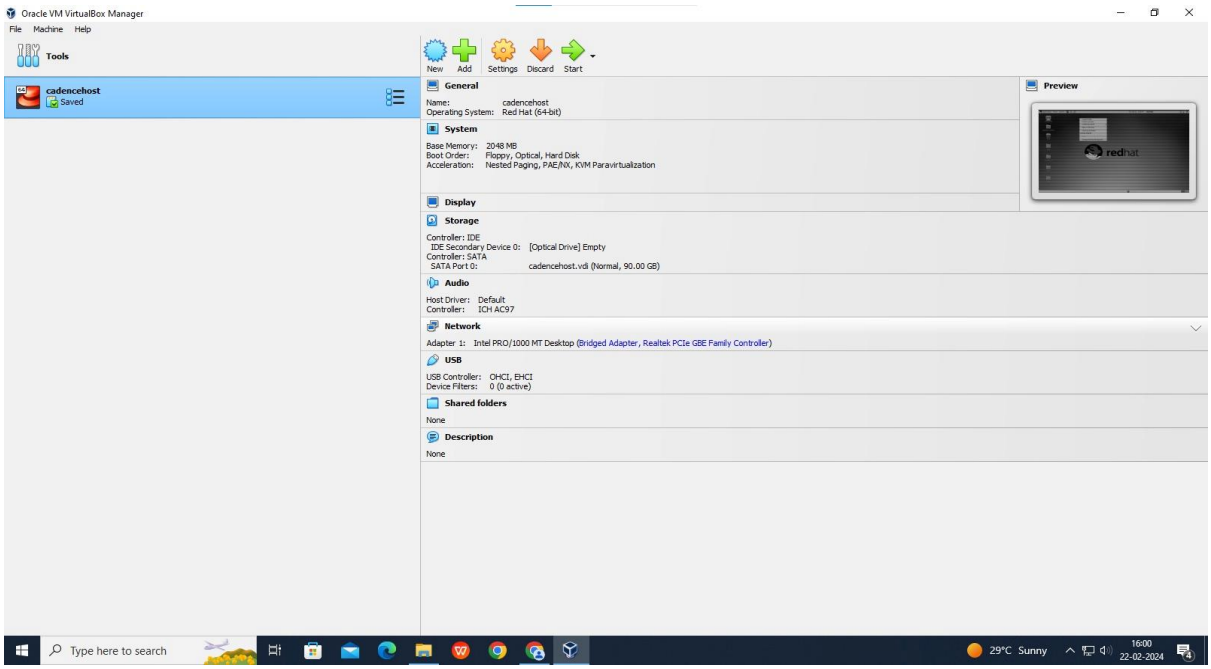
SCHEMATIC SYMBOL AND SIMULATION OF NAND AND XOR GATES

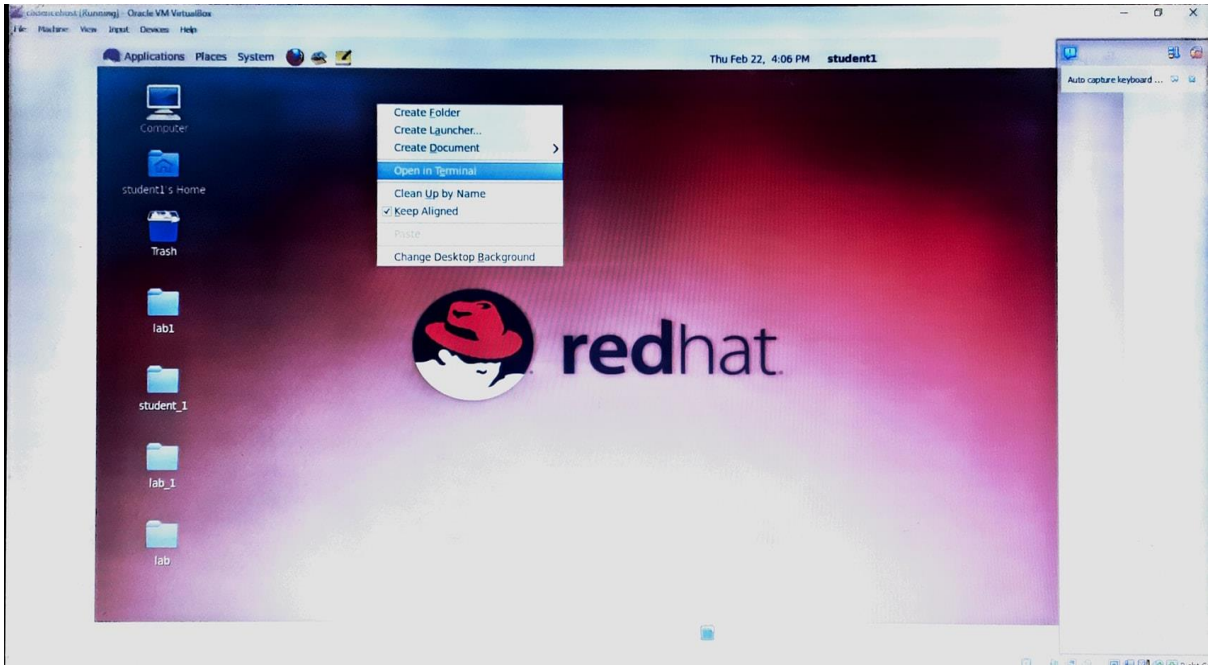
STEPS:

1)Open oracle VM virtual box

2)Click on start



3)Right click on workspace, select **open in terminal**



4)Type the commands

mkdir <any name> (ENTER)

cd <any name> (ENTER)

pwd (ENTER)

source /usr/software/gpdk090 (ENTER)

virtuoso & (ENTER)

EXPLANATION:

mkdir: This command is used to create a new directory (folder) within the current directory.

cd: Short for "**change directory**," this command is used to navigate between directories. For example, cd folder_name would move you into the directory named "folder_name."

pwd: Short for "**print working directory**," this command shows you the full path of the current directory you are in.

virtuoso: Virtuoso is a widely-used tool within Cadence for electronic design automation (EDA). It's primarily used for designing and simulating integrated circuits (ICs) and electronic systems. It includes various modules for schematic capture, layout editing, simulation, and more.

5)virtuso tab appears

6)In virtuoso tab

- File>New>Library>mylib(give any name)>select Attach library to technology>Ok
- Select **gpdk090>Ok**

Again in Virtuoso tab

- Tools>Library Manager>mylib

7)In mylib

- File>New>cell view
- Enter cell view: **nand2**
- Select OK

8)Create>Instance(shortcut-press **"I**")

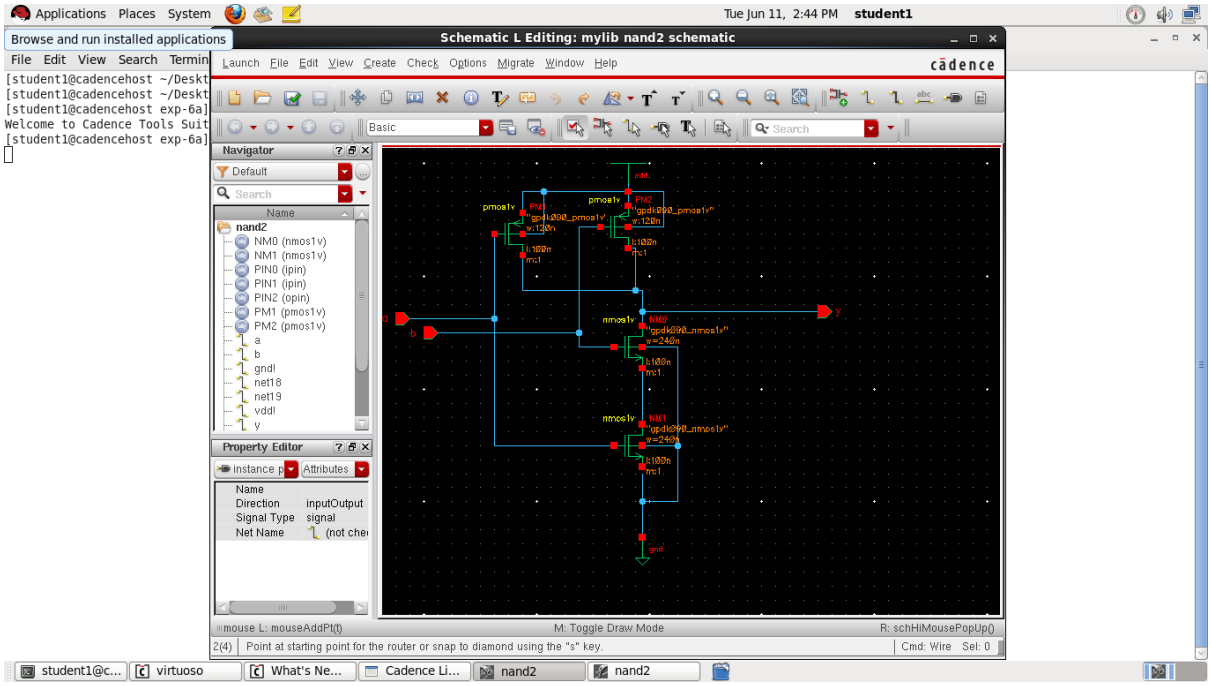
- Select the following and place it on the schematic Editing window each time.

Library	Cell view	Value
gpdk090	nmos1v	2
gpdk090	Pmos1v	2
analogLib	vdd	Hide
analogLib	gnd	Hide

9)Set up the connections as shown

Press **“W”** for wire to connect the circuit

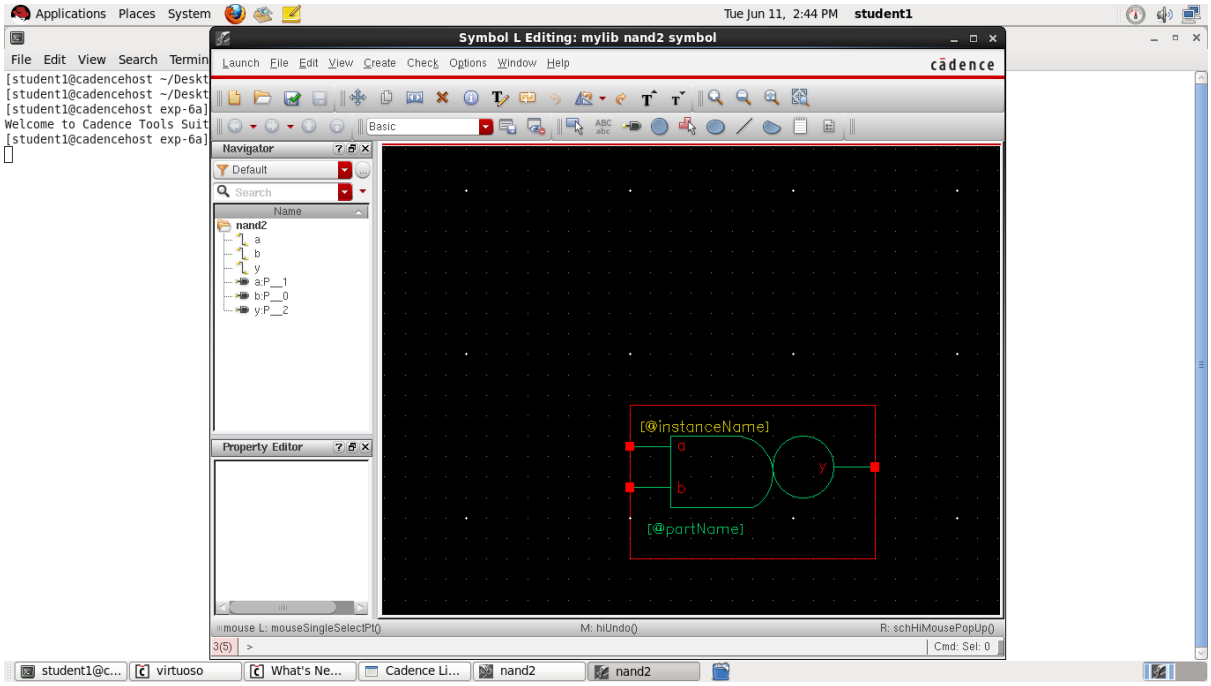
10)Create>pins>a b (input) , y(output)>Save



11)Create>**Cell view**>From Cell view>in Pop Up >OK>In another Pop Up>Select left pin:a b

right pin: y

12)Convert it into the following format using wire and create>shapes:circle, arc



13)Save

14)Go back to **mylib**>click on **nand2**>File>New>cell view>nand2test>a new schematic window appears

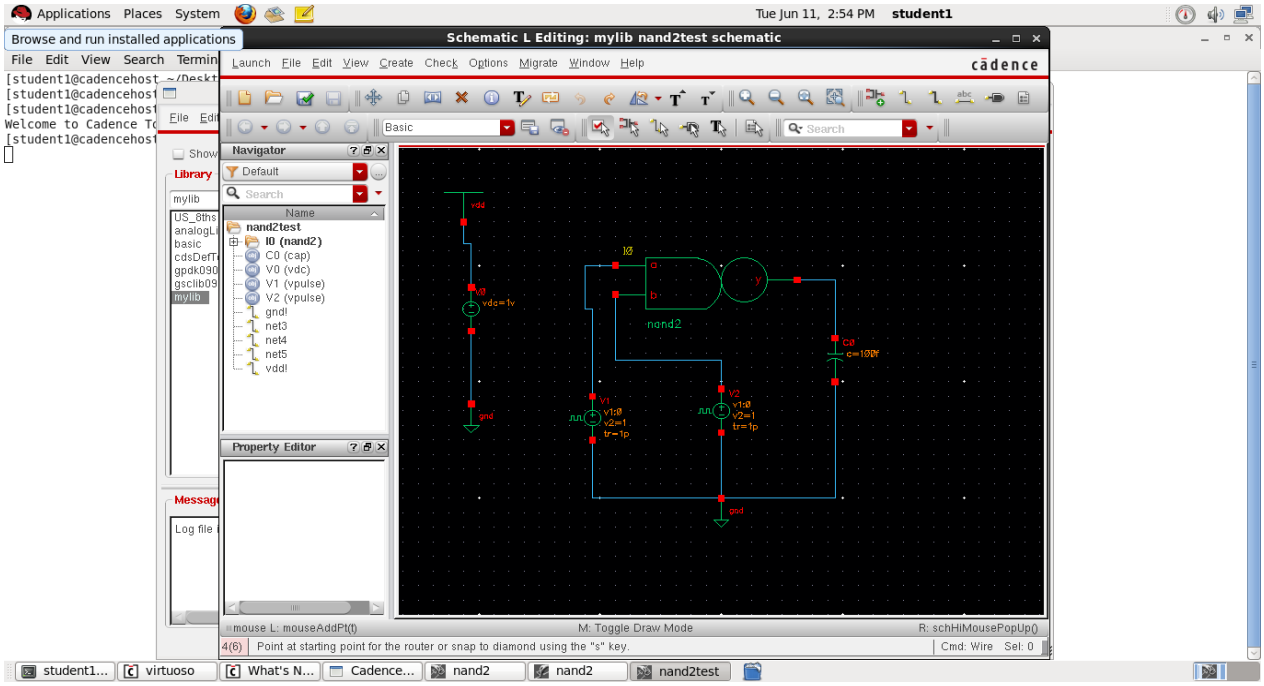
15)Create>instance

Library	Cell view	Select
mylib	nand2	Hide
analogLib	vdc	Hide
analogLib	vdd	Hide
analogLib	gnd	2
analogLib	vpulse	2
analogLib	cap	Hide

16)Set up the connections as shown

Press **“W”** for wire to connect the circuit

17) Create>wire name>va vb vy>Save

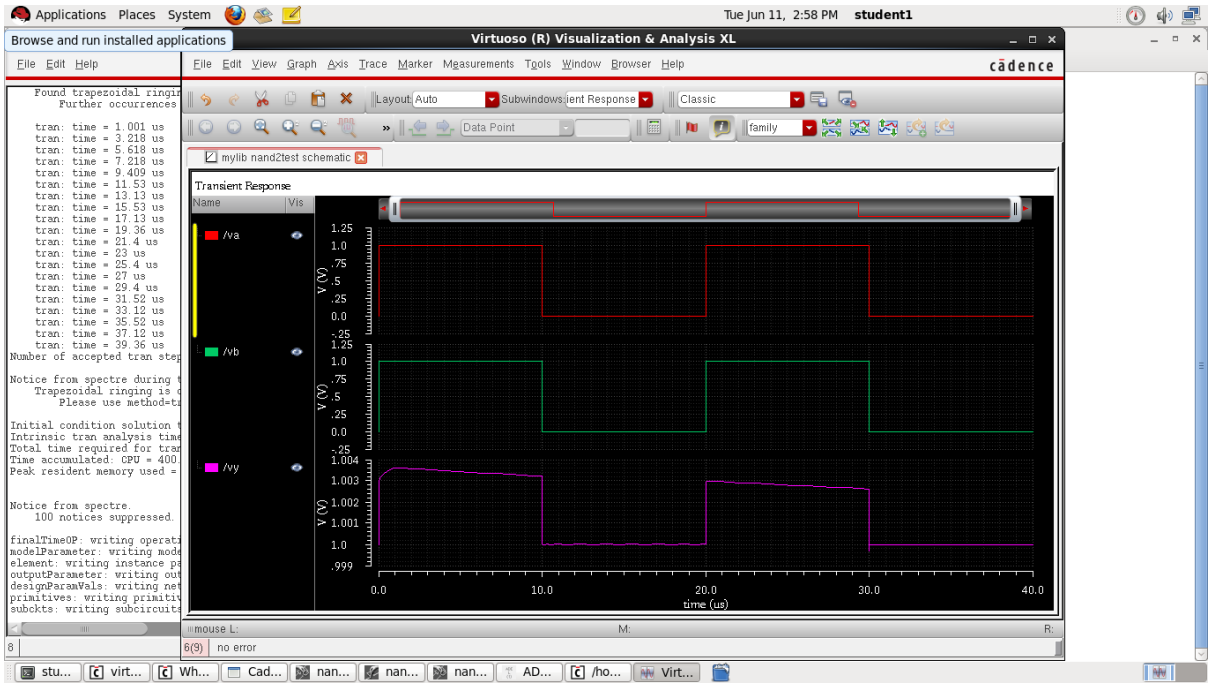


18)save it

19))Launch>ADE L

Output>**To be plotted**>select on simulation>click va vb vy in schematic window

Run



20)In mylib

- File>New>cell view
- Enter cell view: **xor2**
- Select OK

21) Create>Instance(shortcut-press **“I”**)

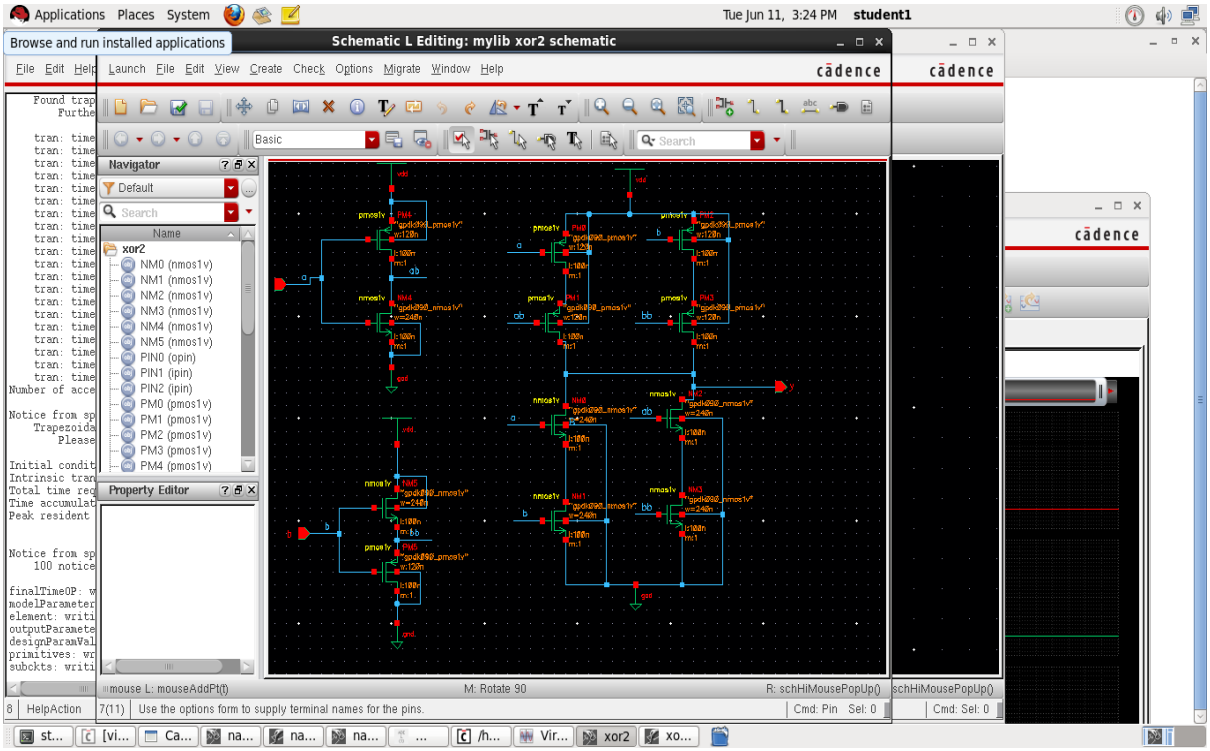
- Select the following and place it on the schematic Editing window each time.

Library	Cell view	Select
gpdk090	nmos1v	6
gpdk090	pmos1v	6
analogLib	vdd	3
analogLib	gnd	3

22)Set up the connections as shown

Press **“W”** for wire to connect the circuit

23) Create>wire name>(a b) (ab bb) (a b a b ab bb) (ab bb)>Save

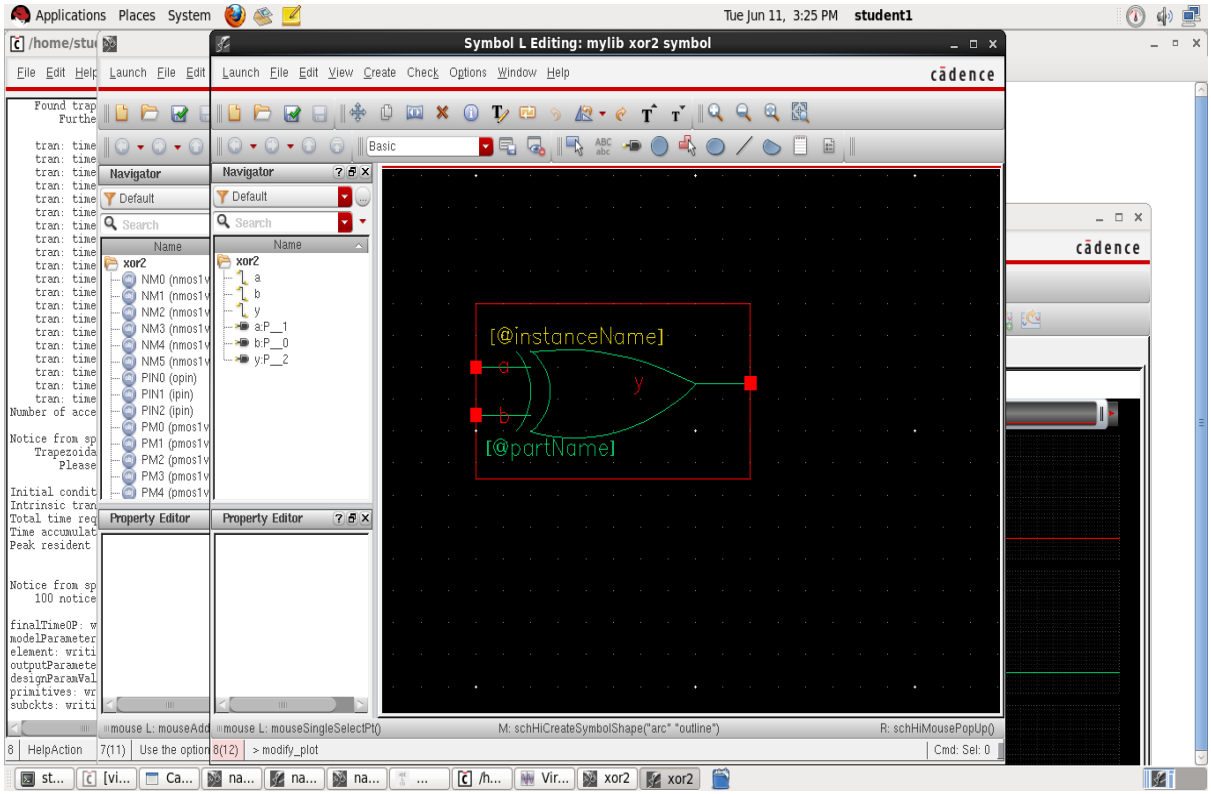


24) Create>Pins>output:y input:a b>Save

25)Create>**Cell view**>From Cell view>in Pop Up >OK>In another Pop Up>Select left pin:a b

right pin: y

26)Convert it into the following format using wire and create>shapes: arc



27)Save

28)Go back to **mylib**>click on **xor2**>File>New>cell view>xor2test>a new schematic window appears

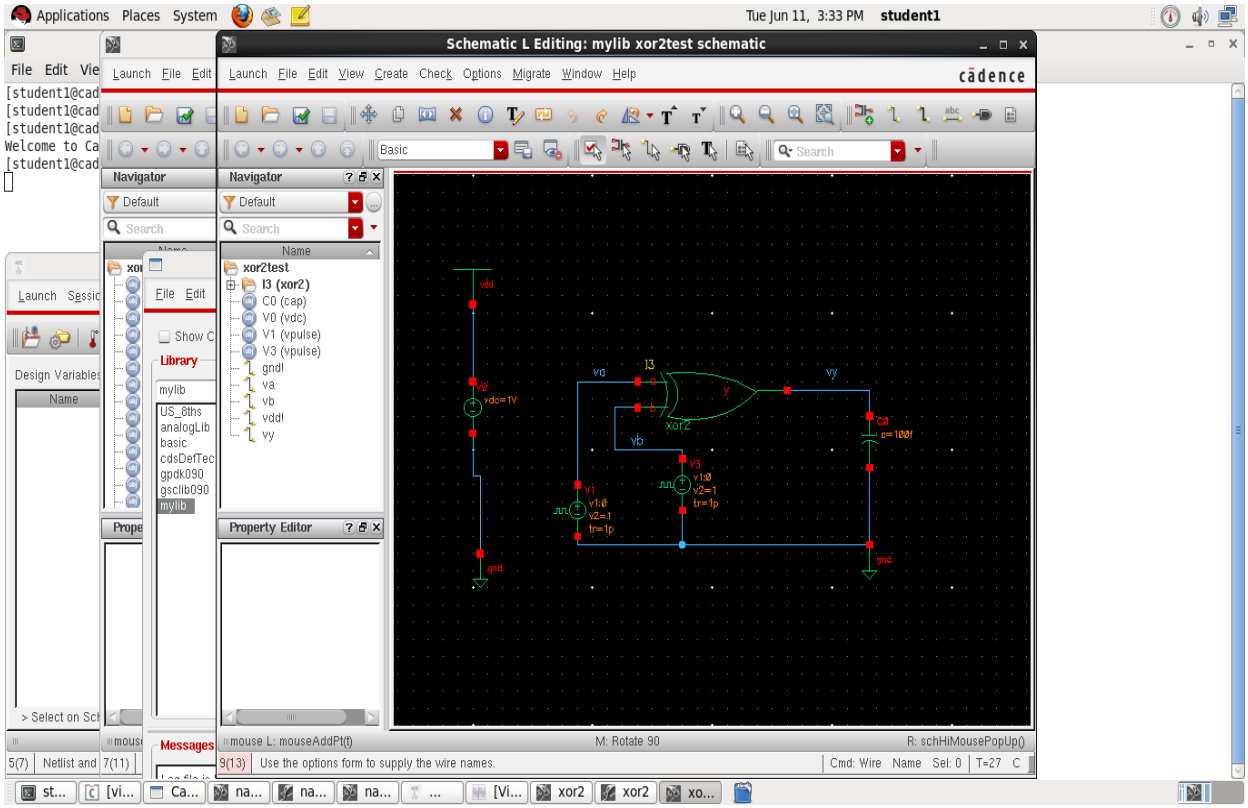
29)Create>instance

Library	Cell view	select
mylib	Xor2	1
analogLib	vdd	1
analogLib	gnd	2
analogLib	vdc	1
analogLib	vpulse	2
analogLib	cap	2

30)Set up the connections as shown

Press **“W”** for wire to connect the circuit

31) Create>wire name>va vb vy>Save



32))Launch>ADE L

Analyses >choose>trans>give stop:20n>OK

33)Again in ADE L

Output>**To be plotted**>select on simulation>click va,vb, vy in schematic window

Run

SCHEMATIC SYMBOL AND SIMULATION OF 1Bit Full Adder

STEPS:

34)In mylib

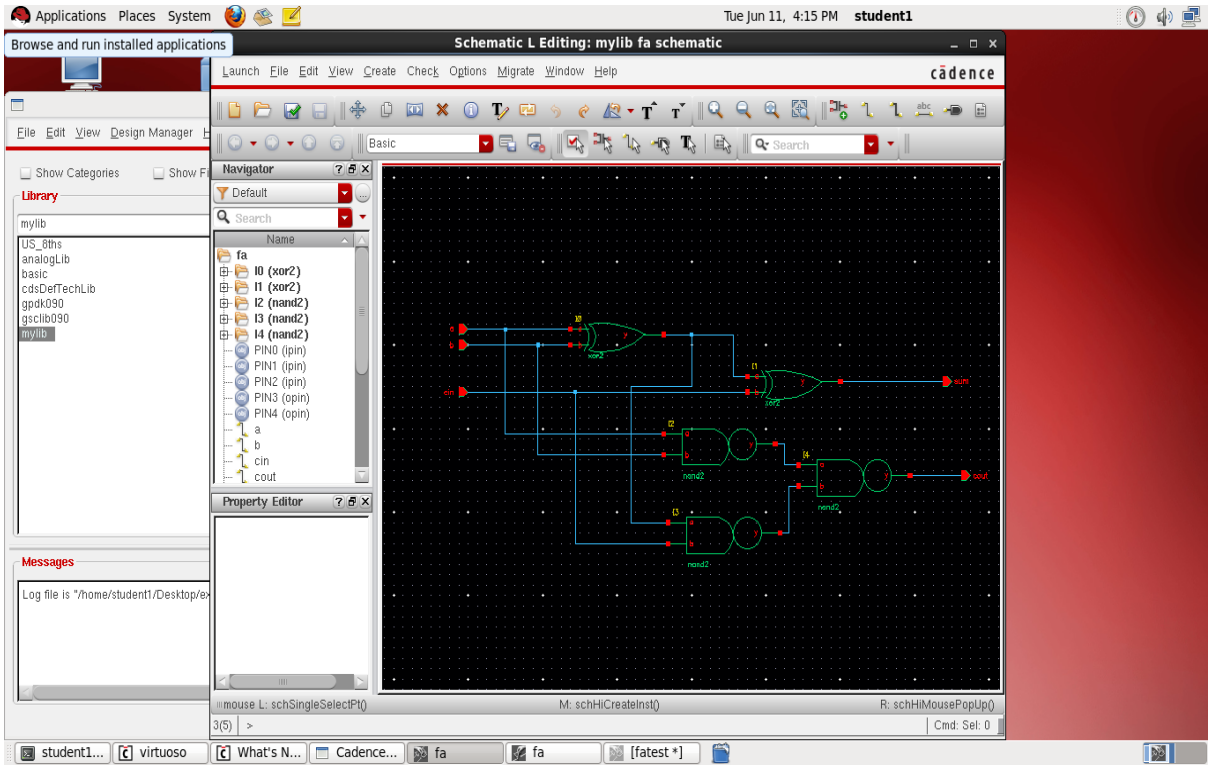
- File>New>cell view
- Enter cell view: **fa**
- Select OK

35)Create>Instance(shortcut-press **"I**")

Select the following and place it on the schematic Editing window each time

Library	Cell view	Select
mylib	xor2	2
mylib	nand2	2

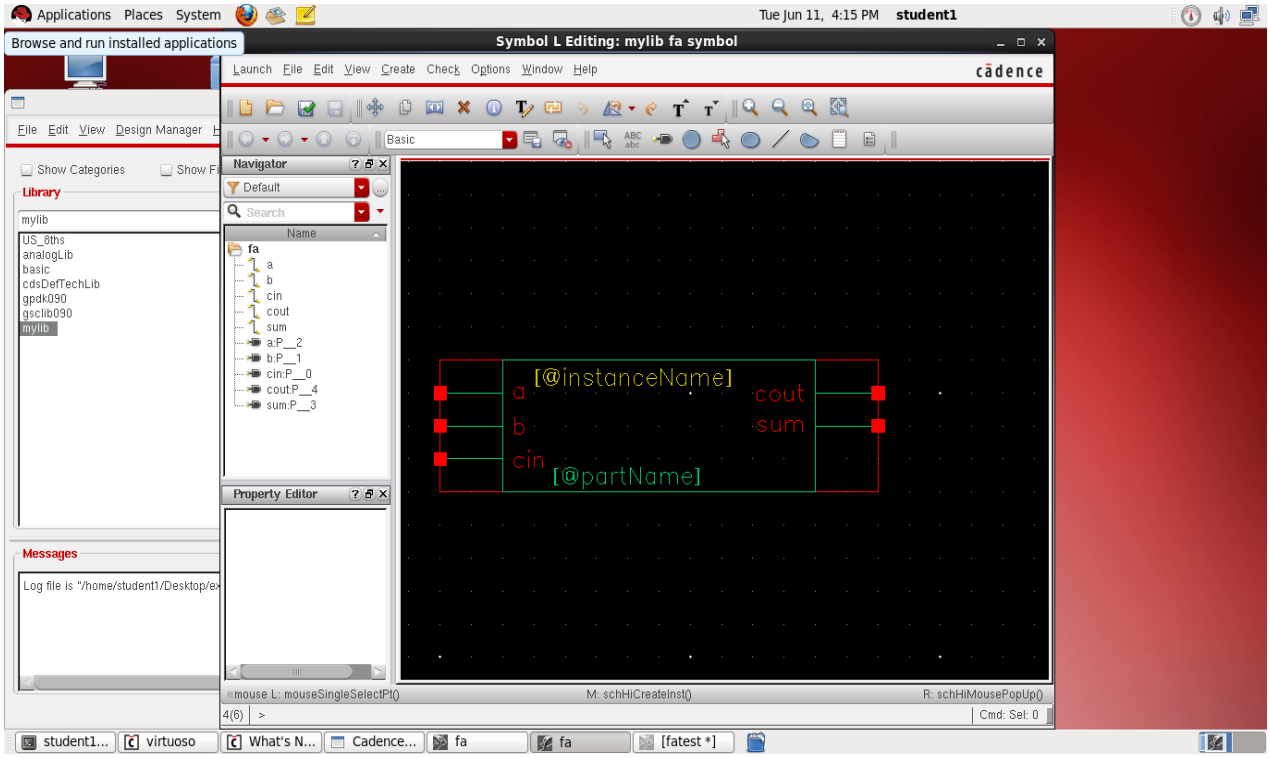
36)Create>pins>a b cin(input) , sum cout(output)>Save



37)Create>**Cell view**>From Cell view>in Pop Up >OK>In another Pop Up>Select left pin:a b cin

right pin: sum cout

38)Convert it into the following format using wire



39)Save

40)Go back to **mylib**>click on **fa**>File>New>cell view>fatest>a new schematic window appears

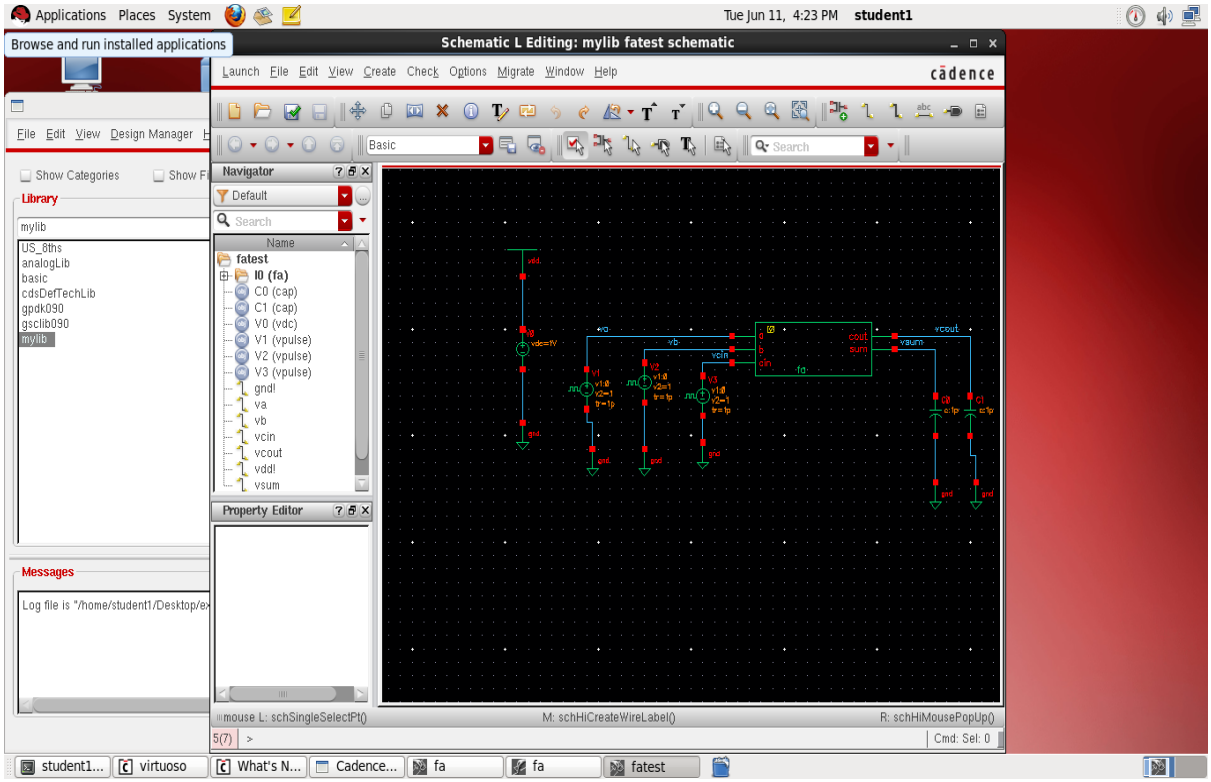
41)Create>instance

Library	Cell view	Select
mylib	fa	1
analogLib	vdd	1
analoglib	gnd	6
analoglib	vpulse	3
analogLib	cap	2
analoglib	vdc	1

42)Set up the connections as shown

Press **"W"** for wire to connect the circuit

43) Create>wire name>va vb vcin vsum vcout>Save



44))Launch>ADE L

Analyses >choose>trans>give stop:20n>OK

45)Again in ADE L

Output>**To be plotted**>select on simulation>click va,vb,vcin,vsum,vcout in schematic window

Run