STEPS TO IMPLEMENT DESIGN OF 2-AND GATE USING PASS TRANSISTOR USING CADENCE TOOL

STEP-1:**LIBRARY CREATION**

1)Open oracle VM virtual box

2)Click on start

3)Right click on workspace, select **open in terminal**

4)Type the commands

mkdir <any name> (ENTER)

cd <any name> (ENTER)

source /usr/software/gpdk090 (ENTER)

virtuoso (ENTER)

EXPLANATION:

mkdir: This command is used to create a new directory (folder) within the current directory.

cd: Short for "**change directory**," this command is used to navigate between directories. For example, cd folder_name would move you into the directory named "folder_name."

virtuoso: Virtuoso is a widely-used tool within Cadence for electronic design automation (EDA). It's primarily used for designing and simulating integrated circuits (ICs) and electronic systems. It includes various modules for schematic capture, layout editing, simulation, and more.

5)virtuoso tab appears

6)In virtuoso tab

- File>New>Library>mylib(give any name)>select Attach library to technology>Ok
- Select **gpdk090>Ok**
- Again in Virtuoso tab
  Tools>Library Manager>mylib

STEP-2:**LIBRARY MANAGING(SET UP CONNECTIONS AND ADD VALUES)**

7)In mylib

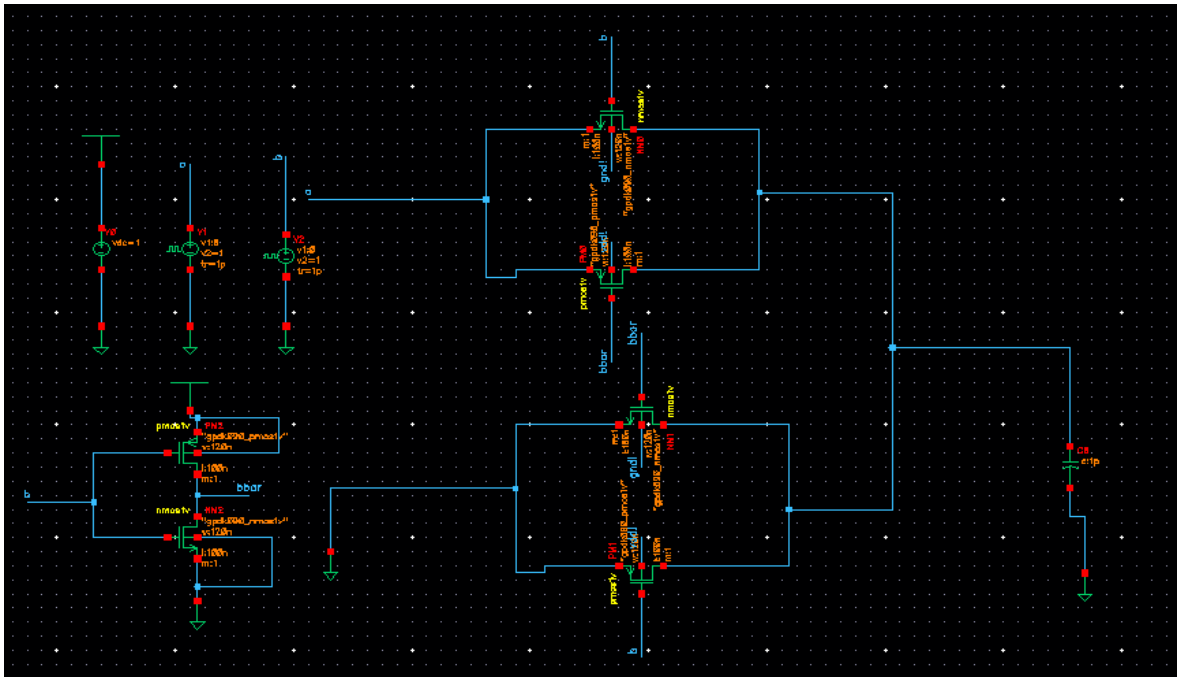
- File>New>cell view
- Enter cell view: **and2**
- Select OK> A schematic tab appears

8)Create>Instance(shortcut-press **"I**") >

- Select the following and place it on the schematic Editing window each time.
- Select vdc twice.

Library	Cell	View
gpdk090	nmos1v(3)	symbol
gpdk090	pmos1v(3)	symbol
analogLib	vdc	symbol
analogLib	vpulse(voltage2 – 1V; period – 10u s; pulse width -5u s; Delay,rise,fall time – 1p s)	symbol
analogLib	vpulse(voltage2 – 1V; period – 20u s; pulse width -10u s; Delay,rise,fall time – 1p s)	symbol
analogLib	Vdd(2)	symbol
analogLib	gnd(6)	symbol
analogLib	cap	symbol

9)Set up the connections as show, Press **"W"** for wire to connect the circuit



10)To name the wires Create > Wire name > provide the names as shown in diagram above

Save (on the top left corner) > check virtuoso tab to make sure everything is correct, if correct it shows “schematic saved”

11)Launch> ADE L

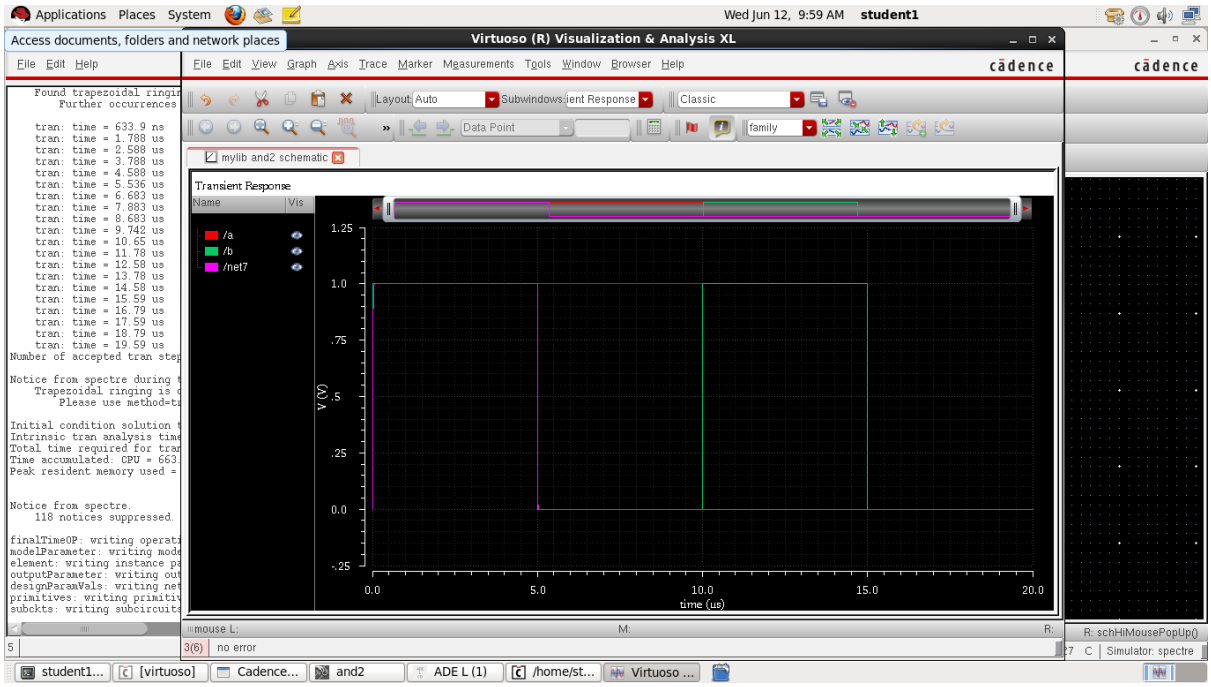
12)In ADE L

Analyses > Choose > Choose **DC;** In DC analysis (same tab) stop time 20u and click OK

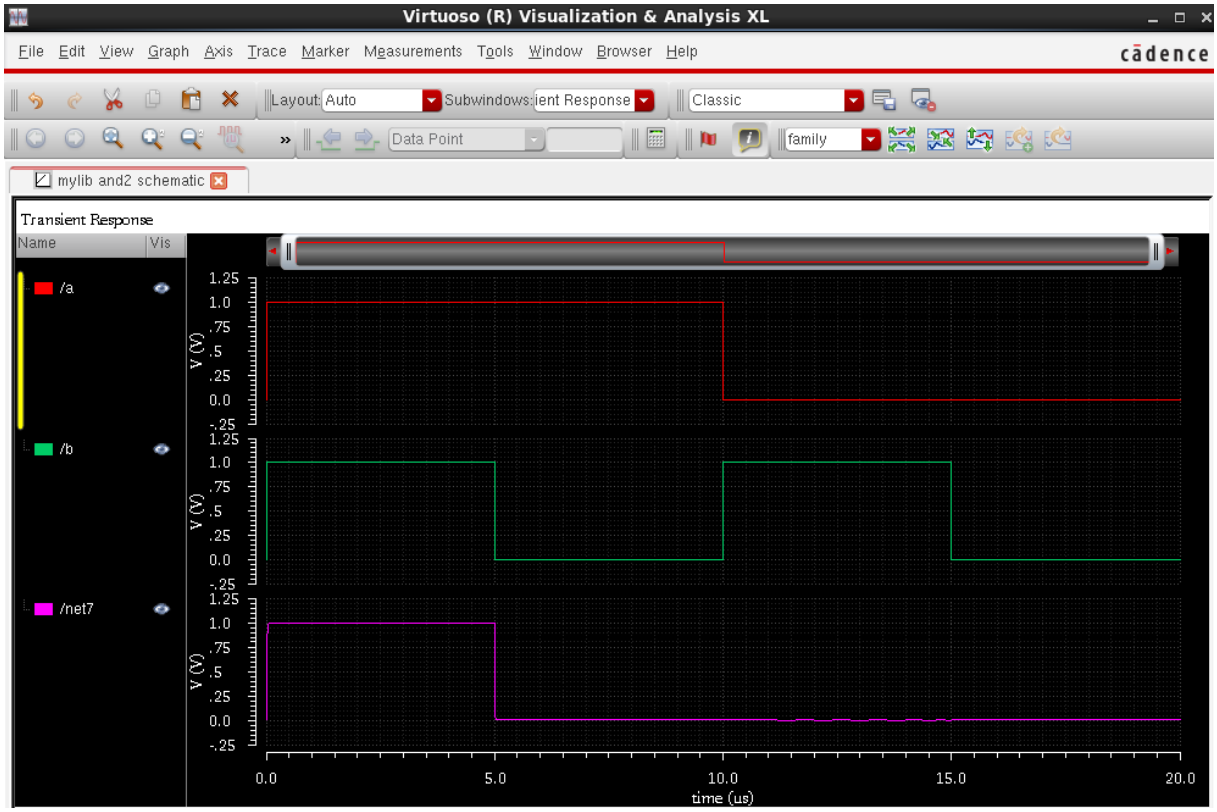
Choose nets a,b and the output line on schematic then you can see those in ADE L tab > outputs

13) On ADE L window select Simulation> Netlist and Run

14) if the simulation is successful the graph tab appears and the results can be viewed in graph tab



To check output graphs separately, click on split all strips on top right side of the panel



The schematic and simulation of 2 and gates using pass transistor is successfully implemented.