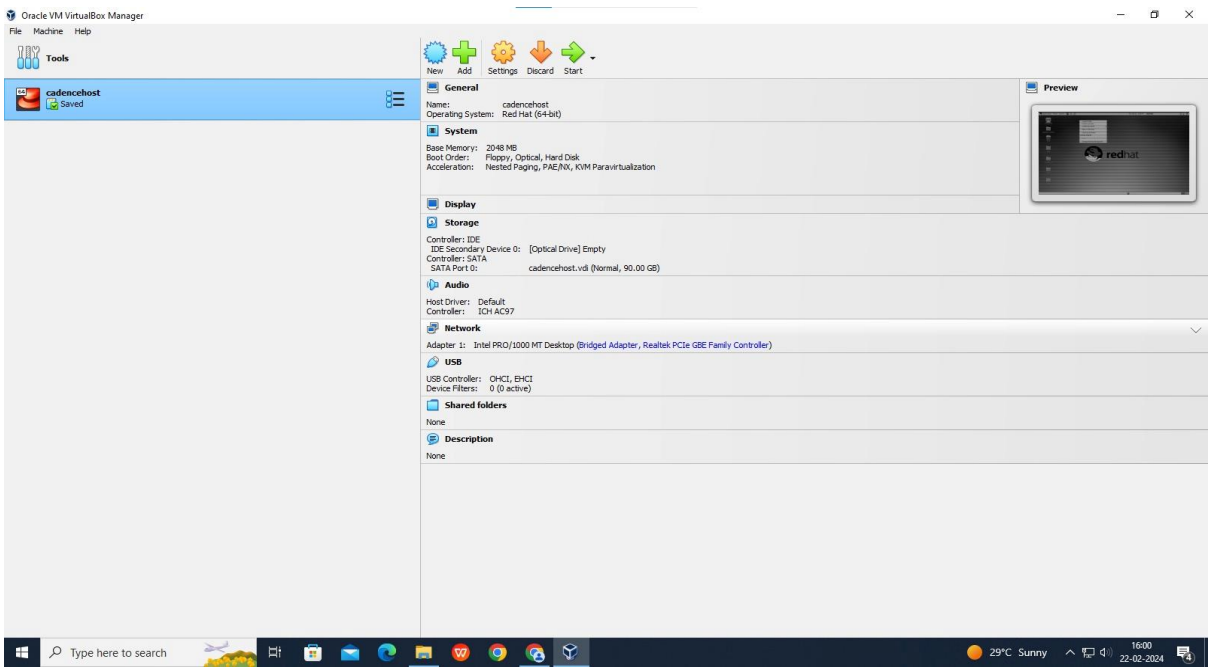
SCHEMATIC LAYOUT, DRC AND LVS OF CMOS INVERTER

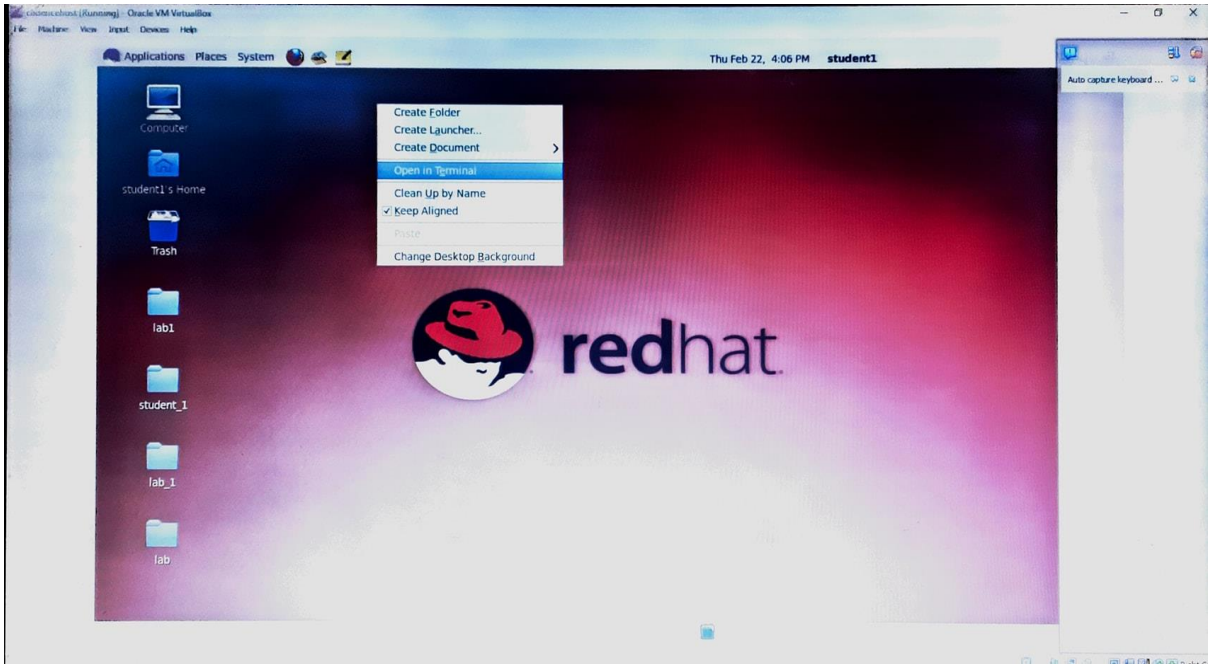
STEPS:

1)Open oracle VM virtual box

2)Click on start



3)Right click on workspace, select **open in terminal**



4)Type the commands

mkdir <any name> (ENTER)

cd <any name> (ENTER)

pwd (ENTER)

source /usr/software/gpdk090 (ENTER)

virtuoso & (ENTER)

EXPLANATION:

mkdir: This command is used to create a new directory (folder) within the current directory.

cd: Short for "**change directory**," this command is used to navigate between directories. For example, cd folder_name would move you into the directory named "folder_name."

pwd: Short for "**print working directory**," this command shows you the full path of the current directory you are in.

virtuoso: Virtuoso is a widely-used tool within Cadence for electronic design automation (EDA). It's primarily used for designing and simulating integrated circuits (ICs) and electronic systems. It includes various modules for schematic capture, layout editing, simulation, and more.

5)virtuso tab appears

6)In virtuoso tab

- File>New>Library>mylib(give any name)>select Attach library to technology>Ok
- Select **gpdk090>Ok**

Again in Virtuoso tab

- Tools>Library Manager>mylib

7)In mylib

- File>New>cell view
- Enter cell view: **inverter**
- Select OK

8)Create>Instance(shortcut-press **"I**")

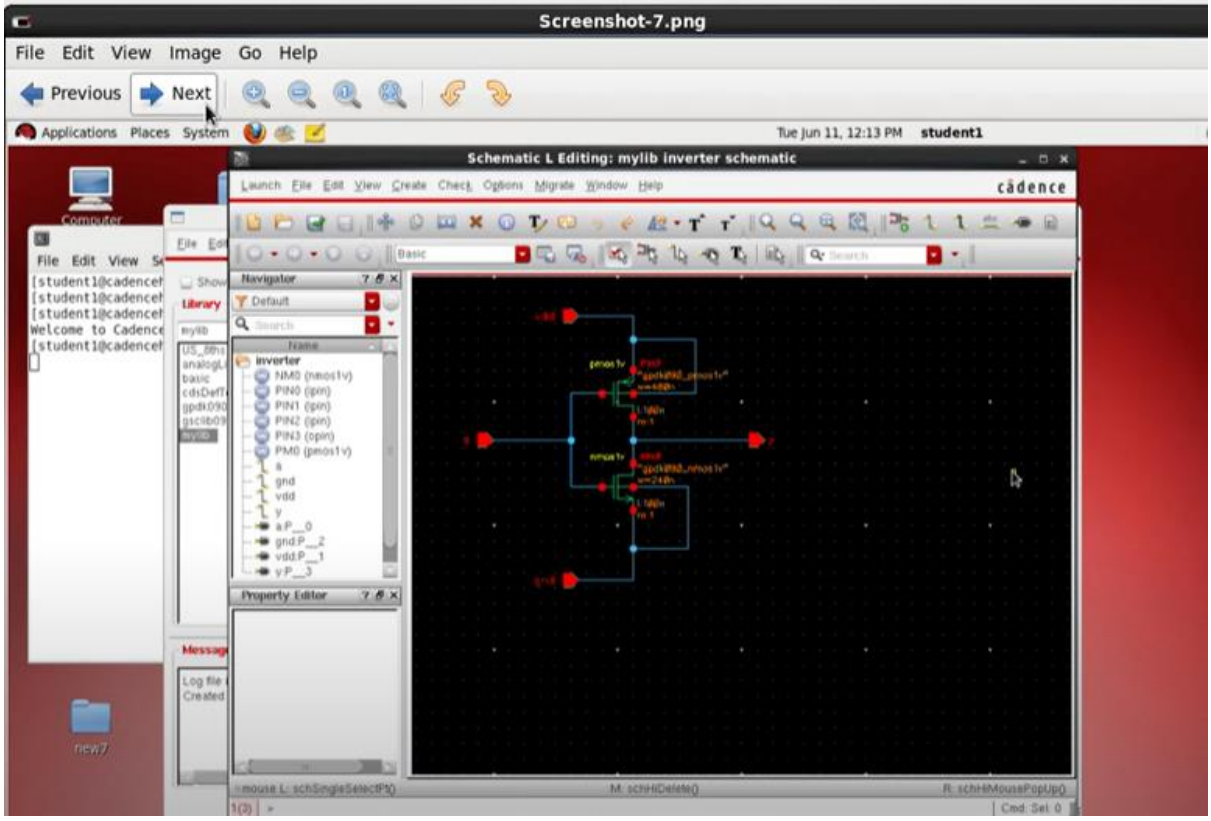
- Select the following and place it on the schematic Editing window each time.

Library	Cell view	Select
gpdk090	nmos1v	Hide
gpdk090	pmos1v	Hide

9)Set up the connections as shown

Press **“W”** for wire to connect the circuit

10)Create>pins>vdd a gnd(input)>y(output)>Save

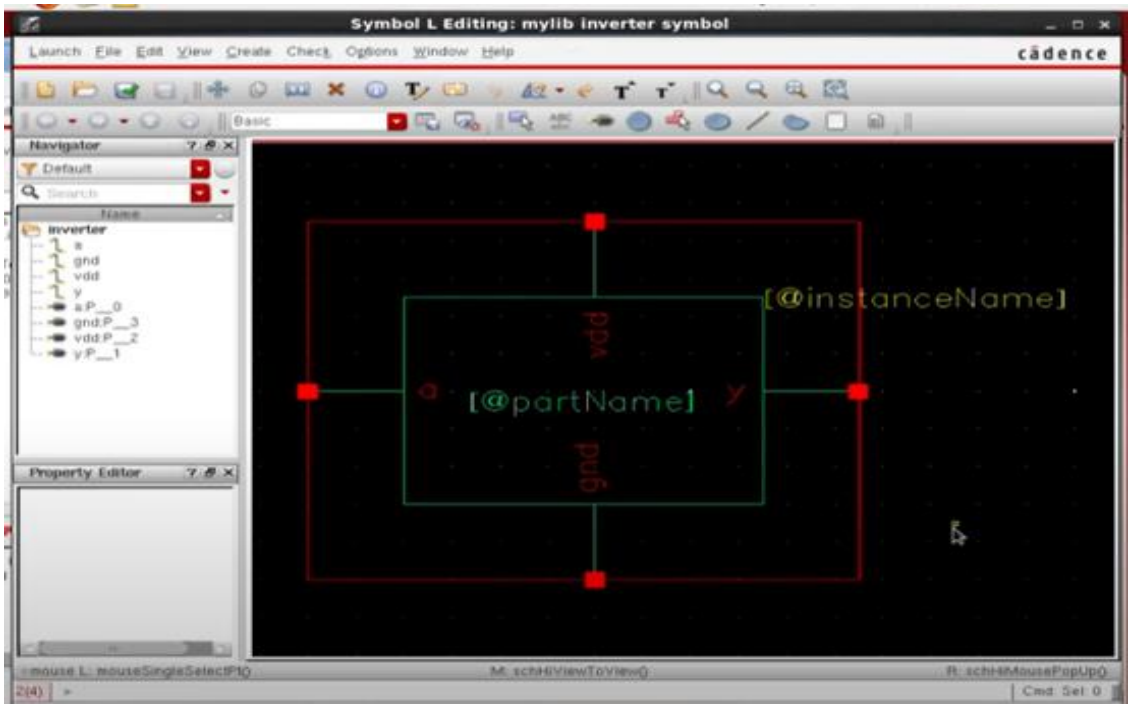


11)Create>**Cell view**>From Cell view>in Pop Up >OK>In another Pop Up>Select left pin:a

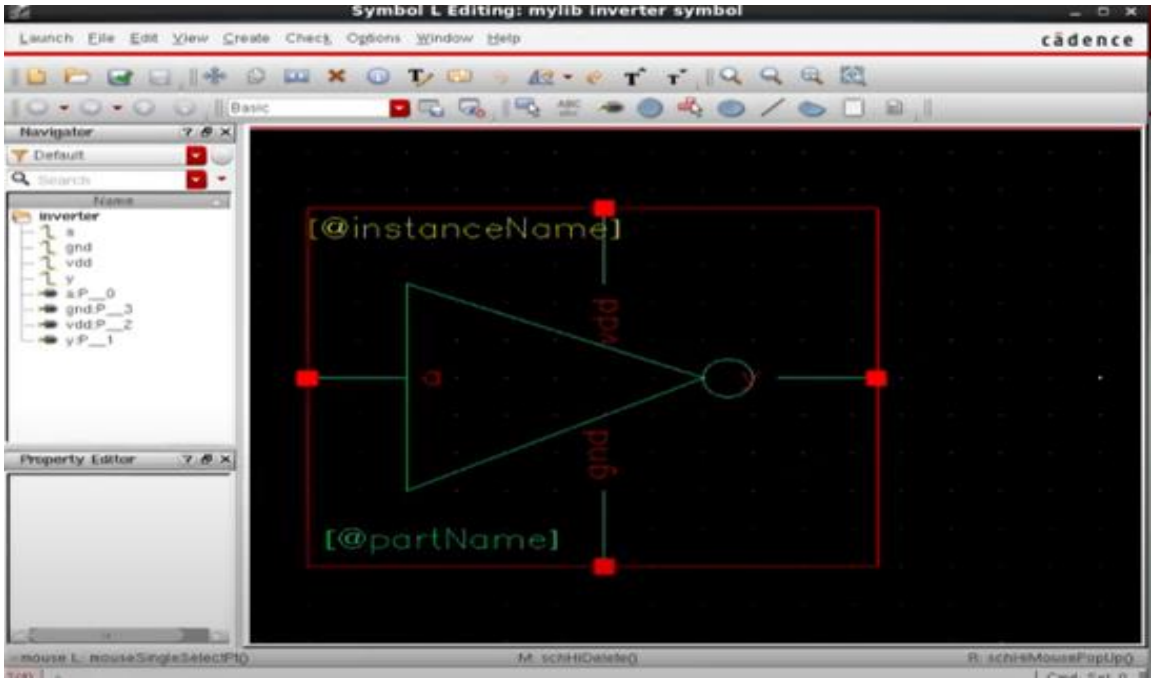
right pin:y

top pin:vdd

bottom pin:gnd



12)Convert it into the following format using wire and create>shapes:circle



13)Save

14)Go back to **mylib**>click on **inverter**>File>New>cell view>invertertest>a new schematic window appears

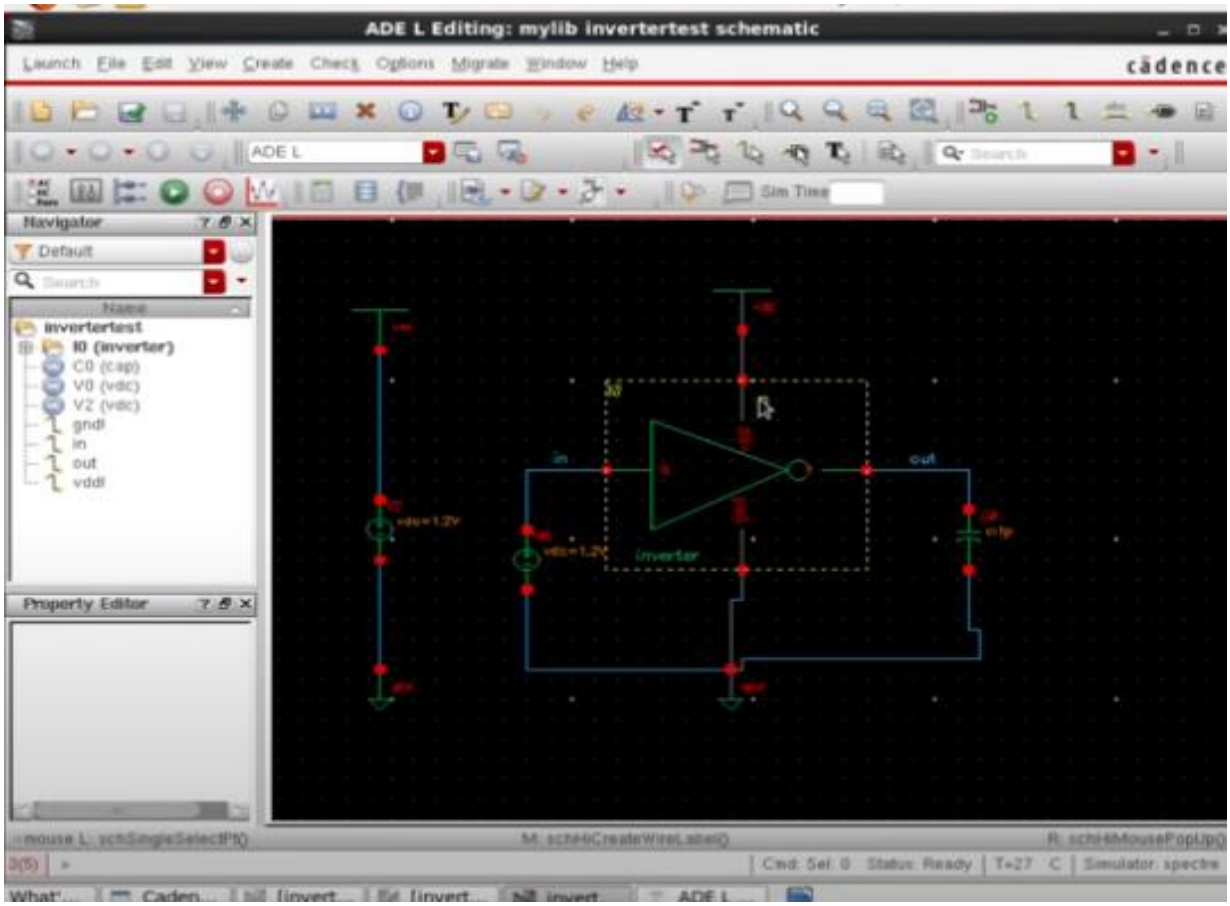
15)Create>instance

Library	Cell view	Value

mylib	inverter	hide
analogLib	vdc	1.2V
analogLib	cap	1pF
analogLib	vdd	hide
analogLib	gnd	hide

16)Set up the connections as shown

Press **"W"** for wire to connect the circuit



17)save it

[THE ABOVE STEPS ARE SIMILAR TO SIMULATION OF CMOS INVERTER]

For LAYOUT DRC AND LVS(go back to virtuoso tab > tools > library manager):

18)In my lib > inverter > (view) create a new file by clicking

File > new > cell view

Cell name – Inverter ; View - Layout > OK

A new layout tab appears

19) In the layout tab > press I > library > gpdk090

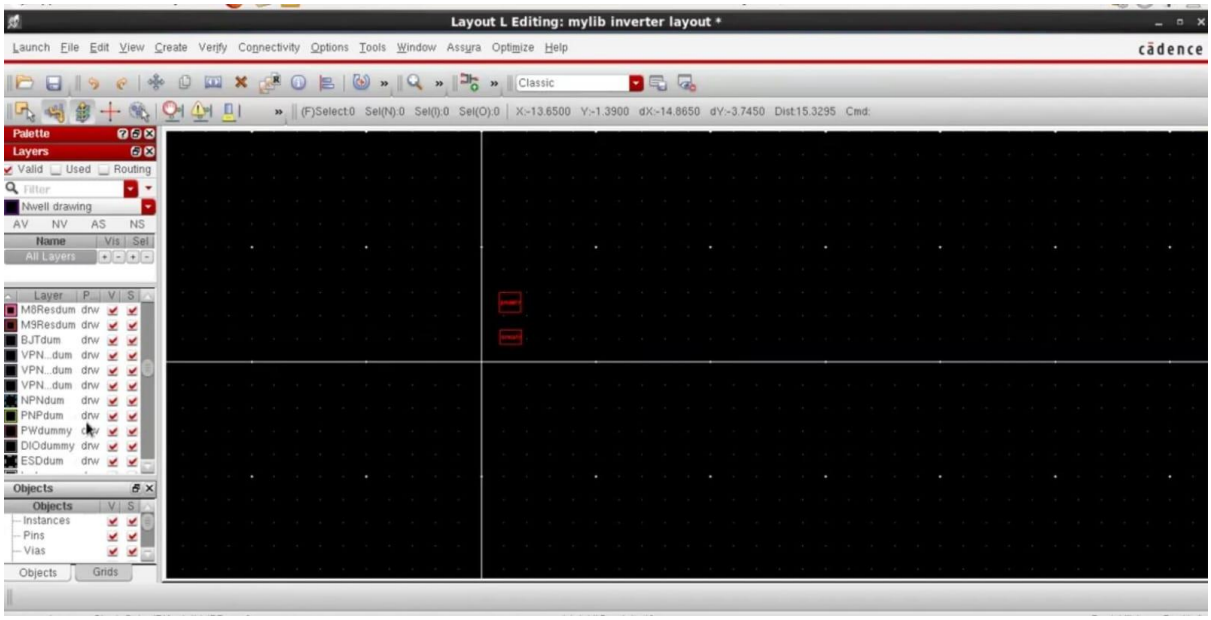
Cell > nmos1v

(scroll down) total width – 240 n M > Hide > (place the transistor on layout)

20) Again press I > library > gpdk090

Cell > pmos1v

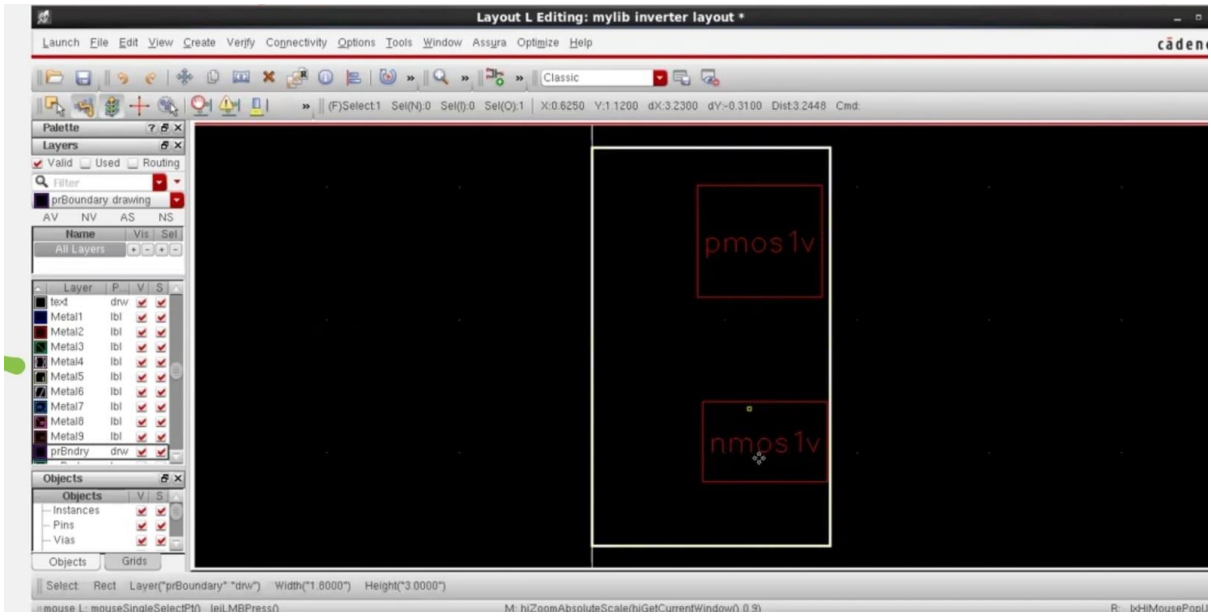
(scroll down) total width – 480 n M > Hide > (place the transistor on layout)



21) From the layer select window(on left) > select prBndry [drw] layer

Select create (On top) > Shape > Rectangle(draw it on left top part of schematic) > escape and then click on rectangle and choose edit properties from top panel – Give values as shown below

The rectangle looks like this later

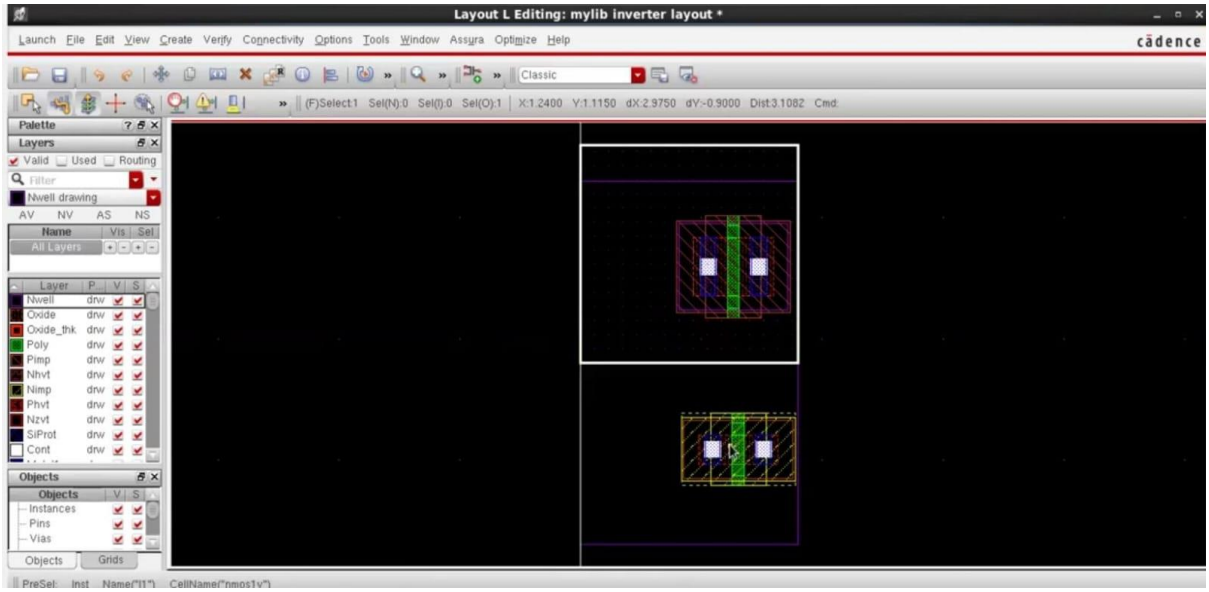


22) (If you want to see different layers)

Options > Display > Stop – 10 (Indicates number of layers)

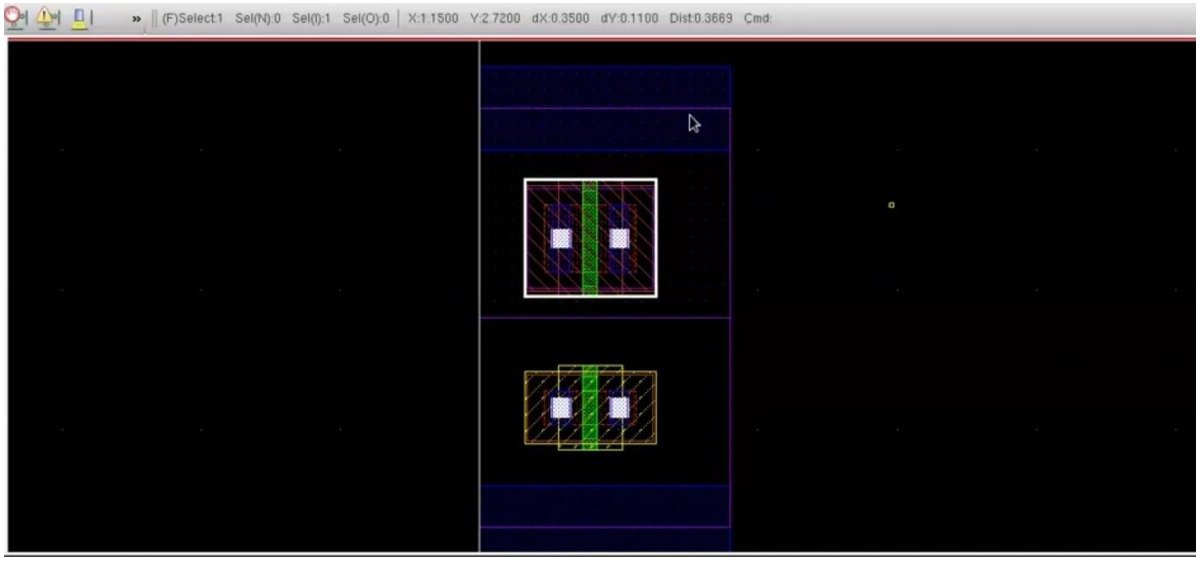
>Display Controls > Enable Pin names > OK

23) From layer select window > Nwell[drw] > Create > Shape > Rectangle(draw it on left top part of schematic) > escape and then click on rectangle and choose edit properties from top panel – Give values as shown below



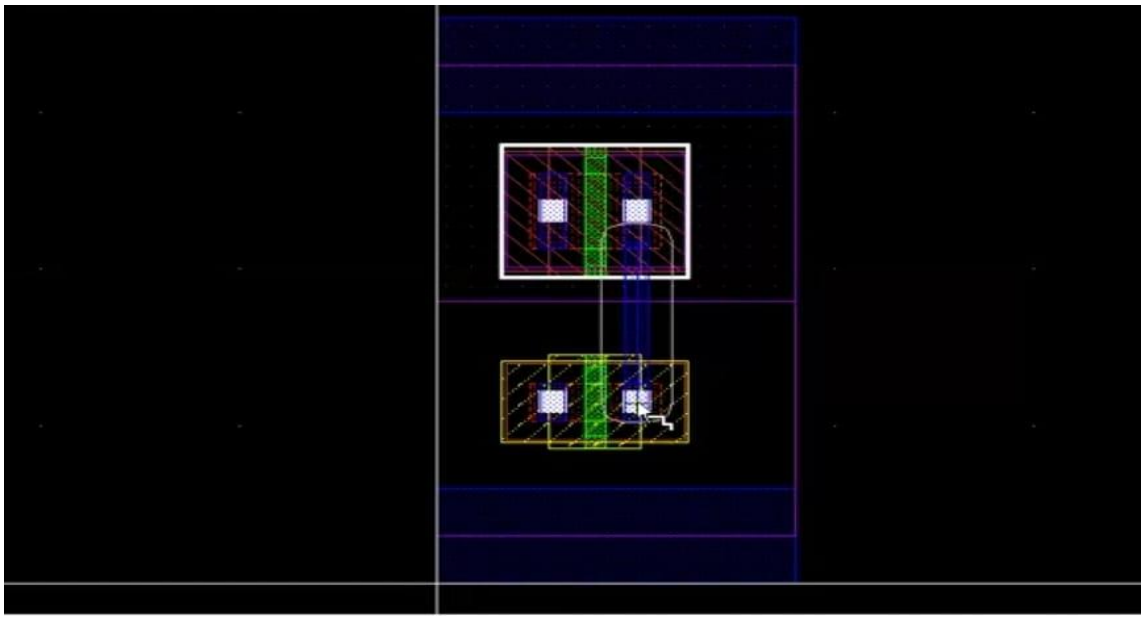
24) Make sure both the paths of resistor are in same line - so that you can create a path later

25) From layer select window > Select Metal1 [drw] > Select > Shape > Rectangle > draw two rectangle with values below



26) Join the drain of PMOS and NMOs by selecting

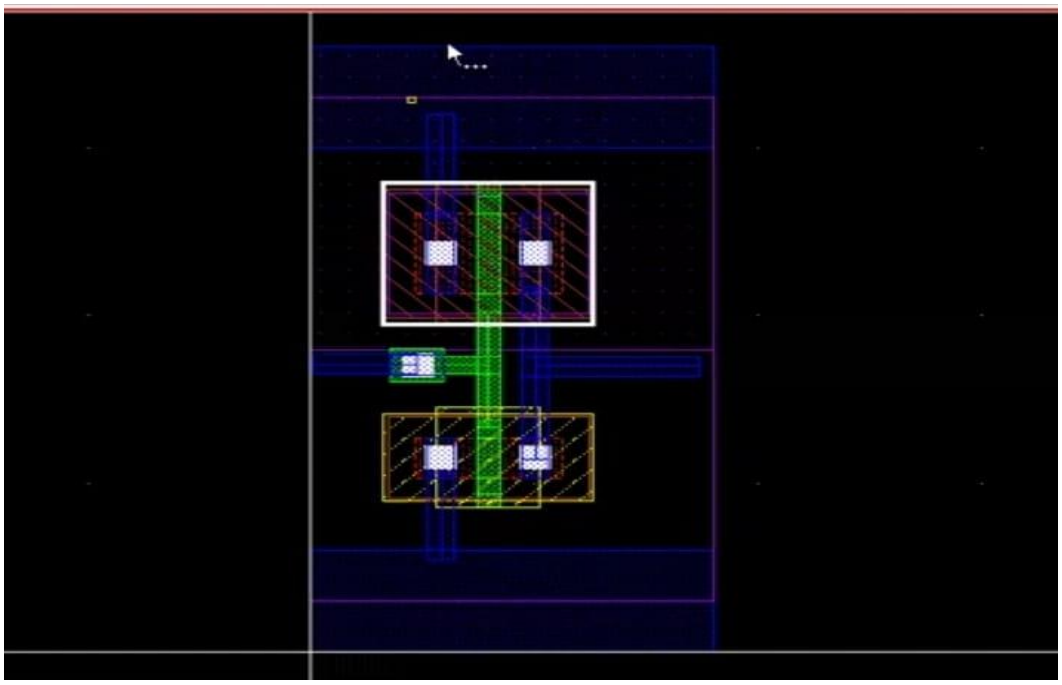
Create > Shape > Path , Zoom in to the figure and join the paths as shown in figure



27) Similarly join the source of nmos to ground and source of nmos to vdd and also create a extented path for output

For creating poly path; Create > Via >Via definition – M1_Pov (rotate and place), and using poly [drw] from layer window create another path to join transistors

And create paths as shown in the below figure

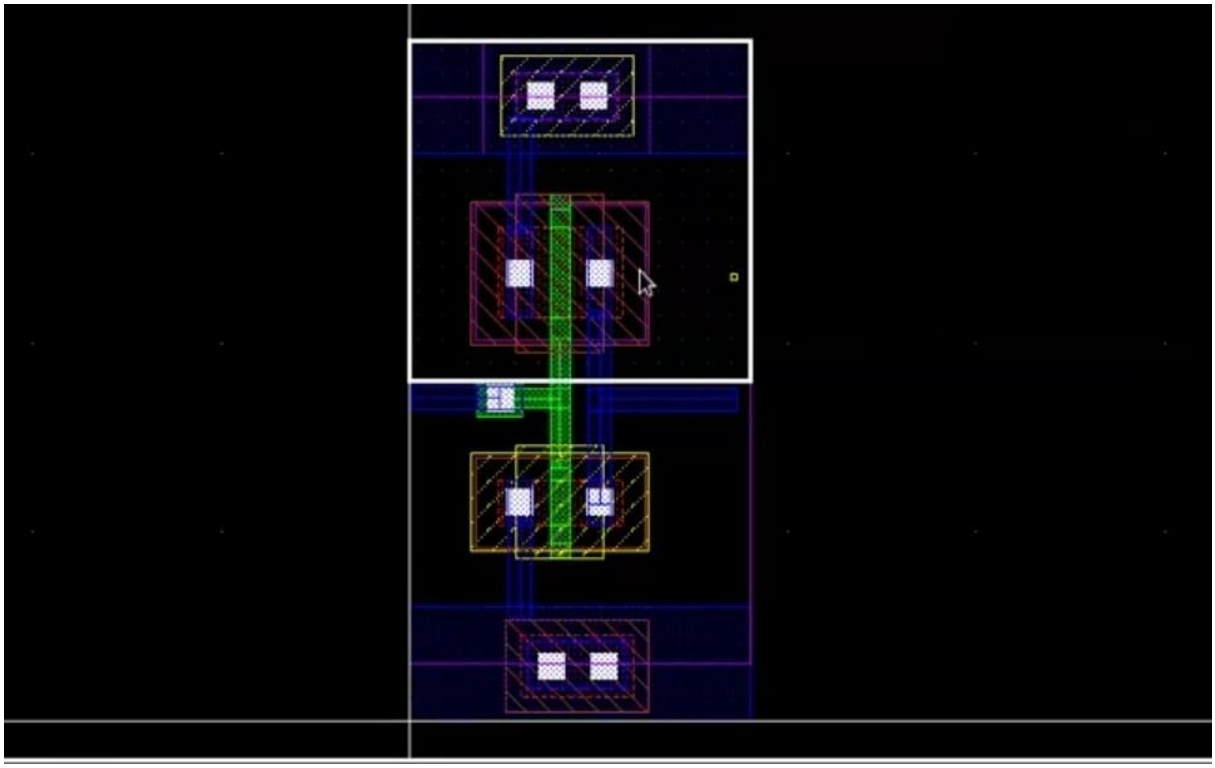


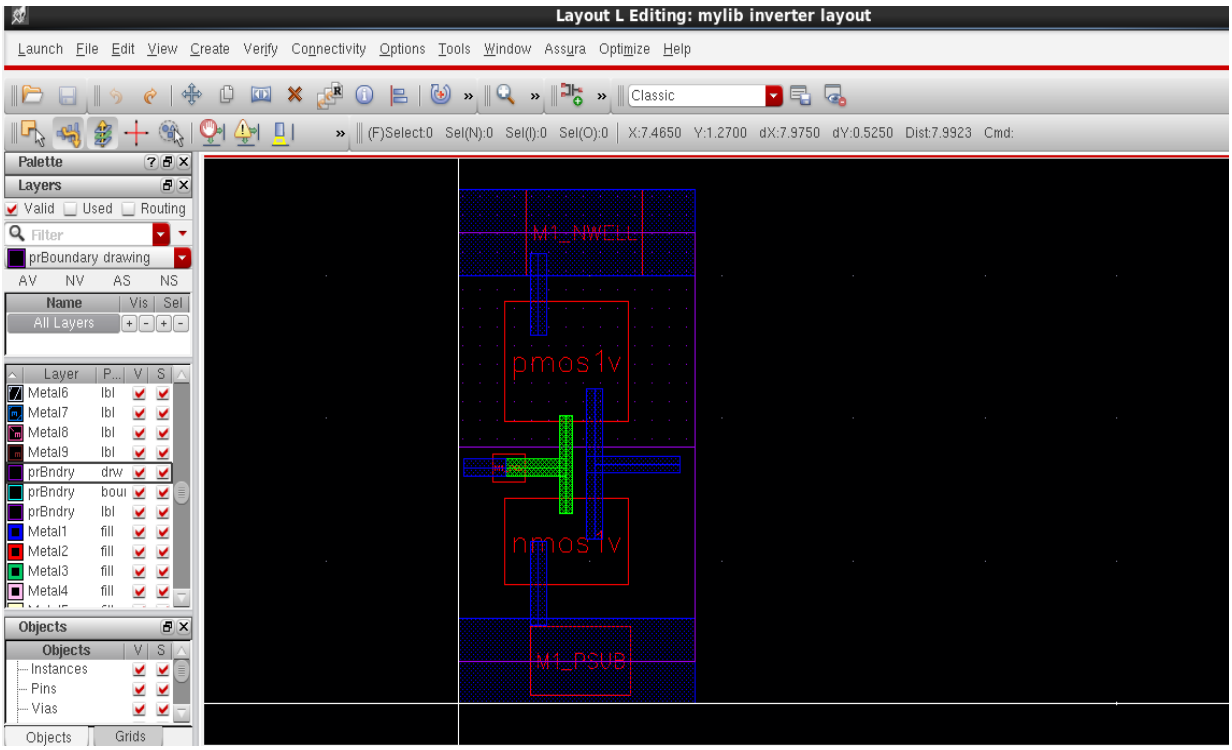
28) To create body contacts :

Create > Via > Via definition - M1_NWELL > 1Row, 2Columns > Hide

Create > Via > Via definition – M1_PSUB > 1Row, 2Columns > Hide

The final layout looks like this





29) To verify, Run a DRC(Design Rule Check)

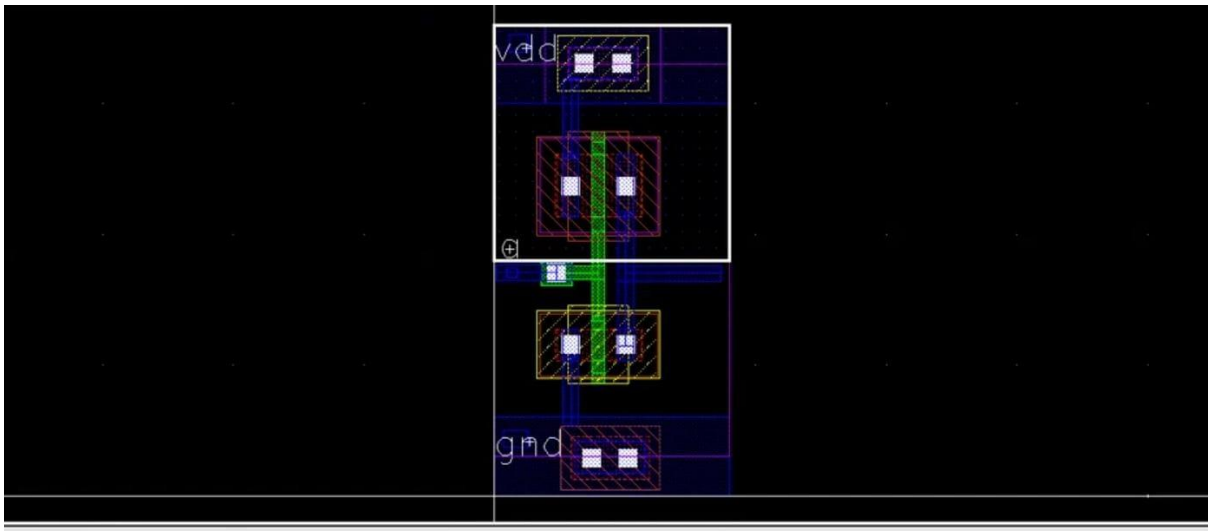
On layout tab > Assura > Run DRC > In DRC tab select Technology as gpdk090 > OK

30) After the DRC is complete a pop up appears- click yes

If there are no errors (No errors found) - Pop up message appears – click close

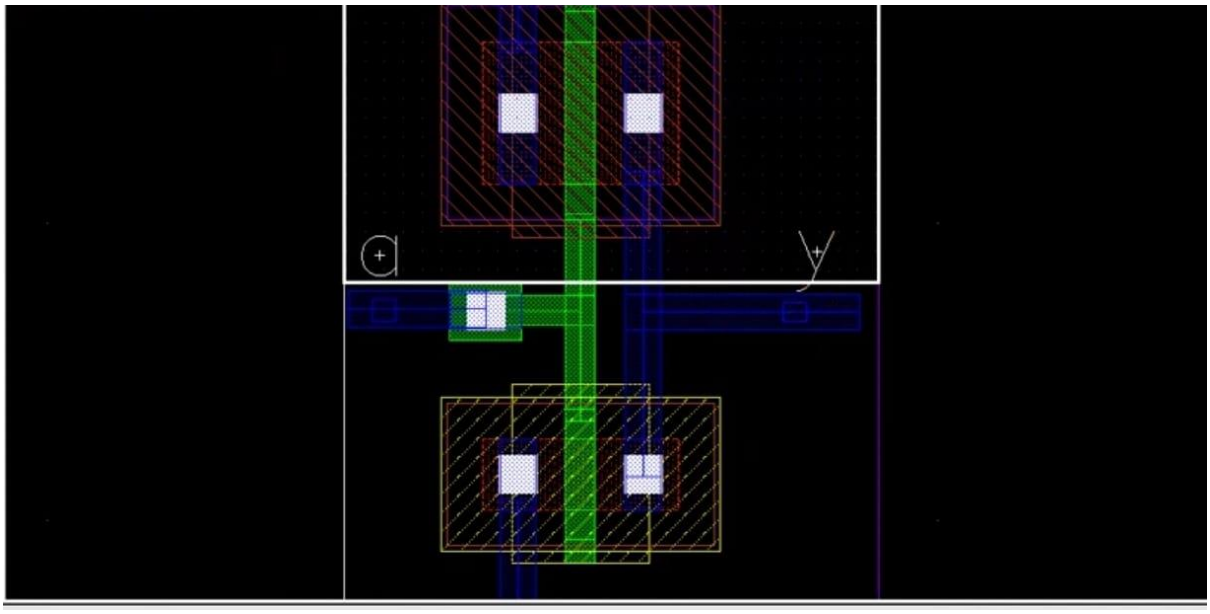
31) Create > Pin > Terminal name - a vdd gnd > Enable Display teminal name > Click on Display terminal name option > give Height as 0.2 > OK, and I/O TYPE should be input > Hide

Place your pins on layout as shown in diagram



31) Create Output Pins

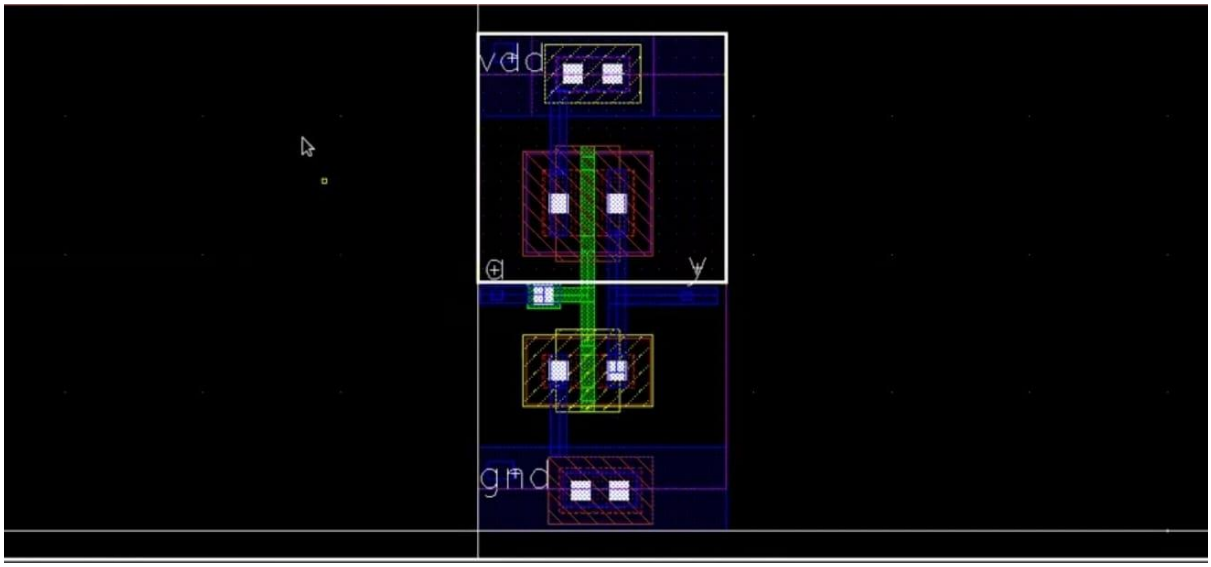
Create > Pin > Terminal name – y > Enable Display teminal name > Click on Display terminal name option > give Height as 0.2 > OK, and I/O TYPE should be Output > Hide



31) Assura > run DRC > OK

If there are no errors (No errors found) - Pop up message appears – click close

Final layout



32) To check if the layout and schematic are same

Assura > Run LVS > > In LVS tab select Technology as gpdk090 > OK > On pop-up > yes

If there are no errors, a pop-up appears stating the layout and schematic match > click yes

This completes the Layout , Layout and Schematic match of a CMOS inverter