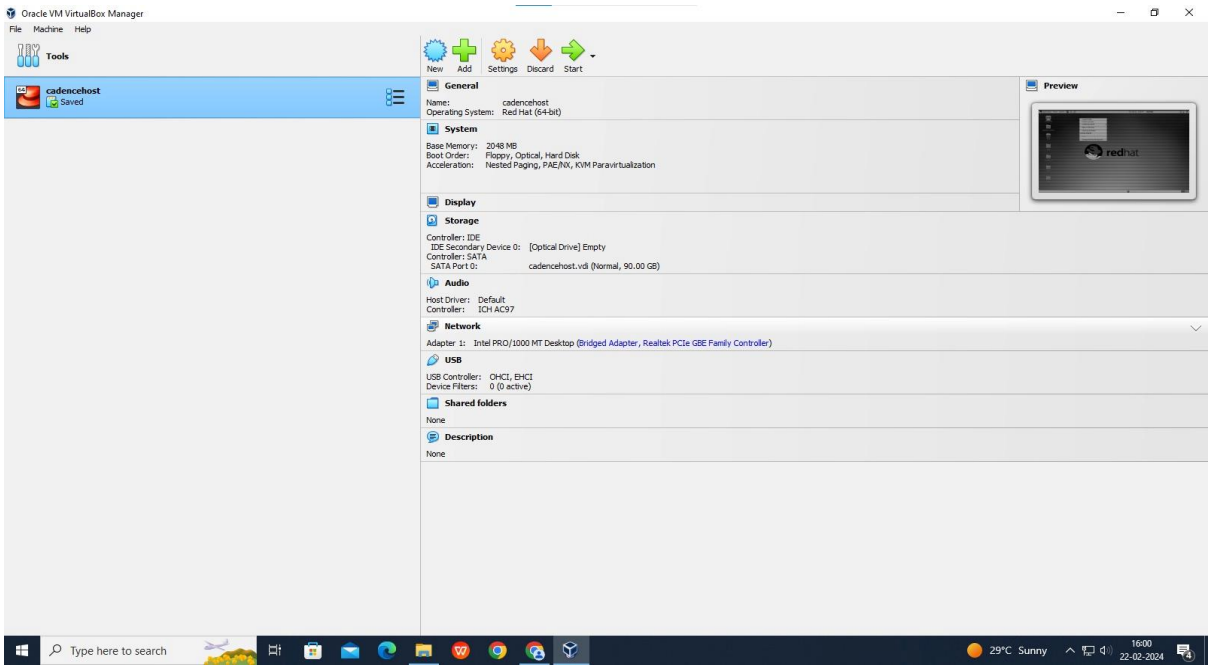
SCHEMATIC SYMBOL AND ANALOG SIMULATION OF CMOS INVERTER

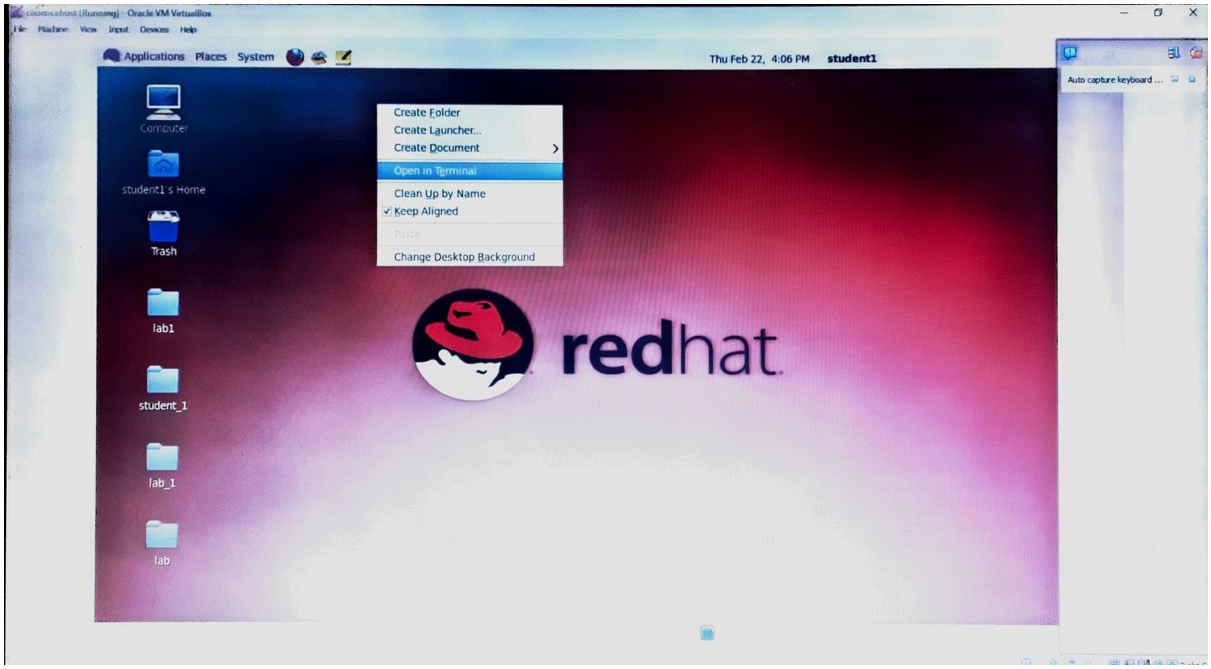
STEPS:

1)Open oracle VM virtual box

2)Click on start



3)Right click on workspace, select **open in terminal**



4)Type the commands

mkdir <any name> (ENTER)

cd <any name> (ENTER)

pwd (ENTER)

source /usr/software/gpdk090 (ENTER)

virtuoso & (ENTER)

EXPLANATION:

mkdir: This command is used to create a new directory (folder) within the current directory.

cd: Short for "**change directory**," this command is used to navigate between directories. For example, cd folder_name would move you into the directory named "folder_name."

pwd: Short for "**print working directory**," this command shows you the full path of the current directory you are in.

virtuoso: Virtuoso is a widely-used tool within Cadence for electronic design automation (EDA). It's primarily used for designing and simulating integrated circuits (ICs) and electronic systems. It includes various modules for schematic capture, layout editing, simulation, and more.

5)virtuso tab appears

6)In virtuoso tab

- File>New>Library>mylib(give any name)>select Attach library to technology>Ok
- Select **gpdk090>Ok**

Again in Virtuoso tab

- Tools>Library Manager>mylib

7)In mylib

- File>New>cell view
- Enter cell view: **inverter**
- Select OK

8)Create>Instance(shortcut-press **"I**")

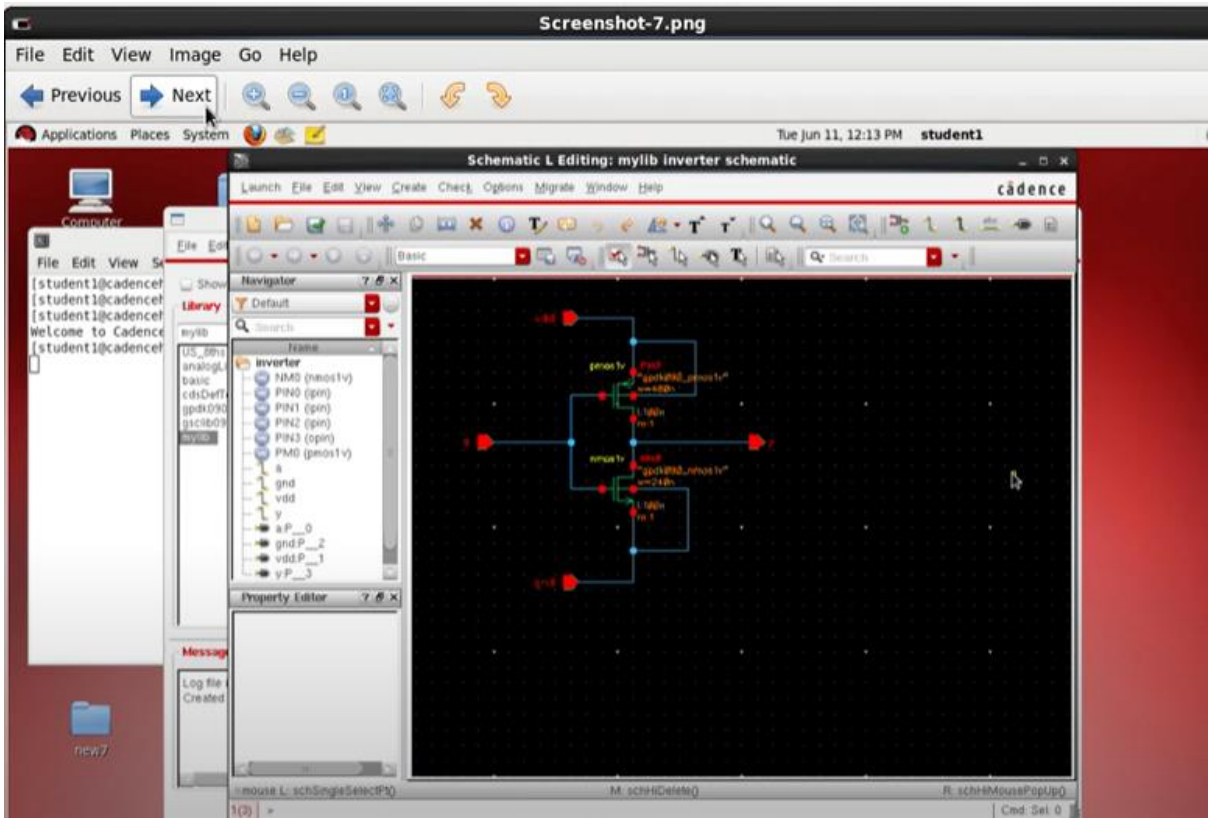
- Select the following and place it on the schematic Editing window each time.

Library	Cell view	Select
gpdk090	nmos1v	Hide
gpdk090	pmos1v	Hide

9)Set up the connections as shown

Press **“W”** for wire to connect the circuit

10)Create>pins>vdd a gnd(input)>y(output)>Save

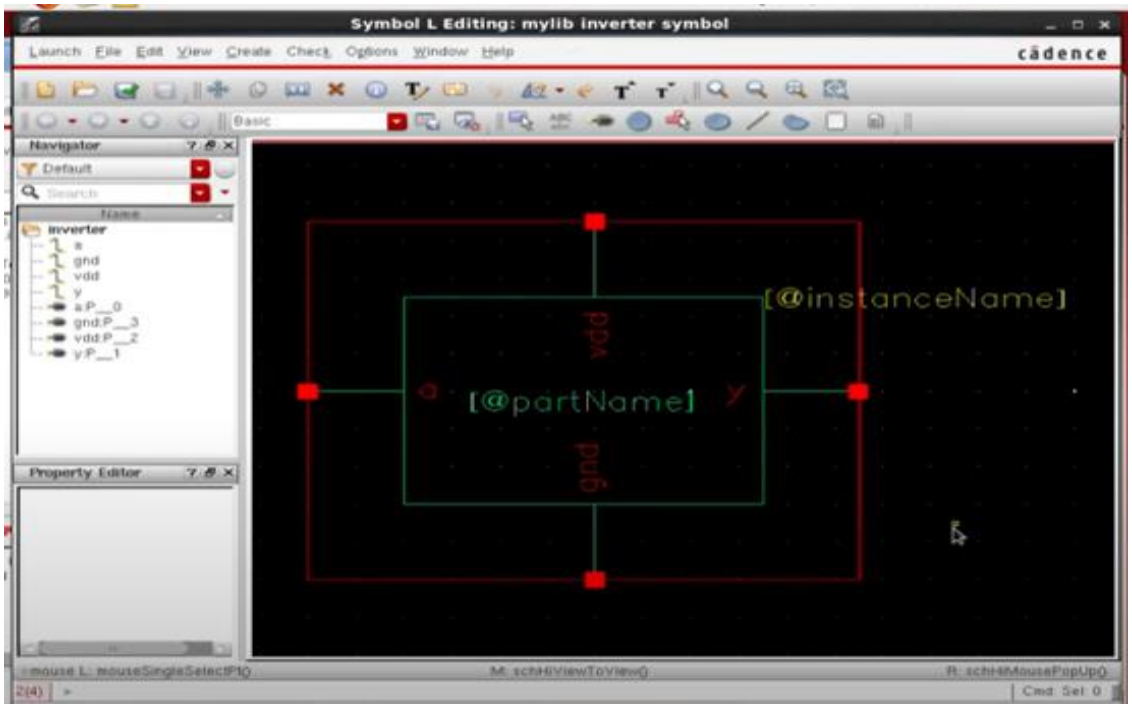


11)Create>**Cell view**>From Cell view>in Pop Up >OK>In another Pop Up>Select left pin:a

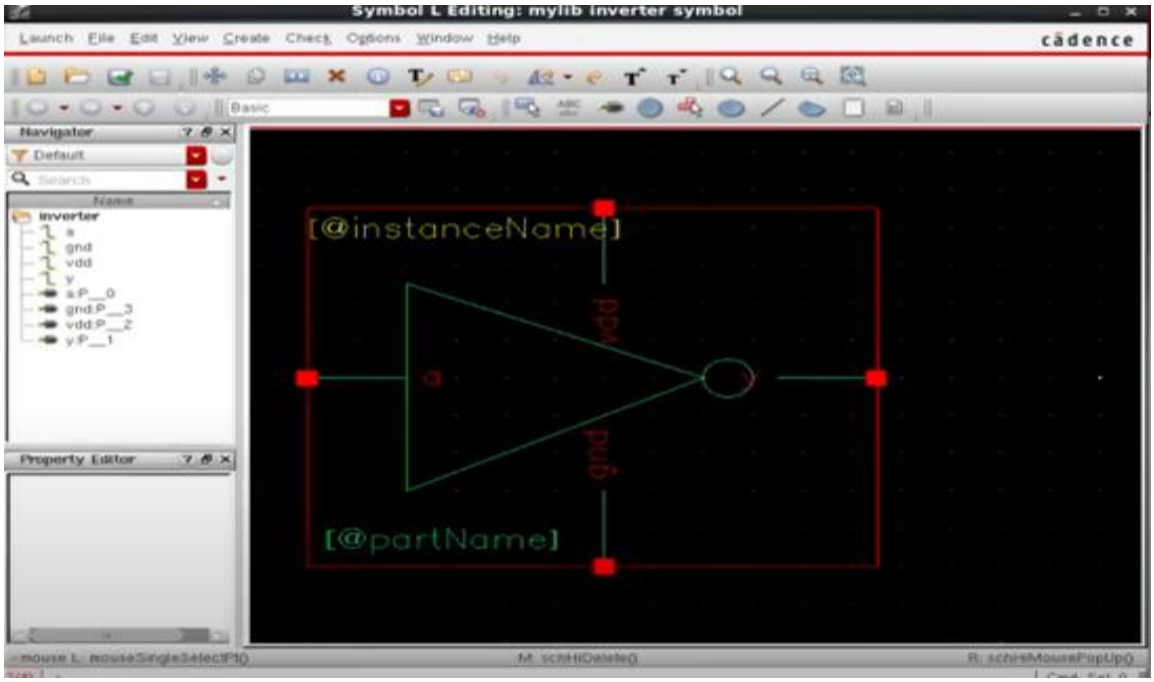
right pin:y

top pin:vdd

bottom pin:gnd



12)Convert it into the following format using wire and create>shapes:circle



13)Save

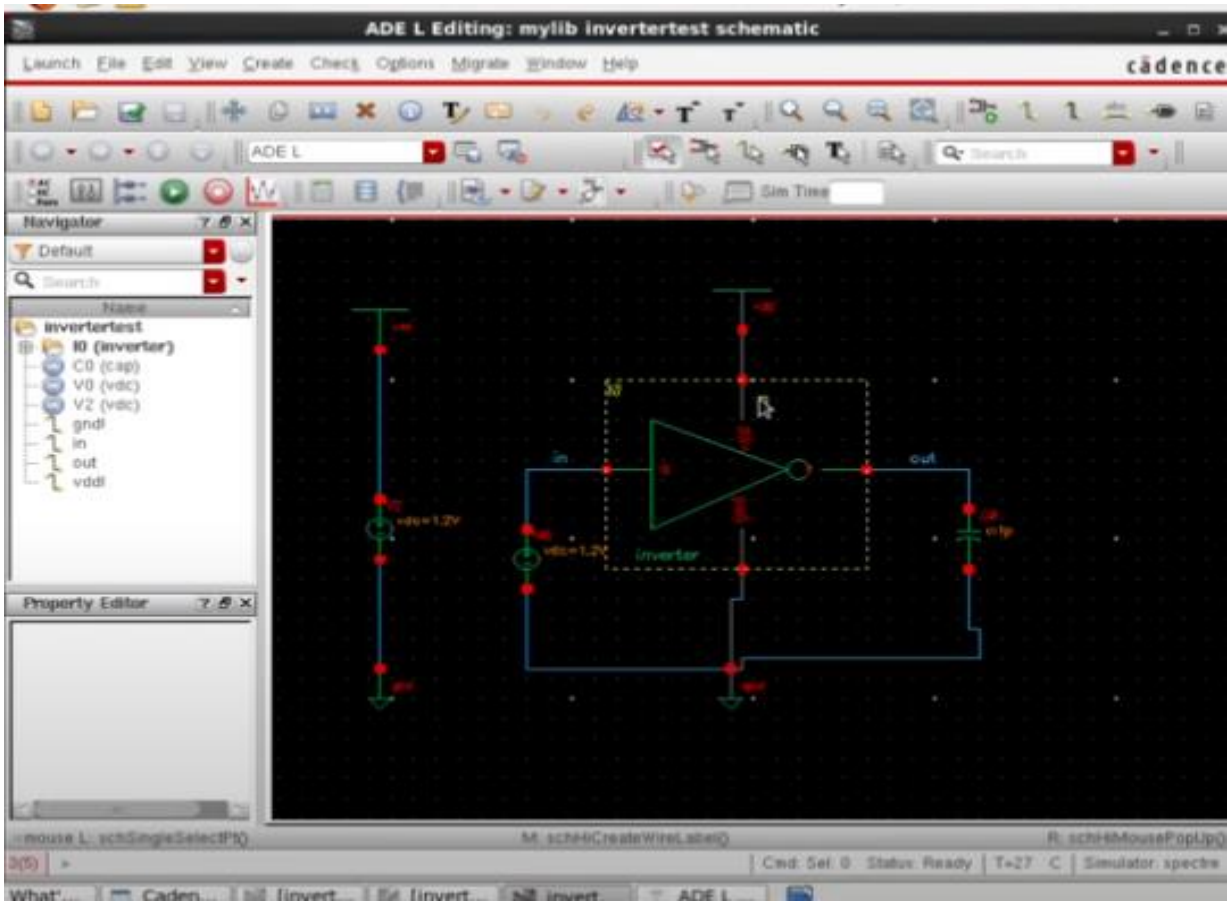
14)Go back to **mylib**>click on **inverter**>File>New>cell view>invertertest>a new schematic window appears

15)Create>instance

Library	Cell view	Value
mylib	inverter	hide
analogLib	vdc	1.2V
analogLib	cap	1pF
analogLib	vdd	hide
analogLib	gnd	hide

16)Set up the connections as shown

Press **“W”** for wire to connect the circuit



17)save it

18))Launch>ADE L

Analyses >choose> DC>select **save Dc operating point**>select component parameter>select component>click on **vdc** in schematic tab>a pop up appears>select DC

19)Go back to choosing analysis tab>give start:0 stop:1.2>OK

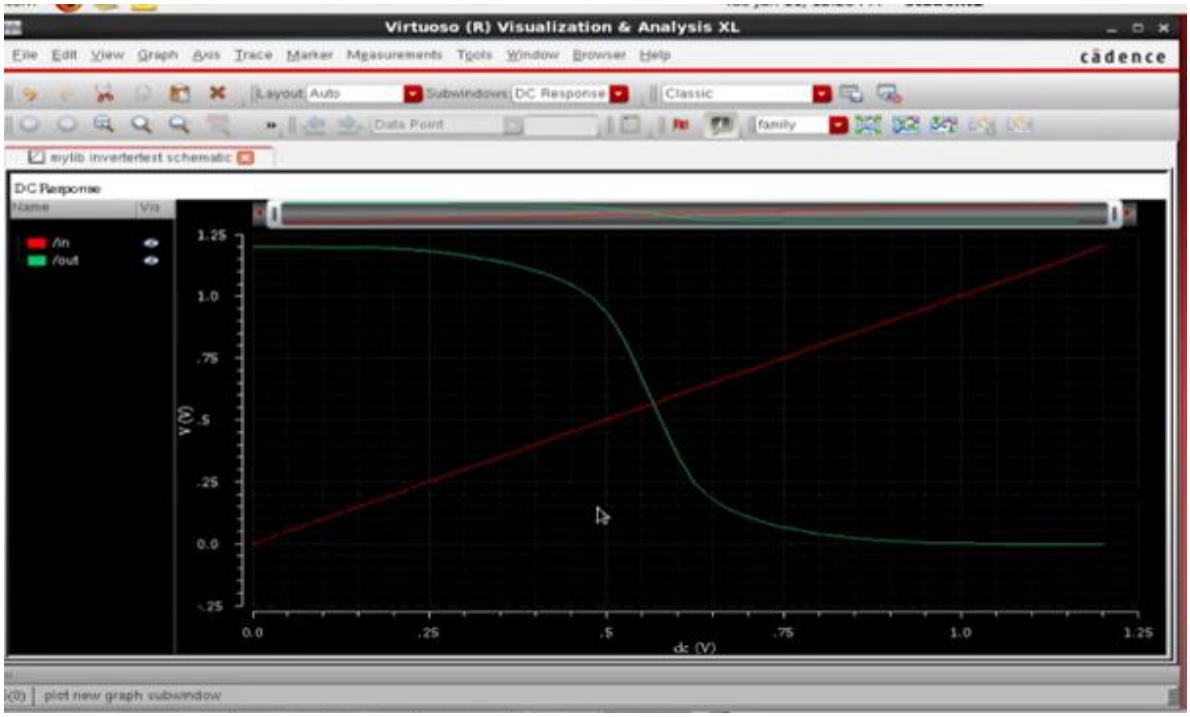
20)In schematic window

Create>wire name>in out

21)Again in ADE L

Output>**To be plotted**>select on simulation>click in out in schematic window

Run



22)In schematic window>Choose vdc>click **Q**>change vdc to vpulse

Votage2:1.2v

Period:10ns

Delay:1ps

Rise time:1ps

Fall time:1ps

Pulse width:5ns

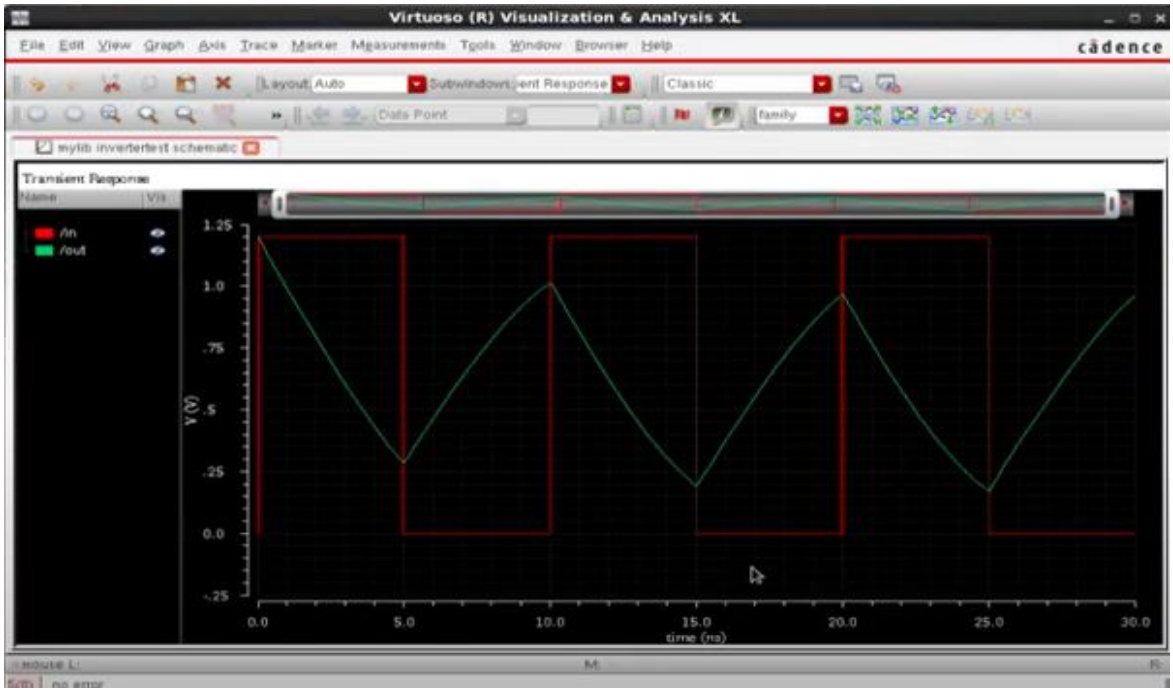
23)click ok

24)check and save

25)Go back to ADE L window

Analyses >choose> Trans>stop:30n

26)Netlist Run


Virtuoso (R) Visualization & Analysis XL
File Edit View Graph Axis Trace Marker Measurements Tools Window Browser Help
cadence
mylib invertertest schematic
Transient Response
Name
Vis
/in
/out
1.25
1.0
.75
.5
.25
0.0
-.25
V (V)
0.0
5.0
10.0
15.0
20.0
25.0
30.0
time (ns)