TPU-MLIR: A Compiler For TPU Using MLIR

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Abstract

Multi-level intermediate representations (MLIR) show great promise for reducing the cost of building domain-specific compilers by providing a reusable and extensible compiler infrastructure. This work presents TPU-MLIR, an end-to-end compiler based on MLIR that deploys pre-trained neural network (NN) models to a custom ASIC called a Tensor Processing Unit (TPU). TPU-MLIR defines two new dialects to implement its functionality: 1. a Tensor operation (TOP) dialect that encodes the deep learning graph semantics and independent of the deep learning framework and 2. a TPU kernel dialect to provide a standard kernel computation on TPU. A NN model is translated to the TOP dialect and then lowered to the TPU dialect for different TPUs according to the chip's configuration. We demonstrate how to use the MLIR pass pipeline to organize and perform optimization on TPU to generate machine code. The paper also presents a verification procedure to ensure the correctness of each transform stage.

1. Introduction

The development of deep learning (DL) has profoundly impacted various scientific fields, including speech recognition, computer vision, and natural language processing. In order to facilitate the process of training deep learning models, industry and academia have developed many frameworks, such as Caffe, Tensorflow, Pytorch, Mxnet, and PaddlePaddle, which boost deep learning in many areas. However, each framework has its proprietary graph representation, which brings lots of work for deploying as we need to support many DL model formats.

At the same time, matrix multiplication and high dimensional tensor convolution are the heavy computation in DL, which evoke the passion of chip architects to design customized DL accelerators to achieve high performance at low energy. Although GPU is still the leading hardware in training DL models and all the DL frameworks have contributed much work to support this general-purpose hardware, GPU is not the perfect piece in the inference domain of DL. GPU is for gaming, graph rendering, scientific computation, and much more, not tailored for DL only. Thus, many DL accelerators, such as Google TPU, Apple Bonic, Graphcore IPU, and SOPHGO TPU, are more energy efficient than GPU and benefit many of these emerging DL applications.

In addition, the DL community has resorted to domain-specific compilers for rescue to address the drawback of DL libraries and alleviate the burden of manually optimizing the DL models on each DL hardware. The DL compilers take the model described in the DL frameworks as inputs and generate efficient code for various DL hardware as outputs. The transformation between a model definition and specific code implementation is highly optimized, considering the model specification and hardware architecture. Several popular DL compilers, such as TVM, Tensor Comprehension, and XLA, have been proposed by industry and academia. Specifically, they incorporate DL-oriented optimizations such as layer and operator fusion, which enables highly efficient code generation.

Herein, We provide TPU-MLIR, an open-source DL compiler for TPU. In particular, we chose Open Neural Network Exchange (ONNX)[1] as a DL format to represent our compiler's input model and use Multi-level Intermediate Representation (MLIR) [7], a modern open-source compiler infrastructure for multi-level intermediate representation, to design TPU-MLIR[1] compiler.

In this work, we will introduce our compiler by

- presenting the overall design and architecture of the compiler,

- introducing two new dialects: TOP dialect to encode the deep learning graph semantics independent of the deep learning framework and TPU dialect to provide a common lowering point for all TOP dialect operations but device-dependent,

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[1]https://github.com/sophgo/tpu-mlir

- detailing each compile stage, such as converting NN models to Top dialect as device independent and then converting TOP to TPU for various chips and types,

- defining WeightOp for weight operation and store weight data in the NumPy npz file, and

- providing InferenceInterface for TOP and TPU to ensure correct conversions.

We organize the remainder of the paper as follows. In Sec. 2, we briefly discuss MLIR, ONNX, on which our compiler is based, and the calibration processing, which tailors computation for TPU. Sec. 3, we introduce our compiler's design principle and architecture and discuss TOP and TPU dialects. We also discuss using inference to ensure each conversion stage correction. Finally, we conclude our paper and discuss future work in Sec. 4.

2. Background

2.1. MLIR

The MLIR, with much reusable and extensible, is a novel approach or constructing new domain-specific compilers. An open ecosystem is the most significant difference from LLVM. MLIR standardizes the Static Single Assignment (SSA)-based IR data structures allowing one to express a range of concepts as first-class operations. Operations can represent many different levels of abstraction and computations, from dataflow graphs to target-specific instructions and even hardware circuitry. They take and produce zero or more values, called operands and results, respectively. A value represents data at runtime and is associated with a type known at compile-time, whereas types model compile-time information about values. Complementary to this, attributes contain compile-time information to operations. Operations, Attribute, and type systems are open and extensible. The custom types, operations, and attributes are logically grouped into dialects. A dialect is one of the most fundamental aspects of MLIR that enables the infrastructure to implement a stack of reusable abstractions. Each abstraction encodes and preserves transformation validity preconditions directly in its IR, reducing the complexity and the cost of analysis passes. The MLIR IR has a recursive structure where operations contain a list of regions, and regions contain a list of blocks, which in turn, contain a list of operations.

In particular, MLIR features operation, attribute and type interfaces providing a generic way of interacting with the IR. Interfaces allow transformations and analyses to work with abstract properties rather than fixed lists of supported concepts. Interfaces can be implemented separately from operations and mixed in using MLIR's registration mechanism, thus fully separating IR concepts from transformations. Furthermore, transformations can be written as compositions of orthogonal localized "match and rewrite" primitives. These are often decomposed further into rewriting rules when applied within a dialect and lowering rules when converting from a higher-level dialect to a lower-level dialect. Throughout the compilation, separate dialects can co-exist to form a hybrid program representation. The ability to progressively lower dialects to the target hardware during the compilation process has made MLIR an excellent compiler infrastructure for domain-specific languages.

This article relies on several MLIR dialects and types, briefly described below.

2.1.1 Ranked Tensor Type

Values with tensor type represent aggregate N-dimensional homogeneous data indicated by element type and a fixed rank with a list of dimensions[2]. Each dimension could be a static non-negative integer constant or be dynamically determined (marked by ?).

This abstracted runtime representation carries both the tensor data values and information about the tensor shape, but the compiler has not decided on its representation in memory. Tensor values are immutable and subject to def-use SSA semantics[9]. Operations on tensors are often free of side effects, and operations always create new tensors with a value. The textual format of the tensor is $\mathsf{tensor}\langle\mathsf{d_1xd_2x\cdots xd_Nxdtype}\rangle$, where $\mathsf{d_1}$, $\mathsf{d_2}$, ... $\mathsf{d_N}$ are integers or symbol ? representing the dimensions of a tensor, and dtype is the type of the elements in a tensor, e.g., F32 for float32. A tensor can be unranked when its shapes are unknown. MLIR uses $\mathsf{tensor}\langle\mathsf{*xdtype}\rangle$ to represent unranked tensor types.

2.1.2 Quantization Dialect

Quantization dialect[3] provides a family of quantized types and type-conversion operations. The "quantization" refers to the conversion of floating-point computations to corresponding variants expressed in integer math for inference, as has been supported by low-bit depth inference engines such as various accelerator hardware and many DSPs. There are three types defined in quantization dialect: UniformQuantizedType, UniformQuantizedPerAxisType, and CalibratedQuantizedType.

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[2]https://mlir.llvm.org/docs/Dialects/Builtin/#rankedtensortype
[3]https://mlir.llvm.org/docs/Dialects/QuantDialect

The UniformQuantizedType and UniformQuantizedPer-AxisType represent the mapping between expressed values (e.g., a floating-point computer type) and storage values (typically of an integral computer type), expressing the affine transformations from uniformly spaced points to the real number line. The relationship is: realValue = scale × (quantizedValue − zeroPoint) and will be discussed in more detail in Section 2.3. Where CalibratedQuantizedType holds the range from the given min and max value of the histogram data of the tensor, used for recording the statistics information of the tensor. The UniformQuantizedPerAxisType applies affine transformation individually to each index along a specific axis of a tensor type. However, UniformQuantizedType applies the affine transformation to every value within the target type. The type-conversion defined in quantization dialect provides three operations for converting between types based on a QuantizedType and its expressed and storage subtypes. Those operations are: quant.qcast converting from an expressed type to QuantizedType, quant.dcast converting from a QuantizedType to its expressed type, and quant.scast converting between a QuantizedType and its storage type.

2.2. ONNX

ONNX is an open-source framework-independent format widely used for exchanging computation graph models, including deep learning and traditional machine learning. It was accepted as a graduate project in Linux Foundation AI and maintained by open-source communities. ONNX defines an extensible computation graph model, operators, and standard data types for deep learning and provides a set of specifications to convert a model to a basic ONNX format and another to get the model back from this ONNX form. It is an ideal tool for framework interoperability, especially when deploying a model to specific hardware[5].

ONNX reduces the friction of moving trained DL models among AI frameworks and platforms. ONNX uses the Protocol Buffers language for its syntax and provides rich documents and tools to formalize each operation's semantics and verify its correctness.

2.3. Quantization

Quantization is a promising technique to reduce deep learning models' memory footprint, inference latency, and power consumption, which replaces high-cost floating-point (always F32) computation with low-cost fixed-point numbers[4] (e.g., INT8/INT16) or float-point (e.g., BF16/F16). Because most current DL models are heavily over-parameterized and robust to extreme discretization, there is much opportunity for reducing numeral precision without impacting the model's accuracy, bringing ample

search space for tuning. Although many quantization methods have emerged, there is not a single well-posed or well-conditioned problem being solved[3]. Instead, one is interested in some error metric (based on classification quality, data similarity, etc.). to guide the quantization process. However, due to the over-parameterization, it is possible to have a high error between a quantized and the original model while still attaining excellent generalization performance. Finally, different layers in a Neural Net have a different impact on the loss function, which motivates a mixed-precision approach quantization.

2.3.1 Uniform Quantization

The quantization process is a function mapping from real values r to some numeral values. Quantization function such as

$$\text{quant}(r) = \text{round}(\frac{r}{s}) + \text{zp} \tag{1}$$

where quant is the quantization operator, r is a real-valued input (activation or weight), s is a float-point scaling factor, and zp is an integer zero point, is known as uniform quantization, as the resulting quantized values are evenly spaced.

2.3.2 Symmetric and Asymmetric Quantization

A crucial factor in uniform Quantization is choosing the scaling factor s in Equation 1. This scaling factor, also known as resolution, divides a given range of real-values r into several partitions $s = \frac{\beta - \alpha}{2^b - 1}$, where $[\alpha, \beta]$ denotes the clipping range that we are clipping the real-values with, and b is the quantization bit width[4][6]. Therefore, one should determine the clipping range $[\alpha, \beta]$ before generating the scaling factor. If the clipping range of α equals $-\beta$, we get Symmetric Quantization, and on the contrary, we get asymmetric Quantization. The asymmetric quantization method often results in a tighter clipping range than symmetric Quantization, which is especially important when the dynamic range of the tensor is imbalanced, e.g., the result of ReLU always has non-negative values.

2.3.3 Calibration

The process of choosing the clipping range is called "calibration." One popular method for pre-calculation is to run a series of inferences on some sample data and then get the distribution of each tensor in the graph. Using the min/max of the signal for both symmetric and asymmetric Quantization is typical in most cases. However, this approach is susceptible to outlier data in the activations, which could unnecessarily increase the range and reduce quantization resolution. One approach to address this is
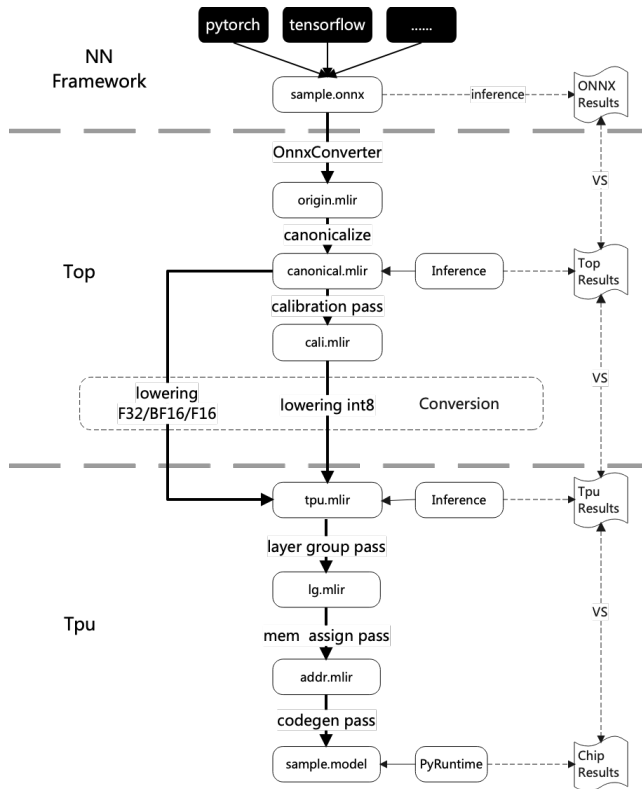
Figure 1: Architecture of tpu-mlir.

using percentile or selecting α and β to minimize KL divergence between the real and the quantized values[8][11]. Besides, there are other metrics to find the best range, including minimizing Mean Squared Error (MSE)[2], entropy, and cosine similarity.

3. Compiler

This section introduces the compiler, TPU-MLIR, which creates two layers by the TOP and TPU dialects for converting NN models to executable files by various types and chips. We discuss TPU-MLIR's overall architecture first.

3.1. Overview

Figure 1 shows the overall architecture of TPU-MLIR. We divide it into the NN Framework, Top, and Tpu.

1) **NN Framework**: TPU-MLIR supports ONNX models directly. Other NN framework models, such as Pytorch, and Tensorflow, need to convert to ONNX modes.

2) **TOP**: refer to the TOP dialect as the top abstraction level representing NN models in the MLIR language. It is device independent.

3) **TPU**: refer to the TPU dialect, which is the TPU abstraction level and represents TPU operations. It is device dependent.

We first convert a NN model to TOP abstraction with TOP dialect and built-in dialect defined in MLIR, which we call TOP mlir file, by python script, i.e., OnnxConverter in figure 1. Then we lower the top mlir file to TPU abstraction with TPU dialect and built-in dialect defined in MLIR, which we call tpu mlir through some passes, such as canonicalization pass and calibration pass. At last, we convert tpu mlir to tpu models by some passes, such as layer group pass and memory assign pass. These passes will be discussed in the later section.

3.2. Module

We introduce our module definition by a simple mlir file showed Listing 1:

Module has some attributes: module.name is related to the NN model name; module.weight_file is a npz[4] file that stores weight data needed by operations. We use location to express operation name. For example, '%2 = "top.Weight"()' (Line 6 in Listing 1) is a weight op, and location is "filter_conv1". So the real weight data is stored in "conv2d_weight.npz" file by name "filter_conv1".

3.3. Top Dialect

TOP dialect is very similar to TOSA (Tensor Operator Set Architecture)[5] dialect in MLIR. So why we don't use TOSA dialect? There are two reasons: the first is that we need to do inference for each operations, and may create some new features in the futrue; the second is that we need to keep extend capability to support various NN models.

TOP Dialect is defined as below:

```
1 def Top_Dialect : Dialect {
2   let name = "top";
3   let summary = "A top dialect for the ←
      TPU_MLIR specification";
4   let cppNamespace = "::tpu_mlir::top";
5   let emitAccessorPrefix = ←
      kEmitAccessorPrefix_Raw;
6   let extraClassDeclaration = [{...}];
7 }
```

In TOP Dialect, TOP_BaseOp and TOP_Op define as:

```
1 class Top_BaseOp<string mnemonic, ←
      list<Trait> traits = []> :
2   Op<Top_Dialect, mnemonic, ←
        !listconcat(traits,[NoSideEffect])>;
3
4 class Top_Op<string mnemonic, list<Trait> ←
      traits = []> :
5 Top_BaseOp<mnemonic, !listconcat(traits,
6 [DeclareOpInterfaceMethods<InferenceInterface>,
```

Listing 1: Simple convolution computation represented by TPU dialect.

```
1  #loc0 = loc(unknown)
2  module attributes {module.name = "Sample", module.weight_file = "conv2d_weight.npz"} {
3    func.func @main(%arg0: tensor<1x16x100x100xf32> loc(unknown)) -> ↩
         tensor<1x32x100x100xf32> {
4      %0 = "top.None"() : () -> none loc(#loc0)
5      %1 = "top.Input"(%arg0) : (tensor<1x16x100x100xf32>) -> tensor<1x16x100x100xf32> ↩
         loc(#loc1)
6      %2 = "top.Weight"() : () -> tensor<32x16x3x3xf32> loc(#loc2)
7      %3 = "top.Weight"() : () -> tensor<32xf32> loc(#loc3)
8      %4 = "top.Conv"(%1, %2, %3) {dilations = [1, 1], do_relu = false, group = 1 : i64, ↩
         kernel_shape = [3, 3], pads = [1, 1, 1, 1], strides = [1, 1]} : ↩
         (tensor<1x16x100x100xf32>, tensor<32x16x3x3xf32>, tensor<32xf32>) -> ↩
         tensor<1x32x100x100xf32> loc(#loc4)
9      return %4 : tensor<1x32x100x100xf32> loc(#loc0)
10   } loc(#loc0)
11 } loc(#loc0)
12 #loc1 = loc("input")
13 #loc2 = loc("filter_conv1")
14 #loc3 = loc("bias_conv1")
15 #loc4 = loc("conv1")
```

```
7 DeclareOpInterfaceMethods<FlopsInterface>])>;
```

TOP_Op has two interfaces: "InferenceInterface" and "FlopsInterface". "InferenceInterface" is used to do inference for operation, which would be introduced later. "FlopsInterface" is used to count FLOPs (floating point operations) of operation, as we are interested in the FLOPs of a NN model, also we use it to evaluate chip performance after running on the chip.

There are top operations defined based on TOP_BaseOp or TOP_Op. Here just using ConvOp and WeightOp for examples.

3.3.1   top::ConvOp

ConvOp is defined as below:

```
1  def Top_ConvOp: Top_Op<"Conv"> {
2    let summary = "Convolution operator";
3    let arguments = (ins
4      AnyTensor:$input,
5      AnyTensor:$filter,
6      AnyTensorOrNone:$bias,
7      I64ArrayAttr:$kernel_shape,
8      I64ArrayAttr:$strides,
9      I64ArrayAttr:$pads, // ↩
           top,left,bottom,right
10     DefaultValuedAttr<I64Attr, "1">:$group,
11     OptionalAttr<I64ArrayAttr>:$dilations,
12     DefaultValuedAttr<BoolAttr, ↩
           "false">:$do_relu,
13     DefaultValuedAttr<F64Attr, ↩
           "-1.0">:$relu_limit
14   );
15   let results = (outs AnyTensor:$output);
16 }
```

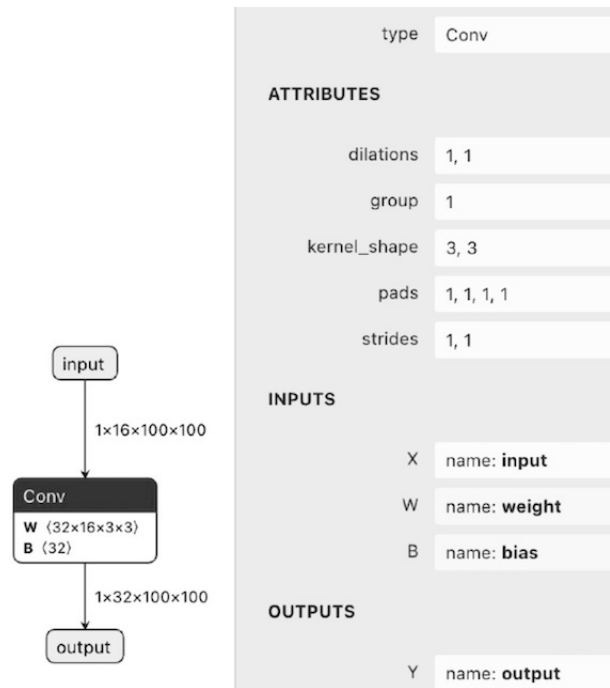ConvOp represents conv operation of NN models, like Figure 2:

Figure 2: Convolution operation defined in ONNX.

and in mlir file experessed as below:

```
1 %4 = "top.Conv"(%1, %2, %3) {dilations = ↩
       [1, 1], do_relu = false, group = 1 : ↩
       i64, kernel_shape = [3, 3], pads = [1, ↩
       1, 1, 1], strides = [1, 1]} : ↩
       (tensor<1x16x100x100xf32>, ↩
       tensor<32x16x3x3xf32>, tensor<32xf32>) ↩
       -> tensor<1x32x100x100xf32>
```

3.3.2 top::WeightOp

WeightOp is a special operation for weight datas. Defined as below:

```
1 def Top_WeightOp : Top_BaseOp<"Weight"> {
2   let summary = "load weight operator";
3   let results = (outs AnyTensor:$output);
4   let extraClassDeclaration = [{
5   template<typename T>
6   std::shared_ptr<std::vector<T>> read();
7   template<typename T>
8   static mlir::Value ←
        create(mlir::Operation * OwnerOp,
9   llvm::StringRef suffix,
10  const std::vector<T>& data,
11  mlir::RankedTensorType& type);
12  }];
13 }
```

WeightOp is corresponding to weight operation. Weight data is stored in "module.weight_file", WeightOp can read data from weight file by **read** method, or create new WeightOp by **create** method.

3.4. TPU Dialect

TPU Dialect is defined as below:

```
1 def Tpu_Dialect : Dialect {
2   let name = "tpu";
3   let summary = "A tpu dialect for the ←
        SOPHGO AI chips";
4   let cppNamespace = "::tpu_mlir::tpu";
5   let useDefaultAttributePrinterParser = 1;
6   let emitAccessorPrefix = ←
        kEmitAccessorPrefix_Raw;
7 }
```

TPU dialect is for TPU chips, here we support SOPHGO AI chips first. It is used to generate chip command instruction sequences by tpu operations.

In TPU dialect, TPU_BaseOp and TPU_Op define as:

```
1 class Tpu_BaseOp<string mnemonic, ←
      list<Trait> traits = []> :
2   Op<Tpu_Dialect, mnemonic,
3       !listconcat(traits,[NoSideEffect, ←
          TpuTypeRestrict])> ;
4
5 class Tpu_Op<string mnemonic, list<Trait> ←
      traits = []> :
6   Op<Tpu_Dialect, mnemonic, ←
          !listconcat(traits,
7     [NoSideEffect, TpuTypeRestrict,
8       DeclareOpInterfaceMethods<
9         GlobalGenInterface>,
10      DeclareOpInterfaceMethods<
11        InferenceInterface>])>;
```

TPU_Op has two interfaces, "GlobalGenInterface" and "InferenceInterface". "GlobalGenInterface" is used to generate chip command. "InferenceInterface" is used to do inference for tpu operations.

There are top operations defined based on TOP_BaseOp or TOP_Op. Here using tpu::ConvOp

, and tpu::CastOp, and tpu::GroupOp for example.

3.4.1 tpu::Conv2DOp

Conv2DOp is defined as below:

```
1 def Tpu_Conv2DOp: Tpu_Op<"Conv2D"> {
2   let arguments = (ins
3     AnyTensor:$input,
4     AnyTensor:$filter,
5     AnyTensorOrNone:$bias,
6     I64ArrayAttr:$kernel_shape,
7     I64ArrayAttr:$strides,
8     I64ArrayAttr:$pads, // ←
        top,left,bottom,right
9     DefaultValuedAttr<I64Attr, "1">:$group,
10    OptionalAttr<I64ArrayAttr>:$dilations,
11    DefaultValuedAttr<BoolAttr, ←
        "false">:$do_relu,
12    DefaultValuedAttr<F64Attr, ←
        "-1.0">:$relu_limit,
13    //new param
14    OptionalAttr<I64ArrayAttr>:$multiplier,
15    OptionalAttr<I64ArrayAttr>:$rshift,
16    OptionalAttr<Tpu_LayerGroupAttr>:$group_info
17  );
18
19  let results = (outs AnyTensor:$output);
20 }
```

Compared to top::ConvOp, tpu::Conv2DOp has some new attributes: "multiplier", "rshift" and "group_info". "multiplier" and "rshift" are used to do INT8 convolution after quantization, and not used if do float convolution. "group_info" is used for the layer group. We will discuss layer group later.

3.4.2 tpu::CastOp

CastOp is defined as below:

```
1 def Tpu_CastOp:Tpu_Op<"Cast",
2   [DeclareOpInterfaceMethods
3     <LocalGenInterface>]> {
4   let summary = "Cast operation";
5   let description = [{}];
6   let arguments = (ins
7     AnyTensor:$input,
8     OptionalAttr<Tpu_LayerGroupAttr>:$group_info
9   );
10  let results = (outs AnyTensor:$output);
11 }
```

CastOp is for transferring tensor type from one type to another. It can convert the F32 type to BF16[10] type or F16 type, or INT8 type, and the other way around is also OK.

Specially, if input is F32 type and output is quantization type, such as Listing 2, then:

$$output = \text{RoundToInt8}(\frac{input_{f32}}{qscale} + zeroPoint) \quad (2)$$

Listing 2: **top.cast** operaiotn convertion a calibrated type to **quant.uniform** type.

```
1 %1 = "tpu.Cast"(%0) : ↩
      (tensor<1x16x100x100x!quant.calibrated<f32<-4.1780586242675781:4.4932479858398438>>>) ↩
      -> tensor<1x16x100x100x!quant.uniform<i8:f32, 0.034005123961205579:-5>>
```

Listing 3: **top.cast** operaiotn convertion a diopquantuniform type to float32 type.

```
1 %5 = "tpu.Cast"(%4) : (tensor<1x32x100x100x!quant.uniform<i8:f32, ↩
      0.43113517013250613:-2>>) -> tensor<1x32x100x100xf32>
```

If input is quantization type and output is F32 type, such as Listing 3, then

$$output = (input_{i8} - zeroPoint) * qscale \qquad (3)$$

.

3.4.3 tpu::GroupOp

GroupOp is defined as below:

```
1 def Tpu_GroupOp:Tpu_BaseOp<"Group"> {
2   let summary = "Group operation";
3   let description = [{
4     Make ops in one group to inferece by ↩
          local mem
5   }];
6   let arguments = (ins
7     Variadic<AnyTensor>:$inputs,
8     I64Attr:$nsecs,
9     I64Attr:$hsecs
10  );
11  let results = (outs ↩
        Variadic<AnyTensor>:$outputs);
12  let regions = (region ↩
        SizedRegion<1>:$body);
13 }
```

GroupOp contains serial operations that can inference in tpu local memory. We will discuss it later.

3.5. Conversion

This section we discuss how to convert top ops to tpu ops.

We define "ConvertTopToTpu" pass like this:

```
1 def ConvertTopToTpu : ↩
     Pass<"convert-top-to-tpu", "ModuleOp"> {
2   let summary = "Convert top-level Top ↩
       Ops to Tpu Ops";
3   let constructor = ↩
       "tpu_mlir::createConvertTopToTpu()";
4   let dependentDialects = ↩
       ["tpu_mlir::top::TopDialect", ↩
       "tpu_mlir::tpu::TpuDialect"];
5   let options = [
6     Option<"mode", "mode", "std::string", ↩
         /*default=*/"",
7           "default quantization mode: ↩
               INT8/BF16/F16/F32">,
```

```
8     Option<"chip", "chip", "std::string", ↩
         /*default=*/"",
9           "chip: ↩
               cv183x/cv182x/bm1684/bm1684x">,
10    Option<"isAsymmetric", "asymmetric", ↩
        "bool", /*default=*/"false",
11          "true for asymmetric ↩
               quantization, or false for ↩
               symmetric">,
12  ];
13 }
```

There are there options: mode, chip and isAsymmetric.

1) **mode**: set quantization mode, e.g. INT8, BF16, F16 or F32. Types should be supported by the chip.

2) **chip**: set chip name. TPU operations will act by this chip.

3) **isAsymmetric**: if **mode** is INT8, set true for asymmetric quantization; false for symmetric quantization.

Normally, TOP ops convert to TPU ops by float type (F32/BF16/F16), most of attributes are the same. But if by INT8 type, TOP ops need do PTQ (Post-training Quantization)[4], and add some external quantization attributes to Tpu Ops, while weight datas and inputs and outputs will be quantized to INT8. In addition, inputs and outputs of a NN model need to insert CastOp if convert type is not F32. The conversion flow chart shows as Figure 3.

3.6. Inference

This section we discuss why to do inference and how to support inference for top dialect and tpu dialect.

3.6.1 Why

TOP dialect do inference and get inference results, which has three uses.

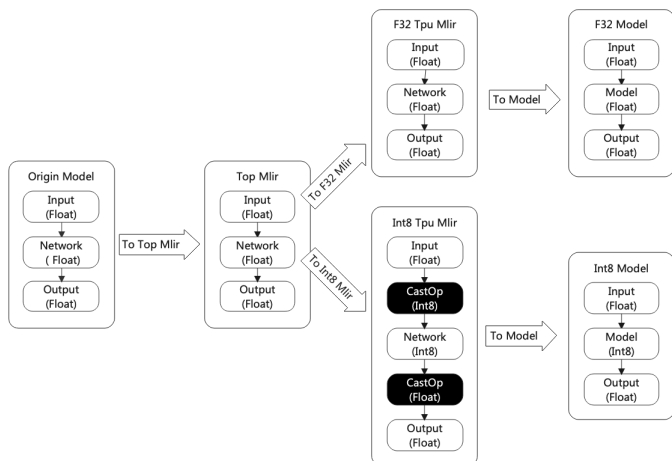1) It can be used to compare with original model results, to make sure NN model convert to TOP dialect correctly.

Figure 3: The neural network model conversion flow of TPU-MLIR.

2) It can be used to do calibration, which uses a few sampled inputs to do inference by top mlir file and get every intermediate result, to stat proper min/max threshold, and would be used by Quantization.

3) It can be used to compare with tpu dialect to ensure tpu mlir is correct.

TPU dialect makes inference and gets inference results, would compare with top mlir results. If tpu mlir is in F32 mode, the results should be the same. If tpu mlir is BF16/F16 mode, the tpu results may have some loss but still should have a good cosine similarity (>0.95) and euclidean similarity (>0.85). If tpu mlir is INT8 mode, cosine similarity should be greater than 0.9, and euclidean similarity should be greater than 0.5, based on experience. If cosine similarity and euclidean similarity are not satisfied, conversion from top to tpu may have some problems.

Cosine similarity is defined as below:

```
1 def square_rooted(self, x):
2   return sqrt(sum([a*a for a in x]))
3
4 def cosine_similarity(self, x, y):
5   numerator = sum(a*b for a,b in zip(x,y))
6   denominator = ←
        self.square_rooted(x)*self.square_rooted(y)
7   return ←
        round(numerator/float(denominator),3)
8
9 cosine_similarity = cosine_similarity(x, y)
```

Euclidean similarity is defined as below:

```
1 def euclidean_distance(x, y):
2   return sqrt(sum(pow(a-b,2) for a, b in ←
        zip(x, y)))
3 ed = euclidean_distance(x, y)
4 sr = square_rooted((x+y)/2)
5 euclidean_similary = 1 - ed/sr
```

At last, after being compiled, the model needs to do inferences in the tpu chip and compare with tpu mlir results to ensure codegen is correct. If not similar, codegen or chip may have some problems.

3.6.2   How

NN models inference by NN runtime. For example, ONNX models inference by ONNX runtime.

TOP dialect and TPU dialect inference by "InferenceInterface", which defines as below:

```
1 struct InferenceParameter {
2   std::vector<float *> inputs;
3   std::vector<float *> outputs;
4   void *handle = nullptr;
5 };
```

```
1 def InferenceInterface : ←
      OpInterface<"InferenceInterface"> {
2   let cppNamespace = "::tpu_mlir";
3   let methods = [
4       InterfaceMethod<
5         /*desc=*/[{}],
6         /*retType=*/"::mlir::LogicalResult",
7         /*methodName=*/"inference",
8         /*args=*/(ins ←
              "InferenceParameter&":$param)
9     >
10      InterfaceMethod<
11        /*desc=*/[{}],
12        /*retType=*/"::mlir::LogicalResult",
13        /*methodName=*/"init",
14        /*args=*/(ins ←
              "InferenceParameter&":$param)
15    >,
16      InterfaceMethod<
17        /*desc=*/[{}],
18        /*retType=*/"void",
19        /*methodName=*/"deinit",
20        /*args=*/(ins ←
              "InferenceParameter&":$param)
21    >,
22  ];
23 }
```

"inputs" and "outputs" in "InferenceParameter" point to input buffers and output buffers of the operation. All buffers that tensor needed would be allocated after mlir file were loaded. Each buffer size is calculated from Value's type. For example, the type tensor⟨1x32x100x100xf32⟩', need size $1 \times 32 \times 100 \times 100 \times$ sizeof(float) $= 1280000$bytes. Figure 4 is an example.

Weights are allocated and loaded first, and then activations are allocated. Before inference, inputs of the model will be loaded to input buffers. And then, do inference. After inference, results are stored in each activation buffers.

"handle" in "InferenceParameter" is used to point third-party excute engine, and it is optional.

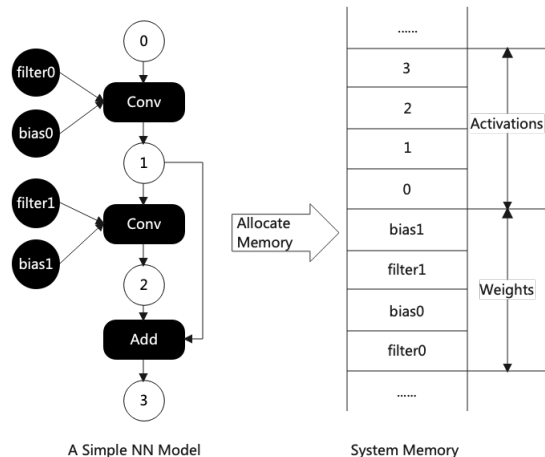"InferenceInterface" has three functions: "init", "in-
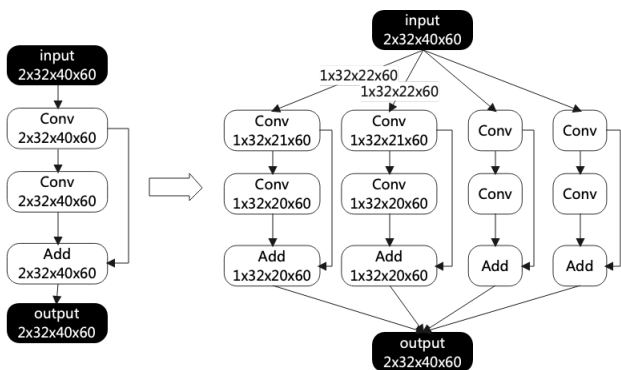
Figure 4: Buffer allocation in TPU-MLIR.

Figure 5: Slice the H dimensional in a layer group.

ference", "deinit". "init" and "deinit" are used to init and deinit handle of third-party engine if needed, or do nothing. "inference" is used to do inference by "inputs" in "InferenceParameter" and store results in "outputs" of "InferenceParameter".

3.7. Layer Group

Layer group in TPU-MLIR means some layers composed into one group execute in the TPU chip. The layer here is the same thing as the operation in MLIR. Typically, RAM on a chip is tiny, such as 256KB, while DDR off-chip is very large, such as 4GB. We need layers to run on the chip successively to achieve high performance, but the RAM on a chip is too small to support it. So we slice layers into small pieces to make sure layers in a group can run successively. Usually, we slice layers by N or H dimension. Figure 5 shows an example.

In mlir, we define group attributes for tpu operations:

```
1 def Tpu_LayerGroupAttr : ↩
      Tpu_Attr<"LayerGroup", "lg"> {
2   let summary = "Structure of layer group ↩
```

```
      parameters";
3   let parameters = (ins
4     "int64_t":$out_addr,
5     "int64_t":$out_size,
6     "int64_t":$buffer_addr,
7     "int64_t":$buffer_size,
8     "bool":$eu_align,
9     ArrayRefParameter<"int64_t">:$h_idx,
10    ArrayRefParameter<"int64_t">:$h_slice,
11    ArrayRefParameter<"int64_t">:$n_idx,
12    ArrayRefParameter<"int64_t">:$n_slice
13  );
14  let assemblyFormat = "`<` ↩
        struct(params) `>`";
15 }
```

Different architecture TPU may have different attributes, attributes in "LayerGroup" are examples:

1) out_addr: output address in RAM on chip

2) out_size: output memory size in RAM on chip

3) buffer_addr: buffer address for operation in RAM on chip

4) buffer_size: buffer size in RAM on chip

5) eu_align: whether data arranged in RAM on chip is aligned

6) h_idx: offset positions in h dimension as h has been sliced

7) h_slice: size of each piece after sliced

8) n_idx, n_slice: for n dimension slice

MLIR file with groups, like this Listing 4 (to make it simple, we have removed unrelated info from the file): Layers in a group will execute on a chip successively, and the DMA will load data from DDR off-chip to RAM on-chip and store results back to DDR at the frontier of each group.

3.8. Workflow

This section we discuss the workflow of TPU-MLIR, expecially the main passes.

1) OnnxConverter: use python interface to convert ONNX NN models to the TOP dialect mlir.

2) Canolicalize for TOP: do graph optimization on top operations. For example, we fuse top::ReluOp into top::ConvOp, and we use depthwise conv to take the place of the batchNorn operation.

3) Calibration for TOP: use a few sampled inputs to do inference by top mlir file, and get every intermediate result, to stat proper min/max threshold. We

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Listing 4: MLIR file with layer groups.

```
1    %0 = "top.None"() : ()
2    %1 = "top.Weight"() : ()
3    %2 = "tpu.Group"(%arg0) ({
4      %3 = "tpu.Load"(%arg0) {group_info = #tpu.lg<...>}
5      %4 = "tpu.Cast"(%3) {group_info = #tpu.lg<...>}
6      %5 = "tpu.Load"(%1) {group_info = #tpu.lg<...>}
7      %6 = "tpu.Conv2D"(%4, %5, %0) {group_info = #tpu.lg<...>}
8      %7 = "tpu.Cast"(%6) {group_info = #tpu.lg<...>}
9      %8 = "tpu.Store"(%7) {group_info = #tpu.lg<...>}
10     tpu.Yield %8 : tensor<1x32x100x100xf32, 4295618560 : i64>
11   }) {hsecs = 1 : i64, nsecs = 1 : i64}
12   return %2 : tensor<1x32x100x100xf32, 4295618560 : i64>
```

use quant::CalibratedQuantizedType to express these calibration informations. For example, a value type is tensor⟨1x16x100x100xf32⟩, and it's calibration informations are: min = -4.178, max = 4.493, threshold = 4.30. Then new type would be tensor⟨1x16x100x100x!quant.calibrated⟨f32⟨-4.178:4.493⟩⟩⟩ for asymmetric quantizaion, and tensor⟨1x16x100x100x!quant.calibrated⟨f32⟨-4.30:4.30⟩⟩⟩ for symmetric quantization. Do calibation only for int8 quantizaiton, and there is no need to do it for float convertion.

4) Conversion for TOP: convert top operations to tpu operations. We have discussed it above.

5) Layer group for TPU: determine groups of operations to execute successively in ram on tpu. We have discussed it above.

6) Memory assign for TPU: after TPU operations are ready, all operations out of group need to assign memory in DDR, especially assign physical address. We set physical address in tensor type, such as 4295618560 in tensor⟨1x32x100x100xf32, 4295618560:i64⟩. We don't discuss how to assign memory by an optimal solution here.

7) Codegen for TPU: each TPU operation has codegen interface for different chips and has a corresponding TPU commands packaged in one kernel API. So what codegen to do is here just to call these APIs for each tpu operations, and collect commands to store in one model.

4. Conclusion

We are developing TPU-MLIR to compile NN models for TPU. We design the TOP and TPU dialects as device-independent and device-dependent, respectively. We convert NN models to Top dialect as device independent and convert TOP to TPU for various chips and types. We define WeightOp for weight operation and store weight data in the NumPy npz file. We design 'InferenceInterface' for top and tpu to ensure correct conversions. In the future, we will try to support more TPU chips and NN models with various NN frameworks.

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