SAMEERAN Joshi

# **Contact**

Salt Lake City, Utah, USA

[Joshisameeran17@gmail.com |](mailto:Joshisameeran17@gmail.com%20|)

[https://sameeranjoshi.github.io](https://sameeranjoshi.github.io/sameeran.me//) | [www.linkedin.com/in/sameeran-joshi-b8b1b9144](http://www.linkedin.com/in/sameeran-joshi-b8b1b9144)

# **Research interest**

Compilers, Computer Architecture, Programming Languages, Compiler Optimizations, LLVM, Hardware-Software Codesign, Modern C++, HPC systems

# **Publications**

**PEAK**: **Generating High-Performance Schedules in MLIR**, Amir Mohammad Tavakkoli∗, **Sameeran Joshi∗**, Shreya Singh, Yufan Xu, P. Sadayappan, and Mary Hall. In Proceedings of the 36th International Workshop on Languages and Compilers for Parallel Computing**(**[**LCPC23**](http://www.lcpcworkshop.org/LCPC23/)**)**. Oct. 2023(Accepted)

**An NSF REU Site Based on Trust and Reproducibility of Intelligent Computation: Experience Report**, Mary Hall, Ganesh Gopalakrishnan, Eric Eide, Johanna Cohoon, Jeff M. Phillips, Mu Zhang, Shireen Y. Elhabian, Aditya Bhaskara, Harvey Dam, Artem Yadrov, Tushar Kataria, Amir Mohammad Tavakkoli, **Sameeran Joshi**, Mokshagna Sai Teja Karanam. In **EduHPC workshop** at The International Conference for High Performance Computing, Networking, Storage, and Analysis (**SC23**) (Accepted)

# **Education**

**School of Computing, University of Utah**

PhD Student in Computer Science | Aug 2022 – Currently Enrolled

**Pune University, India**

*Bachelor’s In Computer Engineering | Aug 2015 – May 2019*

GPA: 8.29/10

# **Work experience**

|  | **Argonne National Lab, USA****Research Aide Technical - PhD - LCF | June 2024 – Aug 2024**  * Explored challenges and opportunities in supporting the HPC software stack on **AI accelerators** (Cerebras, Sambanova, Groq, GraphCore) at the AI testbed. * Focused on understanding challenges in compilers, programming languages, and related software stacks.   **Advanced Micro Devices (AMD), India**  **CPU Compiler Engineer | June 2019 - June 2022**   * Extended **LLVM BOLT** to compare statically 2 binaries to report performance difference in 2 CPU generated binaries. * Reported performance issues and suggested optimizations in **AOCC** for SPEC CPU 2017, polybench, and HPC workloads. * Contributed 50+ commits to **LLVM Flang,** adding support for OpenMP and Fortran 2018 features, and reviewing community patches and developing unit tests for Fortran 2008 in AOCC compiler. * Presented paper at AMD's internal conference (13% acceptance rate). |
| --- | --- |

# **other PROJECTS**

|  | [**GCC - GNU Compiler Collection**](https://gcc.gnu.org/)  [Google Summer Of Code](https://summerofcode.withgoogle.com/archive/)  [*Extending Csmith for GCC C-Language Extensions*](https://github.com/Sameeranjoshi/csmith/tree/gcc-extensions)*, June 2018 – April 2019*  Mentor: [Andi Kleen](http://halobates.de/)   * Added ~15 GNU C language extensions to [Csmith](https://embed.cs.utah.edu/csmith/) and found unexplored bugs (ICE’s, seg faults, crashes) in GCC compiler * Found 12 critical bugs, 11 were fixed by GCC community * Increased the fuzzing code coverage of csmith on GCC by – line coverage: 5%, function coverage: 7%, branch coverage: 4% |
| --- | --- |

# **AWARdS**

* TFWS Scholarship (awarded to 5% students of baccalaureate class) *2015-2019*
* AMD Spotlight award for performance recognition at AMD 2020

# **activities and interests**

* Volunteered at [CppOnSea’21](https://cpponsea.uk/), [CppCon’21](https://cppcon.org/)
* [2021 LLVM developers meeting](https://llvm.org/devmtg/2021-11/) PC member
* Co-founded [bitSimplify](https://bitsimplify.github.io/bitsimplify/index.html): RISC-V based LLVM toolchain startup
* Student Travel Grant for attending [Workshop on Sparse Tensor Computations](https://solomonik.cs.illinois.edu/tensor_workshop/index.html)