



**SURESH  
GYAN VIHAR  
UNIVERSITY  
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## Lab Assessment Index

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Name of Faculty :- Dr. Sandhya Sharma

Name of Course :- B.Tech (CSE)

\* Aim :- To study and verify the truth table of logic gates.

\* Apparatus required :- Digital lab kit, single stranded wire, breadboard.

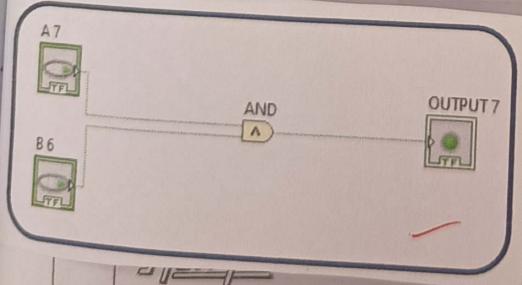
\* Theory :- Logic gates are idealized or physical device implement a Boolean function which if perform a logical operation on or more logical input and produce a single output. Depending on the context, the term may refer to an ideal logic gate.

The main hierarchy is as follow:-

1. Basic gate
2. Universal gate
3. Advance gate

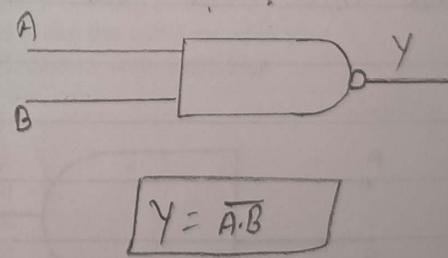
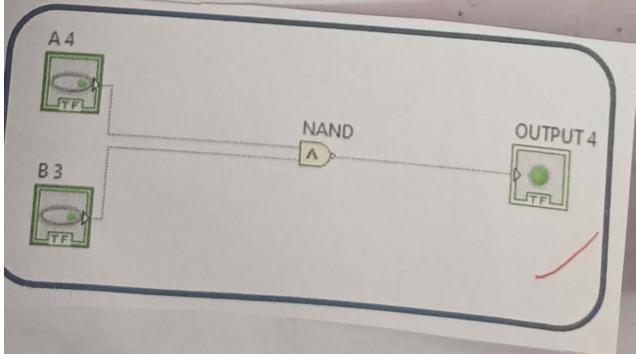
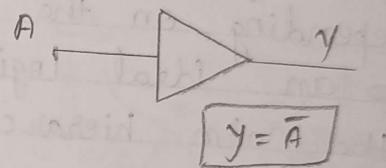
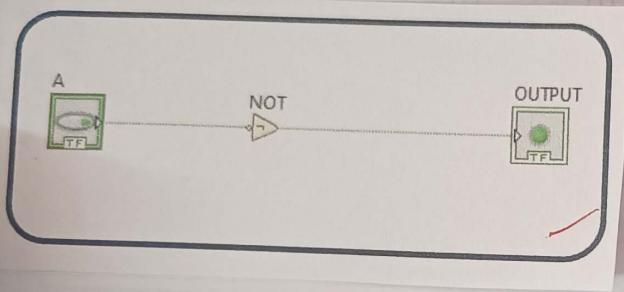
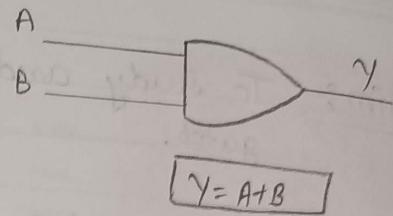
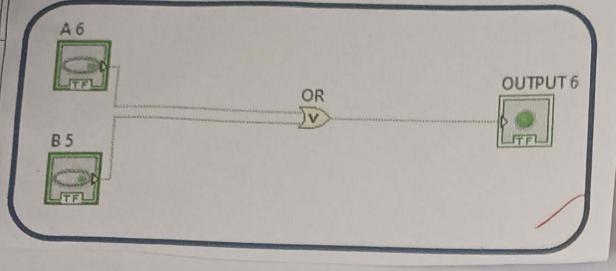
### Basic gates

1. AND gate :- Function of AND gate is to give the output true when both the inputs are true. In all other cases become false.



	A	B	output(A.B)
y	0	0	0
	0	1	0
	1	0	0
	1	1	1

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2. OR Gate:- function of OR gate is to give output true when one of the either input are true. In the remaining cases output become false.

A	B	output ( $A+B$ )
0	0	0
0	1	1
1	0	1
1	1	1

3. NOT gate :- function of NOT gate is to remove the nature of the input. It convert the true input to false and vice-versa.

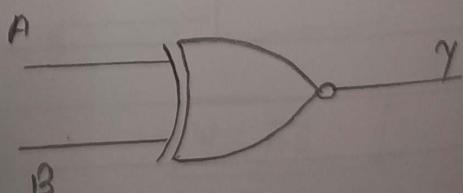
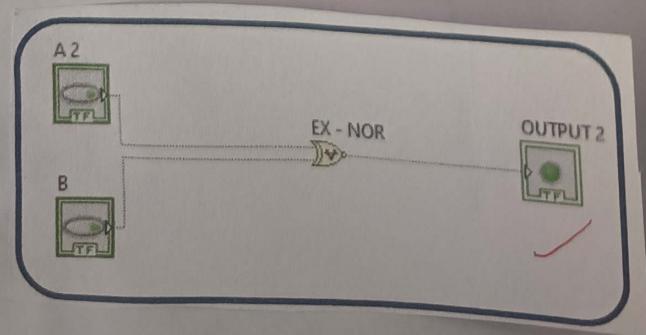
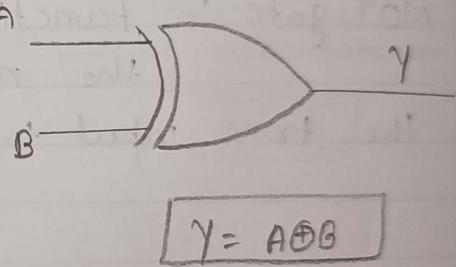
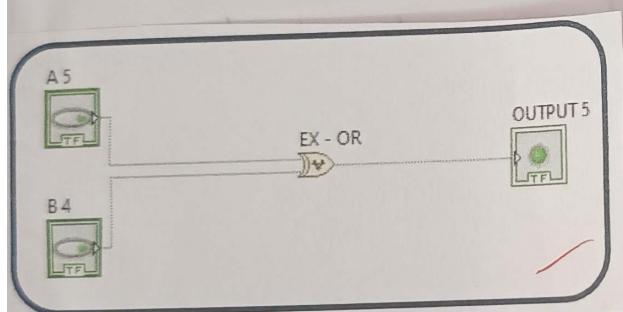
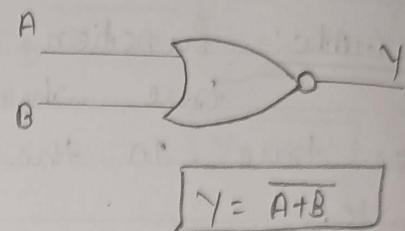
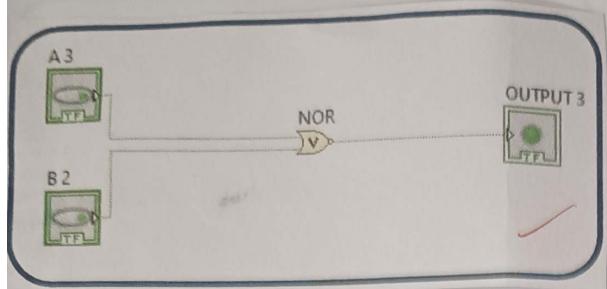
A	Output ( $\bar{A}$ )
0	1
1	0

### Universal gate.

1. NAND GATE :- function of NAND gate is to give true output when one of the two provided inputs are false.

A	B	output ( $A \cdot \bar{B}$ )
0	0	1
0	1	1
1	0	1
1	1	0

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2. NOR Gate:- NOR gate give the output true when both the two provided input are false. In all other cases output remain false.

A	B	Output ( $\bar{A} + \bar{B}$ )
0	0	1
0	1	0
1	0	0
1	1	0

### Advance Gate

1. XOR Gate:- The function of XOR gate is to give output false when both input are same otherwise true output.

A	B	Output ( $A \oplus B$ )
0	0	0
0	1	1
1	0	1
1	1	0

$$A \oplus B = A\bar{B} + \bar{A}B$$

2. EX-NOR Gate:- The function of EX-NOR gate is to give output true when both input are same.

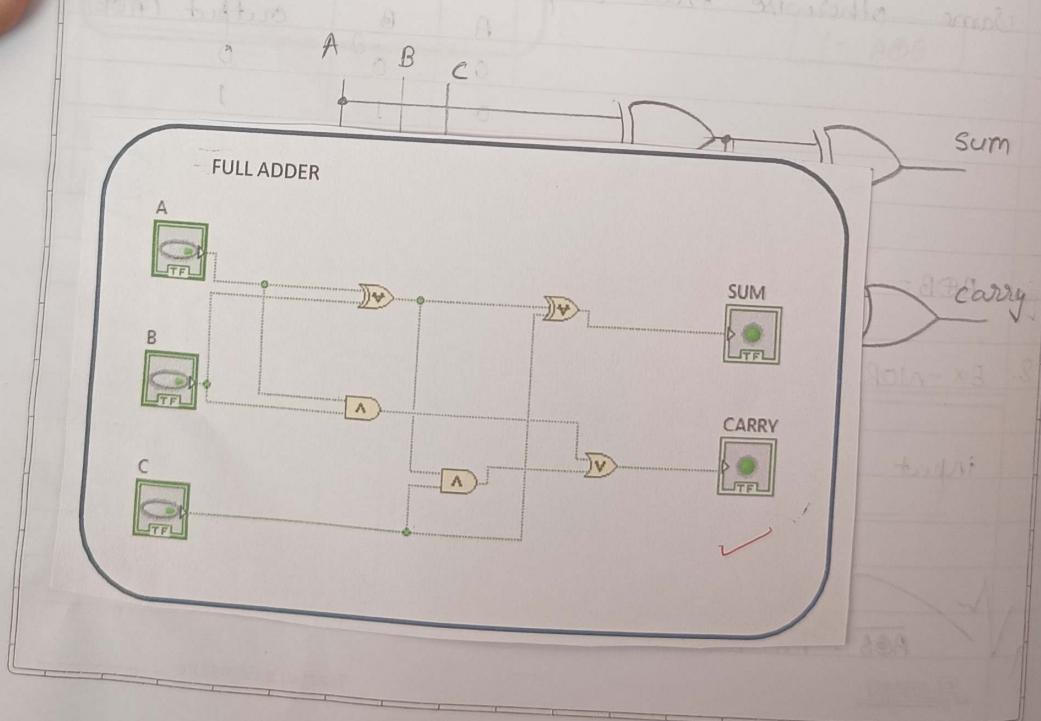
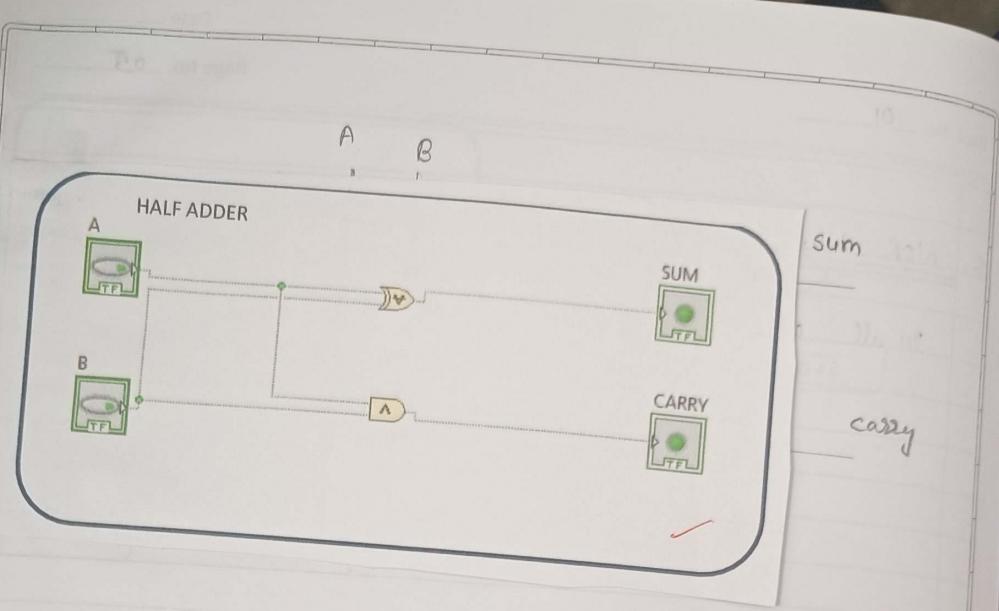
A	B	Output ( $\bar{A} \oplus \bar{B}$ )
0	0	1
0	1	0
1	0	0
1	1	1

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$$\bar{A} \oplus \bar{B} = \bar{A}\bar{B} + A\bar{B} + \bar{A}B$$

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\* Aim :- To realize

- ① Half adder and
- ② full adder

\* Theory :-

1. Half Adder :- A combinational logic circuit that performs the addition of two data bits, A and B is called a half-adder. Addition will result in two output bits; one of which is the sum bit S, and the other is carry bit C. The boolean functions describing the half adder are

$$S = A \oplus B$$

$$C = AB$$

2. Full Adder :- The half adder does not take the carry bit from the previous stage into account. The carry bit from its previous stage is called carry-in bit, A combinational logic circuit that adds two data bit, A and B and a carry-in bit. Cin. is called a full-adder.

$$S = (x \oplus y) \oplus cin$$

$$C = xy + cin(x \oplus y)$$

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1. To realize half adder.  
Truth table.

Inputs		Outputs		Boolean Expression.
A	B	S	C	
0	0	0	0	$S = A \oplus B$
0	1	1	0	$C = AB$
1	0	1	0	
1	1	0	1	

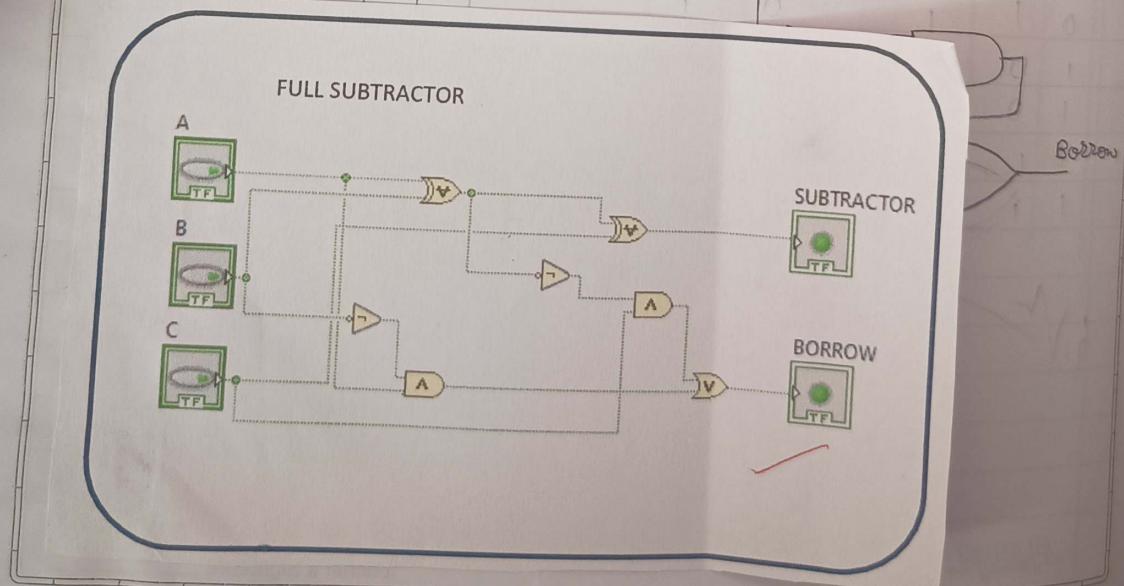
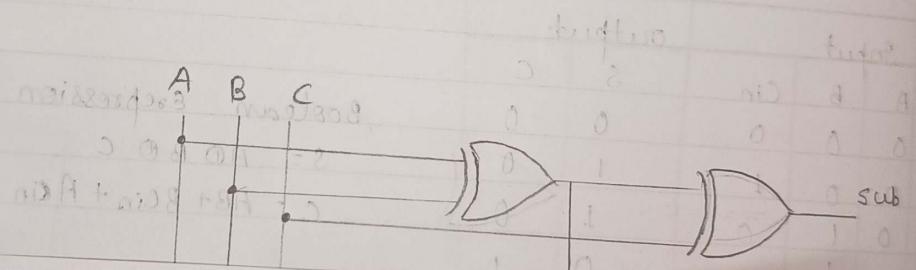
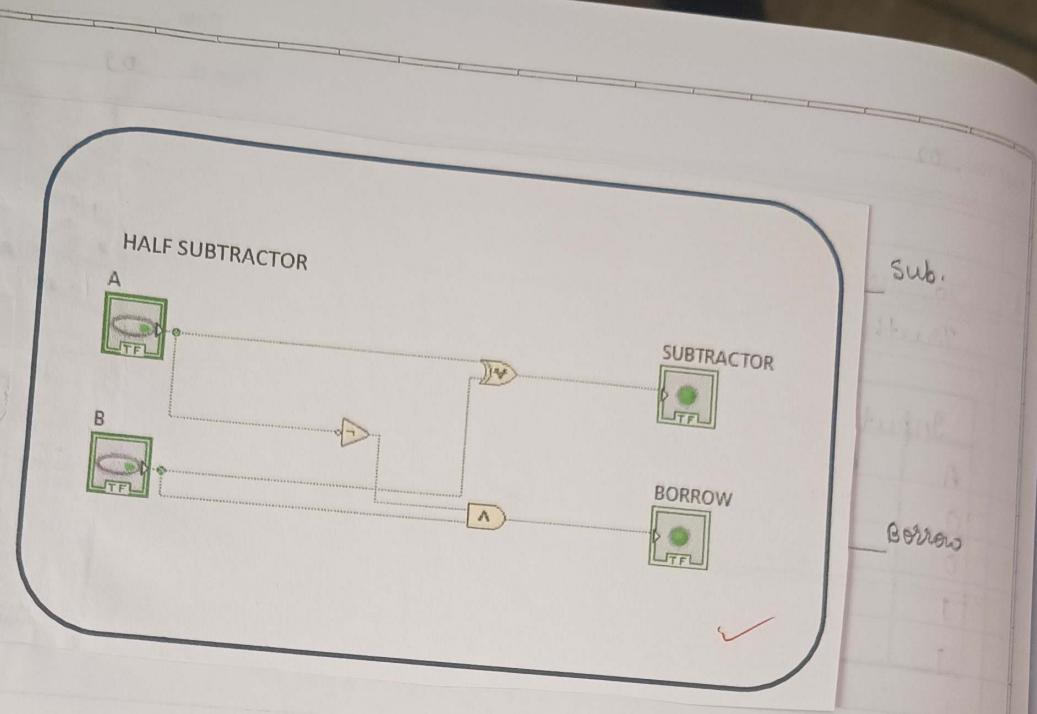
2. Full Adder

Input			Output		Boolean Expression.
A	B	Cin.	S	C	
0	0	0	0	0	$S = A \oplus B \oplus C$
0	0	1	1	0	
0	1	0	1	0	$C = AB + BC_{in} + AC_{in}$
0	1	1	0	1	
1	0	0	1	0	
1	0	1	0	1	
1	1	0	0	1	
1	1	1	1	1	

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\* A/P :- To realize

- ① Half subtractor and
- ② full subtractor.

\* Theory :-

1. Half Subtractor :- Subtracting a single bit binary value B from another A produce a difference bit D and a borrow bit B-out. This operation is called half subtraction and circuit to realize is called half subtractor.

$$S = A \oplus B$$

$$C = A' B$$

2. full subtractor :- Subtracting two single bit binary value B, Cin. from a single bit value A produce a difference bit D and a borrow bit. This is called full subtraction.

$$D = (x \oplus y) \oplus \text{Cin}$$

$$B_2 = A'B + A'(\text{Cin}) + B(\text{Cin})$$

\* Half subtractor  
Truth table:-

Inputs		outputs	
A	B	D	B <sub>r</sub>
0	0	0	0
0	1	1	1
1	0	1	0
1	1	0	0

Boolean expression.

$$D = A \oplus B$$

$$B_r = \bar{A}B$$

\* Full subtractor :-

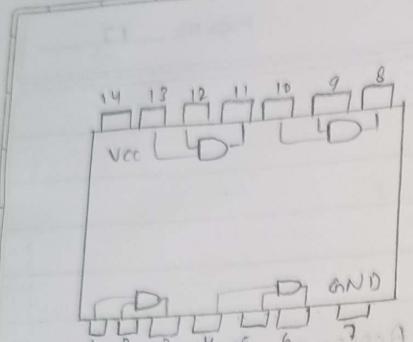
Truth table:-

Inputs			outputs		
A	B	Cin.	D	B <sub>r</sub>	
0	0	0	0	0	<u>Boolean expression.</u>
0	0	1	1	1	
0	1	0	1	1	$D = A \oplus B \oplus \text{Cin.}$
0	1	1	0	1	$B_r = \bar{A}B + B\bar{C}_{in} + \bar{A}\bar{C}_{in}$
1	0	0	1	0	
1	0	1	0	0	
1	1	0	0	0	
1	1	1	1	1	

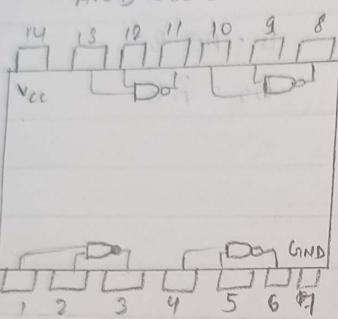
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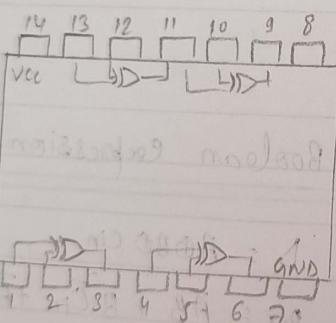
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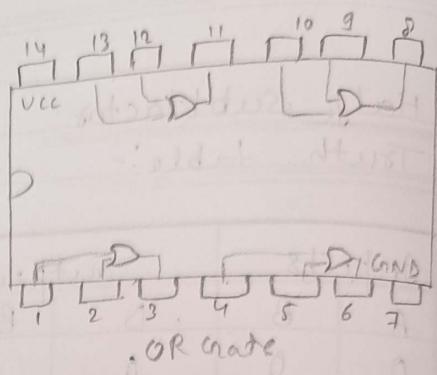
AND Gate



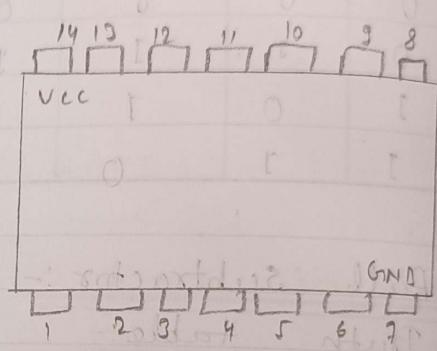
NAND Gate



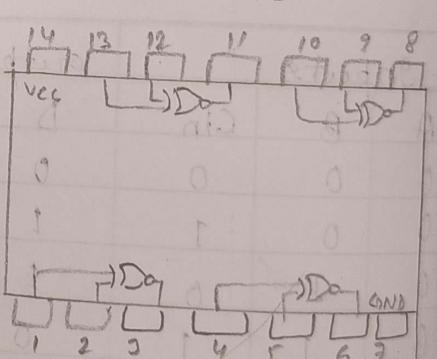
XOR Gate



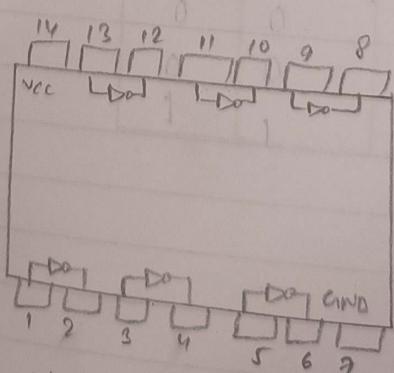
OR Gate



NOR Gate



XNOR Gate



NOT Gate  
(Inverters)

7404

Alm :- ICs of logic gates :-

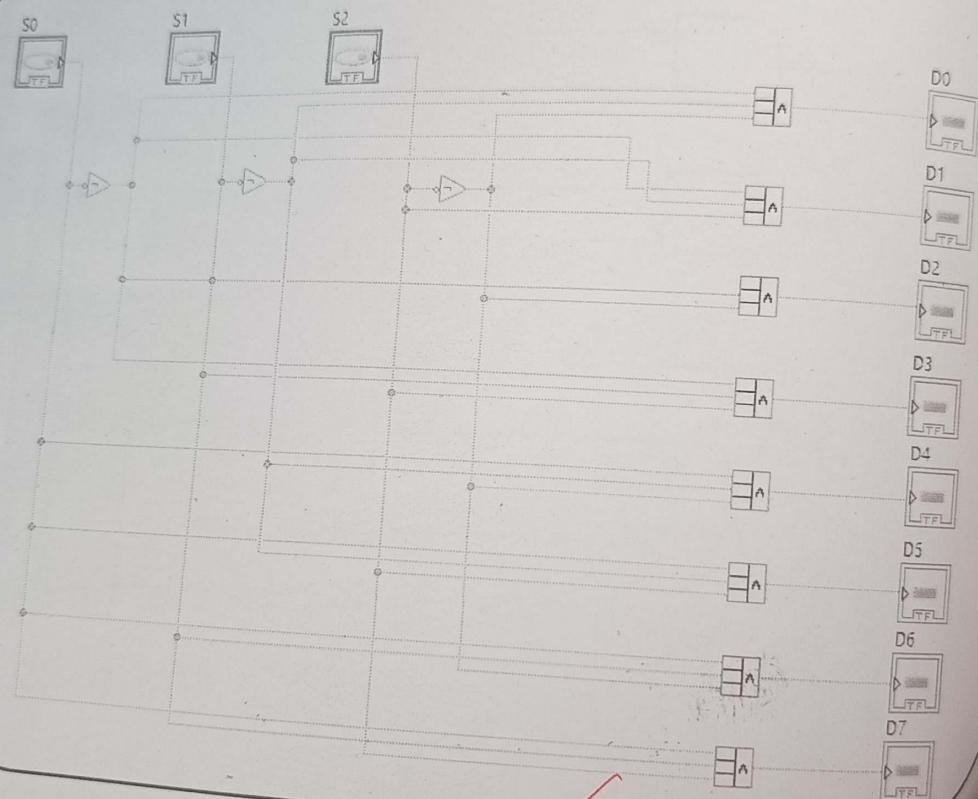
Number	Description
7400	Orued two-input NAND gate (four NAND gates)
7402	Orued two-input NOR gate (four NOR gates)
7404	Hex Inverter (six NOT gate)
7408	Orued two-input AND gate (four AND gate)
7432	Orued two-input OR gate (four OR gates)
7486	Orued two-input XOR gate (four XOR gates)

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DECODER 3:8



Aim :- Implementation and verification of decoder using logic gates.

Apparatus :- Digital trainer kit, 7432 IC, 7404 IC, 7411 IC and connecting wires.

Theory :-

A decoder is a multi-input and multi-output combinational logic circuit which converts coded input into coded outputs, where the input and output codes are different.

INPUTS			OUTPUTS			
$\bar{E}_N$	B	A	$\bar{Y}_0$	$\bar{Y}_1$	$\bar{Y}_2$	$\bar{Y}_3$
0	0	0	0	1	1	1
0	0	1	1	0	1	1
0	1	0	1	1	0	1
0	1	1	1	1	1	0
1	X	X	1	1	1	1

$\rightarrow$  Dont care state

Procedure :- connect the supply from the trainer kit through patch cords; also connect circuit as per circuit diagram.

- drive the input to A, B and EN through switch.
- observe the output  $Y_0$  to  $Y_3$  on the trainer kit through LEDs.

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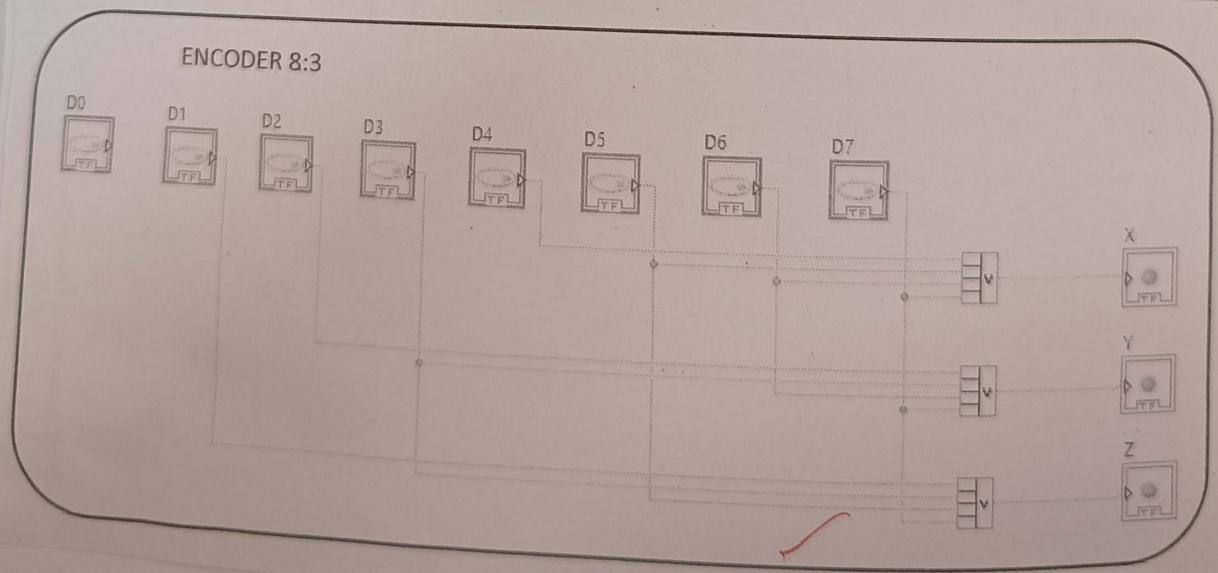
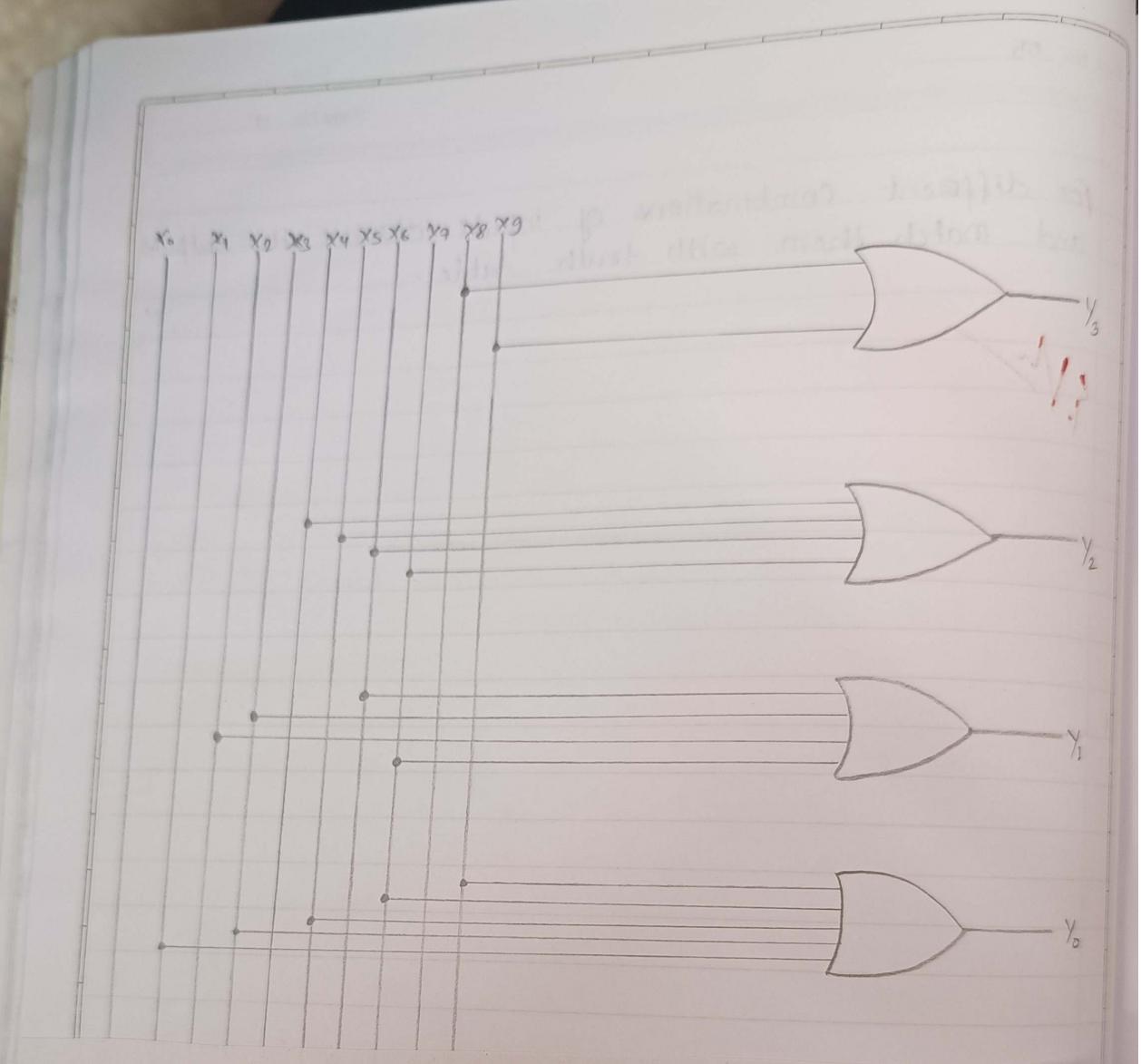
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for different combinations of inputs observe the outputs  
and match them with truth table.

g. V



Aim :- Implementation and verification of encoder using logic gates.

Apparatus :- Digital trainer kit, 7432 IC, 7404 IC, 7413 IC and connecting wires.

Theory :-

An encoder is a combinational logic circuit. It is the reverse of a decoder function. It has  $2^n$  to the power n input and n output lines. An encoder accepts an active level on one of its inputs representing a digit such as a decimal / octal digit and it converts to coded output.

Inputs							Outputs		
D <sub>0</sub>	D <sub>1</sub>	D <sub>2</sub>	D <sub>3</sub>	D <sub>4</sub>	D <sub>5</sub>	D <sub>6</sub>	X	Y	Z
1	0	0	0	0	0	0	0	0	0
0	1	0	0	0	0	0	0	0	1
0	0	1	0	0	0	0	0	1	0
0	0	0	1	0	0	0	1	0	0
0	0	0	0	1	0	0	1	0	1
0	0	0	0	0	1	0	1	1	0
0	0	0	0	0	0	1	1	1	1

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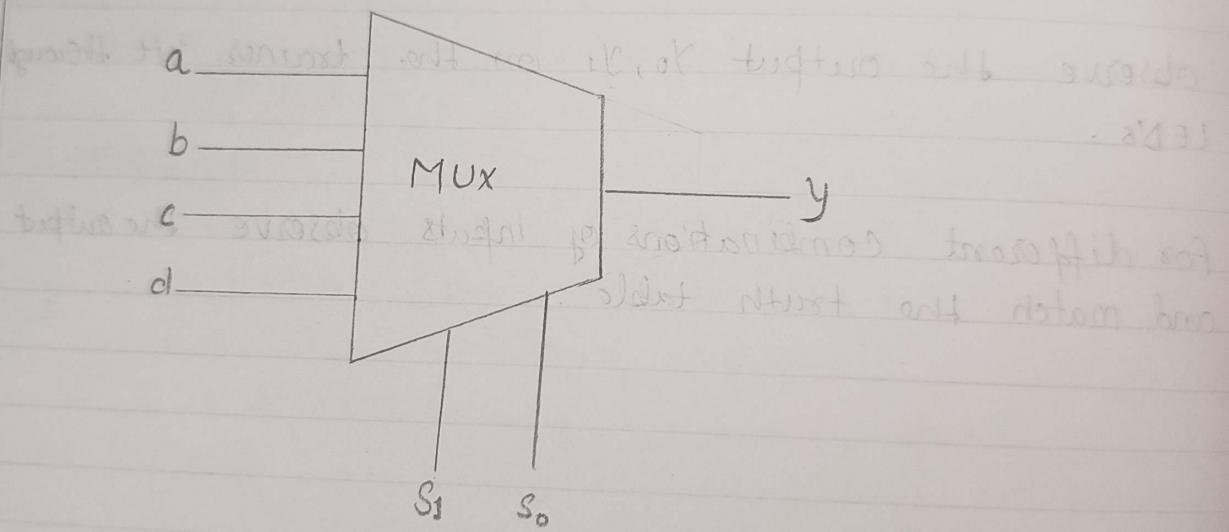
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• Procedure :-

1. connect the supply from the trainer kit through patch chords; also connect circuit as per circuit diagram.
2. Give the input connections to 10, 11, 12 and 13.
3. observe the output  $Y_0, Y_1$  on the trainer kit through LED's.
4. For different combinations of inputs observe the output and match the truth table.



Block diagram of multiplexer:-

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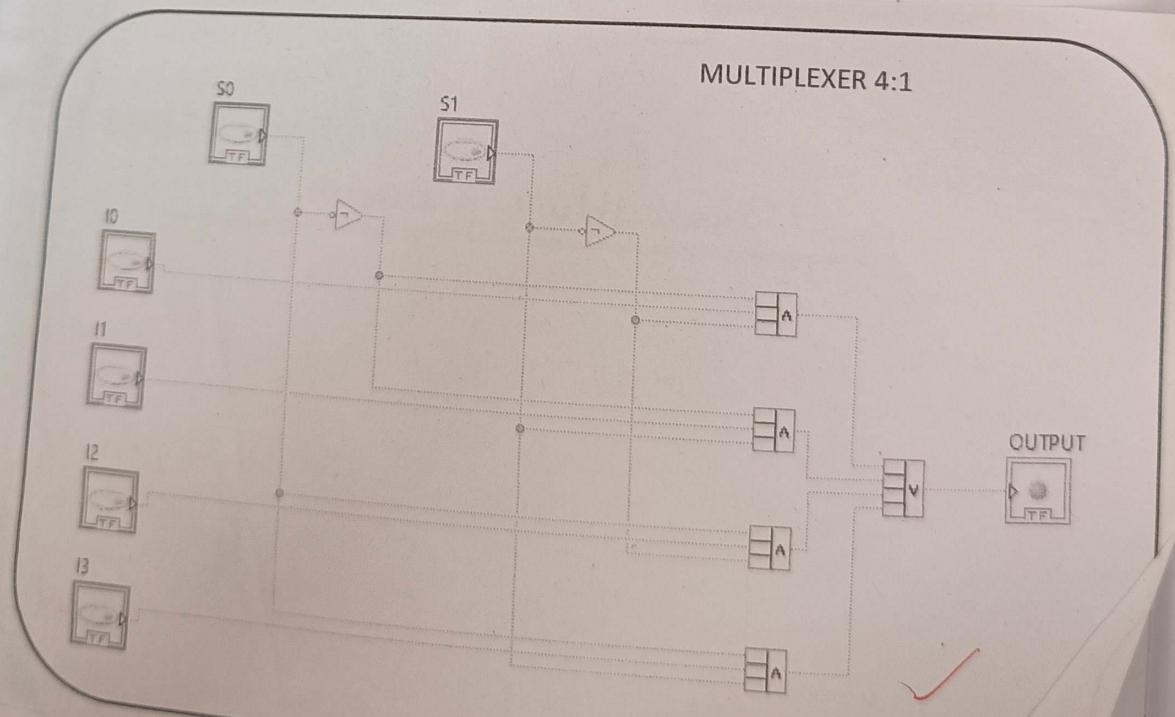
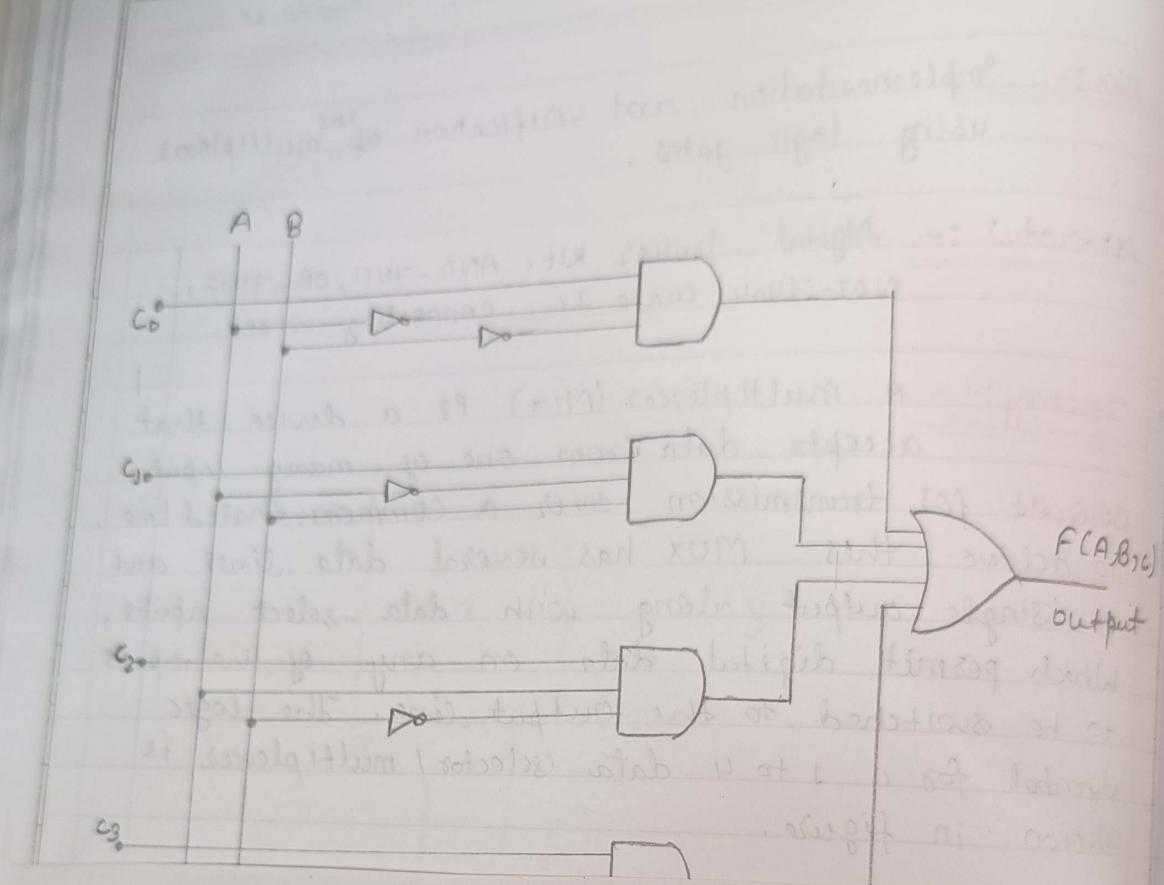
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- Aim :- Implementation and verification of multiplexer using logic gates.
- Apparatus :- Digital trainer kit, AND-7411, OR-7432, NOT-7404 gate IC, connecting wires.
- Theory :- A multiplexer (MUX) is a device that accepts data from one of many input sources for transmission over a common shared line. To achieve this MUX has several data lines and a single output along with data-select inputs, which permit digital data on any of the inputs to be switched to the output line. The logic symbol for a 1 to 4 data selector/multiplexer is shown in figure.
- Truth table :-

Data in selected input		Input selected
$S_1$	$S_0$	
0	0	$D_0$
0	1	$D_1$
1	0	$D_2$
1	1	$D_3$

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- Procedure :-

1. Connection are made as per circuit diagram.
2. Verify the truth table.
3. Also connect Vcc and Ground then performed experiment.

- Result :- Study of 4x1 multiplexers and verified its truth table.

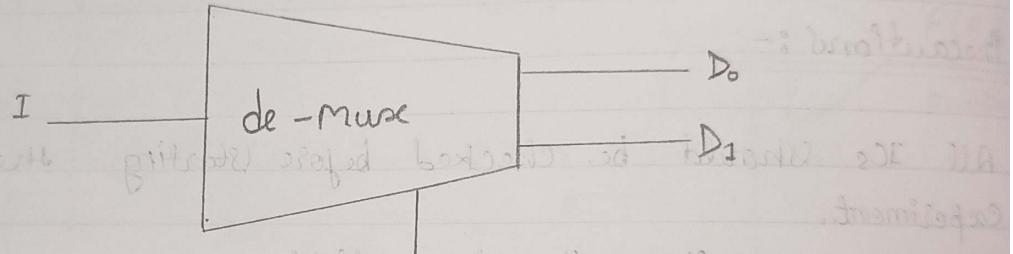
- Precautions :-

1. All ICs should be checked before starting the experiment.
2. All the connection should be tight.
3. Always connect ground first and then connect Vcc.
4. Suitable type wire should be used for different types of circuit.
5. The kit should be off before change the connection.
6. After completed the experiments switch off the supply of the apparatus.

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Block diagram of demultiplexers :-

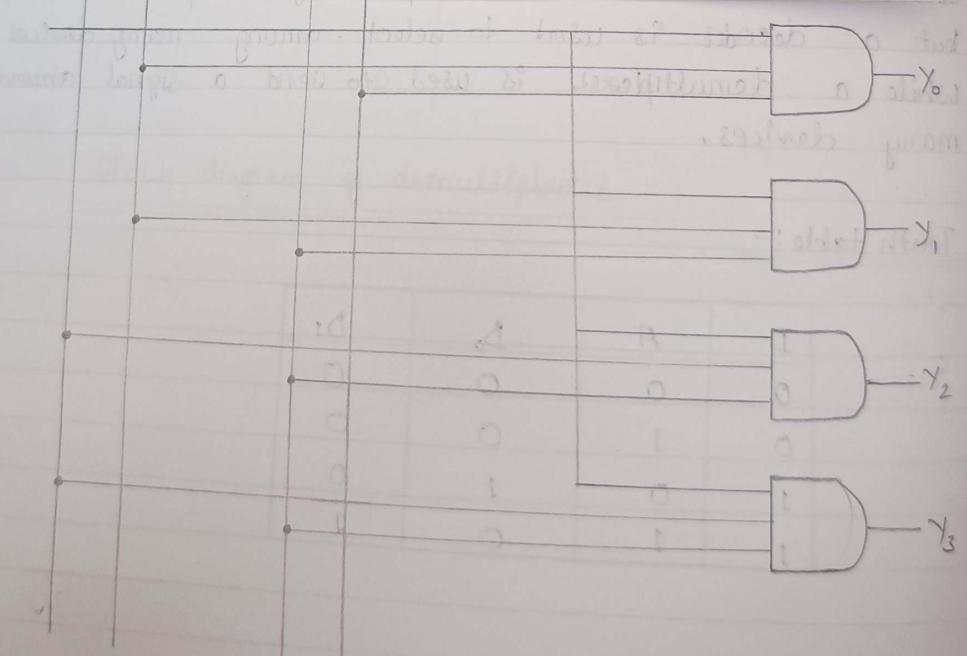
- Aim:- Implementation and verification of de-multiplexer using logic gates.
- Apparatus:- Digital trainer kit, 7432 IC, 7404 IC, 7411 IC and connecting wires.
- Theory:-

A de-multiplexer sometimes abbreviated d-mux, is a circuit that has one input and more than one output. It is used when a circuit wishes to send a single to one of many devices. This description sounds similar to the description given for a decoder, but a decoder is used to select among many devices while a demultiplexer is used to send a signal among many devices.

- Truth table:-

I	A	D <sub>0</sub>	D <sub>1</sub>
0	0	0	0
0	1	0	0
1	0	1	0
1	1	0	1

DE-MULTIPLEXER 1:4



CKT diagram of 1:4 de-multiplexer.

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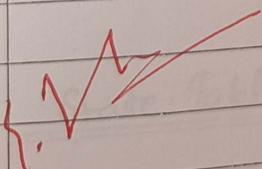
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• Procedure:-

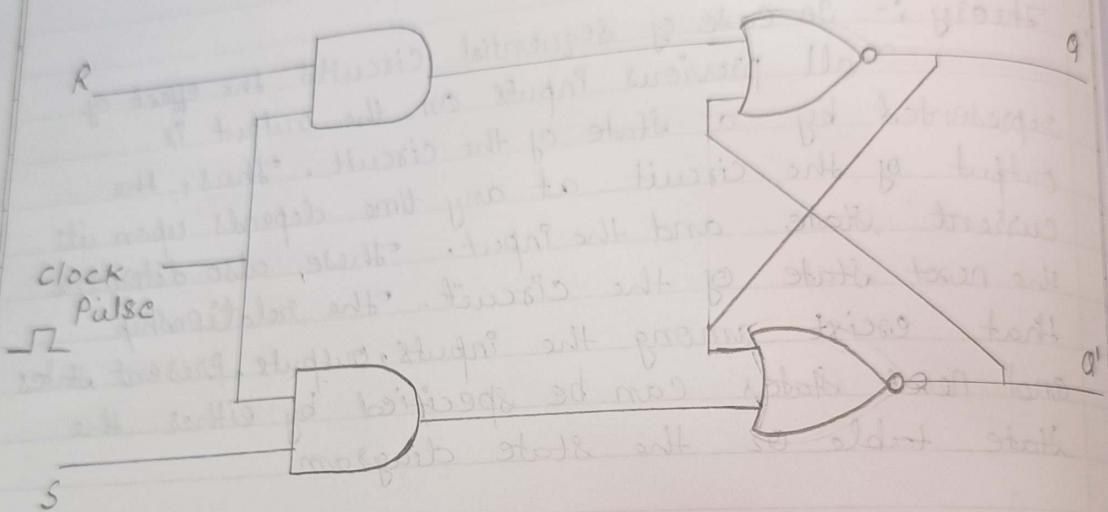
1. Connect the supply from the trainer kit through patch chords, also connect circuit as per circuit diagram.
2. Give input connections at I<sub>1</sub> and at Selection line.
3. Observe the output D<sub>0</sub>, D<sub>1</sub> on the trainer kit through LED's.
4. For different combinations of inputs observe the output and match the truth table.

• Result:- Truth tables of de-multiplexers are verified.

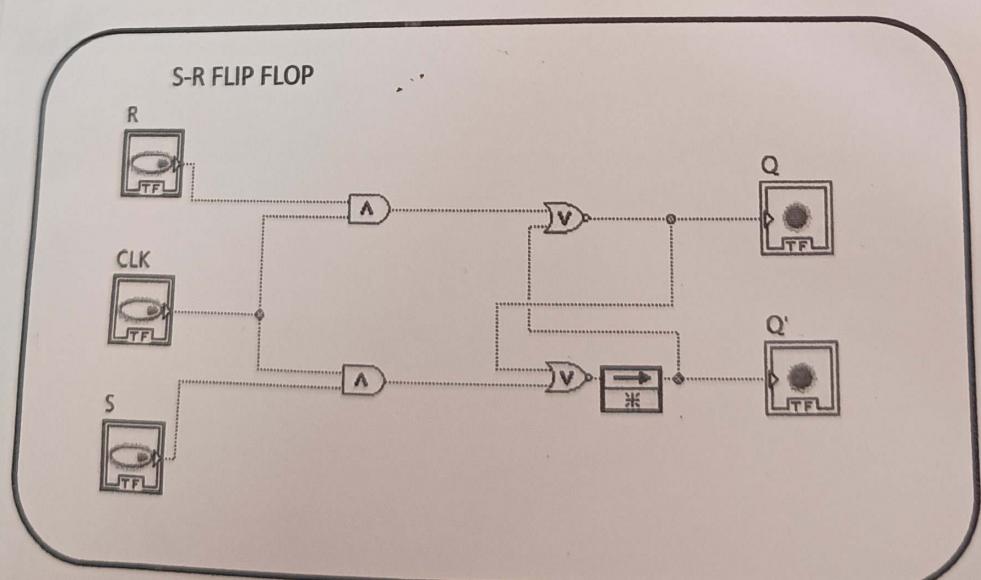


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- Aim :- verification of state tables of R-S flip-flop using NAND and NOR gates.
- Apparatus :- IC 7400 (NAND gate), IC 7402 (NOR gate), IC 7408 (AND gate).
- Theory :- In case of sequential circuits the effect of all previous inputs on the output is represented by a state of the circuit. Thus, the output of the circuit at any time depends upon its current state and the input. These also determine the next state of the circuit. The relationship that exist among the inputs, outputs, present states and next states can be specified by either the state table or the state diagram.
- State Table :- The state table representation of a sequential circuit consists of three sections labelled present state next state and output. The present state designates the state of flip-flops before the occurrence of a clock pulse. The next state shows the states of flip-flops after the clock pulse, and the output section lists the value of the output variables during the present state.



Logic diagram of SR flip-flop



- **flip-flop:-** The basic one bit digital memory circuit is known as flip-flop. It can store either 0 or 1. flip-flops are classified according to the number of inputs.
- **R-S flip-flop:-** The circuit is similar to SR latch except enable signal is replaced by clock pulse.
- Characteristic table for S-R flip-flop:-

$Q$	$S$	$R$	$Q(t+1)$
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	Indeterminate
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	Indeterminate.

- **Procedure:-** Connections are made as per circuit diagram.
- Verify truth-tables for various combinations of input.
- **Result:-** Study and verified truth-tables of various flip-flops.

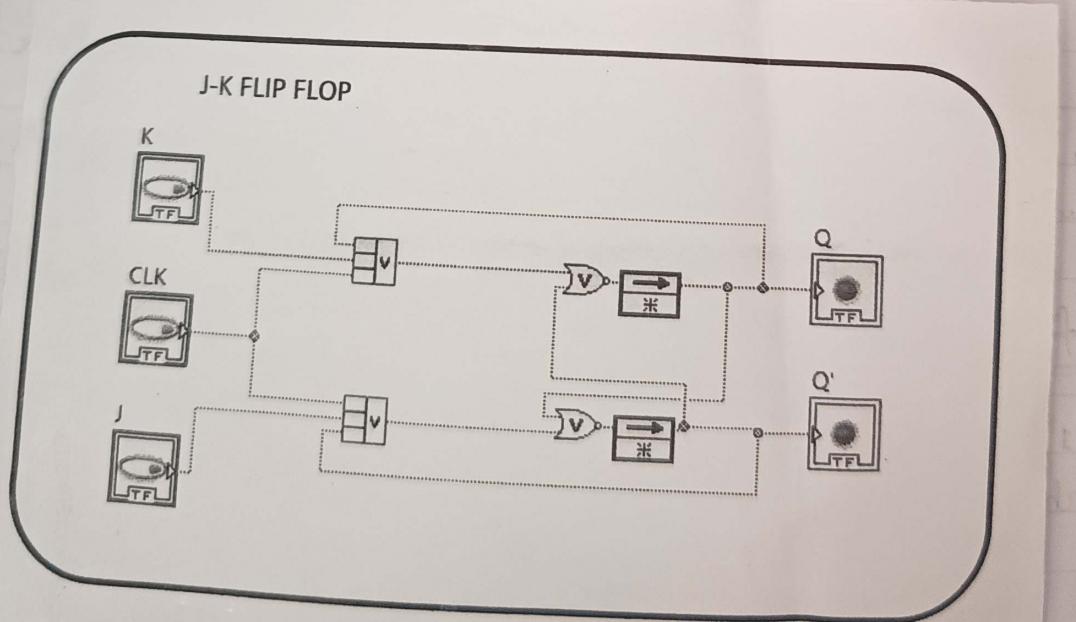
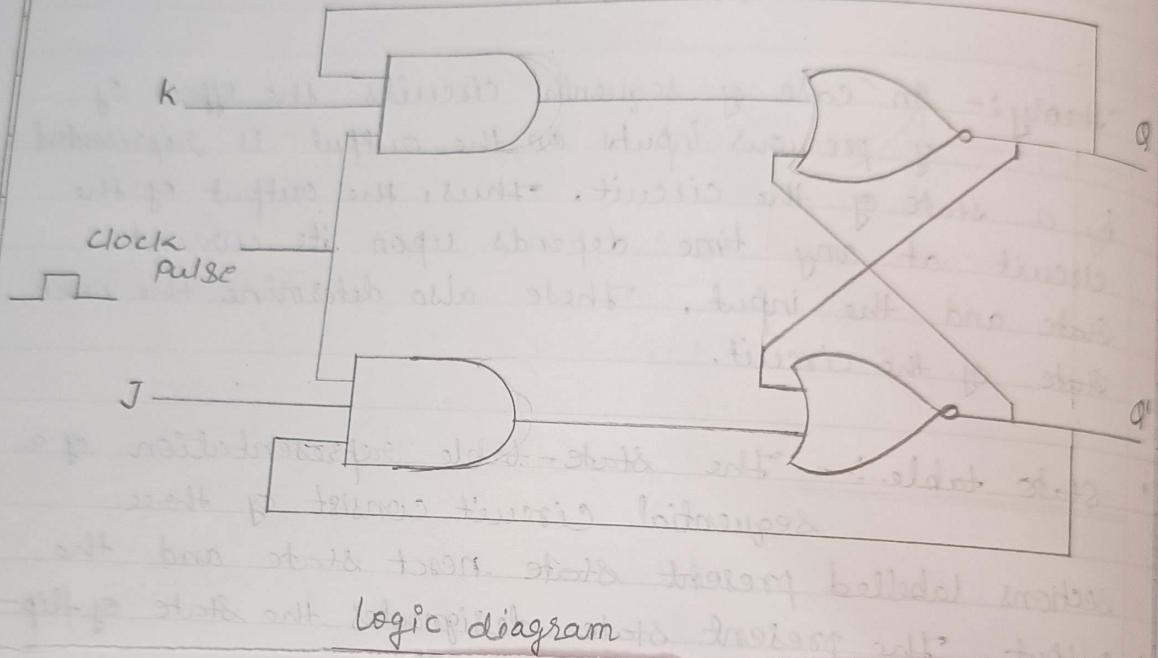
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- Aim :- verification of state tables of J-K flip-flops using NAND and NOR gates.
- Apparatus :- IC 7400(NAND Gate), IC 7402 (NOR gate), IC 7408 (AND gate).
- Theory :- In case of sequential circuits the effect of previous inputs on the output is represented by a state of the circuit. Thus, the output of the circuit at any time depends upon its current state and the input. These also determine the next state of the circuit.
- State table :- The state-table representation of a sequential circuit consist of three sections labelled present state, next state and the output. The present state designates the state of flip-flops before the occurrence of a clock pulse. The next state shows the state of flip-flops after the clock pulse, and the output section list the value of the output variables during the present state.
- flip-flop :- The basic one bit digital memory circuit is known as flip-flop. It can store either 0 or 1. flip-flops are classified according to the number of inputs.

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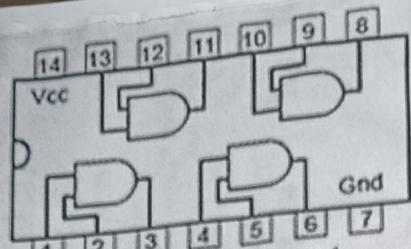
- J-K flip-flop:- In a R-S flip-flop the input  $R=S=1$  leads to an indeterminate output. The R-S flip-flop circuit may be re-jointed if both inputs are 1 than also the outputs are complement of each other.

- Characteristic table for J-K flip-flop:-

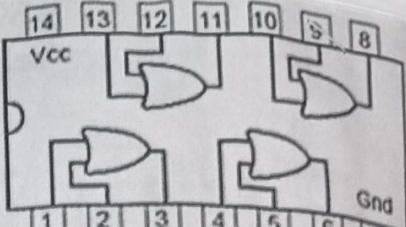
$Q$	$J$	$K$	$Q(t+1)$
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	0

- Procedure:- Connections are made as per circuit diagram.
- Verify truth-tables for various combinations of input.
- Result:- Study and verified truth-tables of various flip-flops.

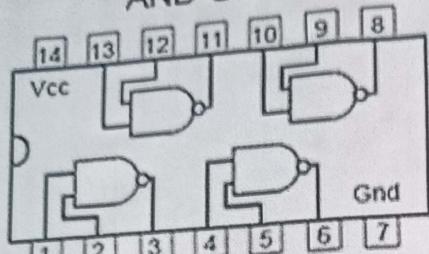
Teacher's Signature \_\_\_\_\_



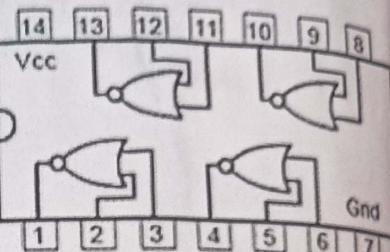
7408 Quad 2 input  
AND Gates



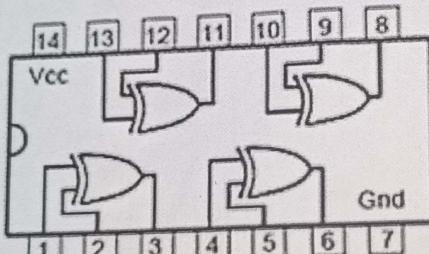
7432 Quad 2 input  
OR Gates



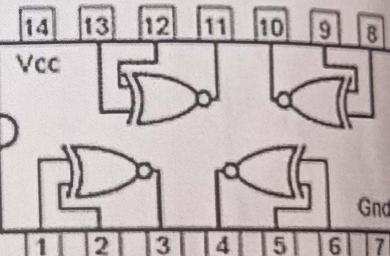
7400 Quad 2 input  
NAND Gates



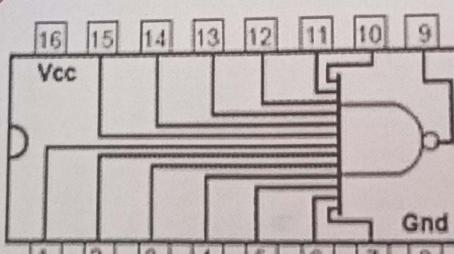
7402 Quad 2 input  
NOR Gates



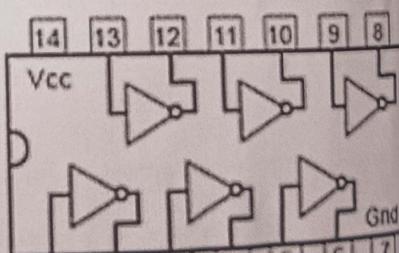
7486 Quad 2 input  
XOR Gates



747266 Quad 2 input  
XNOR Gates



74133 Single 13 input  
—NAND Gate



7404 Hex NOT Gates  
(Inverters)