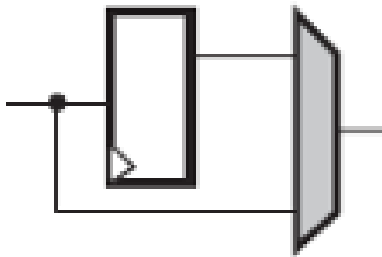


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1 DSP's RTL

1.1 Register-Mux Stage



```
1 module reg_mux_stage (data,clk,rst,mux_out,clk_en,sel);
2
3     parameter D_WIDTH = 18;
4     parameter RSTTYPE = "SYNC";
5
6     input [D_WIDTH-1 : 0] data;
7     input rst,clk,clk_en,sel;
8     output [D_WIDTH-1 : 0] mux_out;
9
10    reg [D_WIDTH-1 : 0] data_reg;
11
12    assign mux_out = (sel) ? data_reg : data;
13
14    generate
15        if (RSTTYPE == "SYNC") begin
16            always @(posedge clk) begin
17                if (rst)
18                    data_reg <= 0;
19                else if (clk_en)
20                    data_reg <= data;
21            end
22        end else if (RSTTYPE == "ASYNC") begin
23            always @(posedge clk or posedge rst) begin
24                if (rst)
25                    data_reg <= 0;
26                else if (clk_en)
27                    data_reg <= data;
28            end
29        end
30    endgenerate
31
32 endmodule : reg_mux_stage
```

1.2 DSP

```
1 module DSP48A1 (A,B,C,D,CARRYIN,M,P,CARRYOUT,CARRYOUTF,CLK,OPMODE,CEA,CEB,CEC,CECARRYIN,CED,CEM,CEP,CEOPMODE
2 ,RSTA,RSTB,RSTC,RSTCARRYIN,RSTD,RSTM,RSTP,RSTOPMODE,BCIN,BCOUT,PCIN,PCOUT);
3
4 parameter A0REG=0, A1REG=1, B0REG=0, B1REG=1, CREG=1, DREG=1, MREG=1, PREG=1, CARRYINREG=1, CARRYOUTREG=1, OPMODEREG=1;
5 parameter CARRYINSEL = "OPMODE5", B_INPUT = "DIRECT", RSTTYPE = "SYNC";
6
7 input [17:0] A,B,D,BCIN;
8 input [47:0] C,PCIN;
9 input CARRYIN,CLK,CEA,CEB,CEC,CECARRYIN,CED,CEM,CEP,CEOPMODE,RSTA,RSTB,RSTC,RSTCARRYIN,RSTD,RSTM,RSTP,RSTOPMODE;
10 input [7:0] OPMODE;
11 output [35:0] M;
12 output [47:0] P,PCOUT;
13 output [17:0] BCOUT;
14 output CARRYOUT,CARRYOUTF;
15
16 wire [17:0] A0_mux_out,B0_mux1_out,D_mux_out,B0_mux0_out,ALU0_out,mux_opmode4_out,B1_mux_out,A1_mux_out;
17 wire [47:0] C_mux_out,ALU1_out;
18 wire [35:0] multiply_out,M_mux_out;
19 wire [7:0] OPMODE_mux_out;
20 wire mux_carryin_out,Cin_mux_out,CYO,CYO_mux_out;
21 reg [47:0] mux_x_out,mux_z_out;
22
23 reg_mux_stage #(.RSTTYPE(RSTTYPE),.D_WIDTH(18)) A0_SIG (A,CLK,RSTA,A0_mux_out,CEA,A0REG);
24 reg_mux_stage #(.RSTTYPE(RSTTYPE),.D_WIDTH(18)) B0_SIG (B0_mux0_out,CLK,RSTB,B0_mux1_out,CEB,B0REG);
25 reg_mux_stage #(.RSTTYPE(RSTTYPE),.D_WIDTH(48)) C_SIG (C,CLK,RSTC,C_mux_out,CEC,CREG);
26 reg_mux_stage #(.RSTTYPE(RSTTYPE),.D_WIDTH(18)) D_SIG (D,CLK,RSTD,D_mux_out,CED,DREG);
27 reg_mux_stage #(.RSTTYPE(RSTTYPE),.D_WIDTH(8)) OPMODE_SIG (OPMODE,CLK,RSTOPMODE,OPMODE_mux_out,CEOPMODE,OPMODEREG);
28 reg_mux_stage #(.RSTTYPE(RSTTYPE),.D_WIDTH(18)) A1_SIG (A0_mux_out,CLK,RSTA,A1_mux_out,CEA,A1REG);
29 reg_mux_stage #(.RSTTYPE(RSTTYPE),.D_WIDTH(18)) B1_SIG (mux_opmode4_out,CLK,RSTB,B1_mux_out,CEB,B1REG);
30 reg_mux_stage #(.RSTTYPE(RSTTYPE),.D_WIDTH(36)) M_SIG (multiply_out,CLK,RSTM,M_mux_out,CEM,MREG);
31 reg_mux_stage #(.RSTTYPE(RSTTYPE),.D_WIDTH(1)) CVI_SIG (mux_carryin_out,CLK,RSTCARRYIN,Cin_mux_out,CECARRYIN,CARRYINREG);
32 reg_mux_stage #(.RSTTYPE(RSTTYPE),.D_WIDTH(1)) CYO_SIG (CYO,CLK,RSTCARRYIN,CYO_mux_out,CECARRYIN,CARRYOUTREG);
33 reg_mux_stage #(.RSTTYPE(RSTTYPE),.D_WIDTH(48)) P_SIG (ALU1_out,CLK,RSTP,PCOUT,CEP,PREG);
34
35
36 assign B0_mux0_out = (B_INPUT == "DIRECT") ? B :
37 (B_INPUT == "CASCADE") ? BCIN : 0;
38
39 assign ALU0_out = (OPMODE_mux_out[6] == 0) ? (D_mux_out + B0_mux1_out) : (D_mux_out - B0_mux1_out);
40 assign mux_opmode4_out = (OPMODE_mux_out[4] == 0) ? B0_mux1_out : ALU0_out;
41 assign BCOUT = B1_mux_out;
42 assign multiply_out = A1_mux_out * B1_mux_out;
43 assign M = M_mux_out;
44 assign mux_carryin_out = (CARRYINSEL == "CARRYIN") ? CARRYIN :
45 (CARRYINSEL == "OPMODE5") ? OPMODE_mux_out[5] : 0;
46
47 always @(*) begin
48 case (OPMODE_mux_out[1:0])
49 2'b00 : mux_x_out = 0;
50 2'b01 : mux_x_out = {(12{1'b0}),M_mux_out};
51 2'b10 : mux_x_out = PCOUT;
52 2'b11 : mux_x_out = {D_mux_out[11:0],A1_mux_out,B1_mux_out};
53 default : mux_x_out = 0;
54 endcase
55
56 case (OPMODE_mux_out[3:2])
57 2'b00 : mux_z_out = 0;
58 2'b01 : mux_z_out = PCIN;
59 2'b10 : mux_z_out = PCOUT;
60 2'b11 : mux_z_out = C_mux_out;
61 default : mux_z_out = 0;
62 endcase
63 end
64
65 assign {CYO,ALU1_out} = (OPMODE_mux_out[7]) ? (mux_z_out - (mux_x_out+Cin_mux_out)) : (mux_x_out + mux_z_out + Cin_mux_out);
66 assign CARRYOUT = CYO_mux_out;
67 assign CARRYOUTF = CYO_mux_out;
68 assign P = PCOUT;
69
70
71 endmodule : DSP48A1
```

2 DSP's Testbench

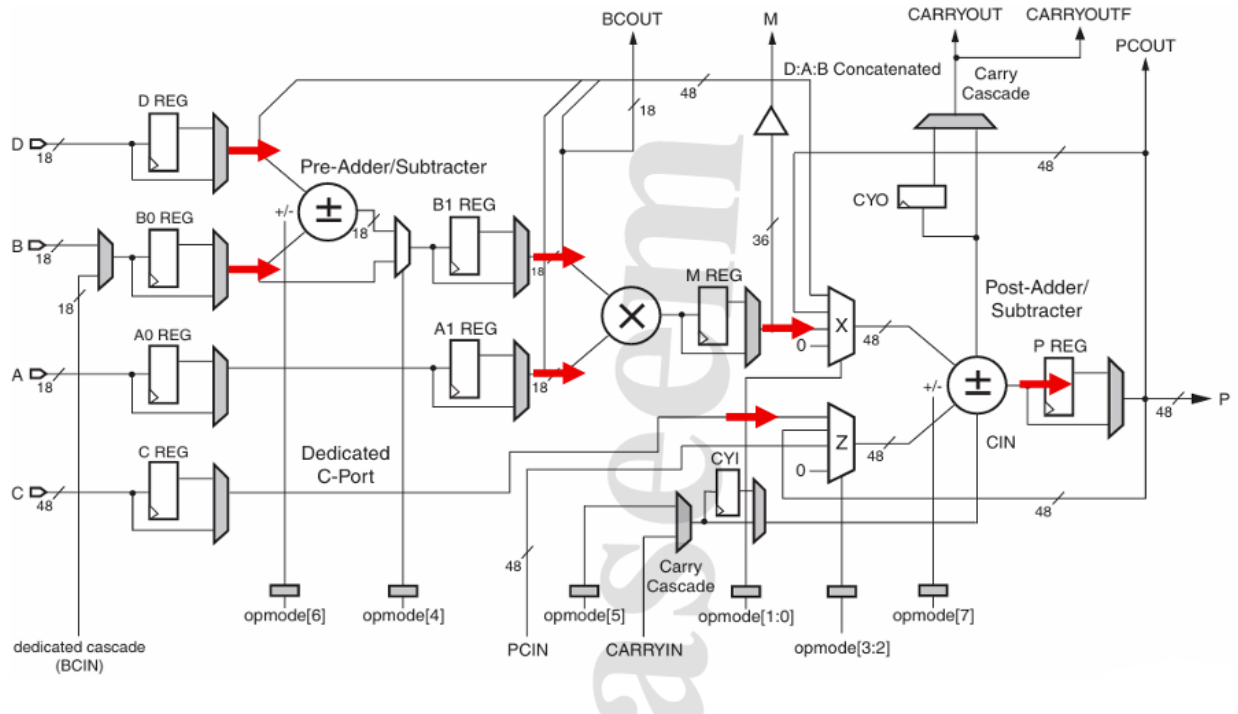
2.1 Tb signals, Instantiation and Clock generation

```
1 module DSP48A1_tb ();
2
3     reg [17:0] A,B,D,BCIN;
4     reg [47:0] C,PCIN;
5     reg CARRYIN,CLK,CEA,CEB,CEC,CECARRYIN,CED,CEM,CEP,CEOPMODE,RSTA,RSTB,RSTC,RSTCARRYIN,RSTD,RSTM,RSTP,RSTOPMODE;
6     reg [7:0] OPMODE;
7
8     wire [35:0] M;
9     wire [47:0] P,PCOUT;
10    wire [17:0] BCOUT;
11    wire CARRYOUT,CARRYOUTF;
12
13    reg [35:0] M_exp;
14    reg [47:0] P_exp,PCOUT_exp;
15    reg [17:0] BCOUT_exp;
16    reg CARRYOUT_exp,CARRYOUTF_exp;
17
18    DSP48A1 dut (A,B,C,D,CARRYIN,M,P,CARRYOUT,CARRYOUTF,CLK,OPMODE,CEA,CEB,CEC,CECARRYIN,CED,CEM,CEP,CEOPMODE
19                ,RSTA,RSTB,RSTC,RSTCARRYIN,RSTD,RSTM,RSTP,RSTOPMODE,BCIN,BCOUT,PCIN,PCOUT);
20
21    initial begin
22        CLK = 0;
23        forever #5 CLK = ~CLK;
24    end
```

2.2 Reset check

```
26    initial begin
27        // reset check
28        RSTA = 1; RSTB = 1; RSTC = 1; RSTD = 1; RSTM = 1; RSTP = 1; RSTOPMODE = 1; RSTCARRYIN = 1;
29
30        A = $random(); B = $random(); C = $random(); D = $random();
31        BCIN = $random(); CARRYIN = $random(); PCIN = $random(); OPMODE = $random();
32
33        CEA = $random(); CEB = $random(); CEC = $random(); CED = $random(); CECARRYIN = $random(); CEM = $random();
34        CEP = $random(); CEOPMODE = $random();
35
36        M_exp = 0; P_exp = 0; PCOUT_exp = 0; BCOUT_exp = 0; CARRYOUT_exp = 0; CARRYOUTF_exp = 0;
37
38        @(negedge CLK);
39
40        if ((M == M_exp) && (P == P_exp) && (PCOUT == PCOUT_exp) && (BCOUT == BCOUT_exp) &&
41            (CARRYOUT == CARRYOUT_exp) && (CARRYOUTF == CARRYOUTF_exp))
42            $display("reset test passed");
43        else begin
44            $display("error in reset");
45            $stop();
46        end
47
48        RSTA = 0; RSTB = 0; RSTC = 0; RSTD = 0; RSTM = 0; RSTP = 0; RSTOPMODE = 0; RSTCARRYIN = 0;
49        CEA = 1; CEB = 1; CEC = 1; CED = 1; CECARRYIN = 1; CEM = 1; CEP = 1; CEOPMODE = 1;
```

2.3 Path 1 check

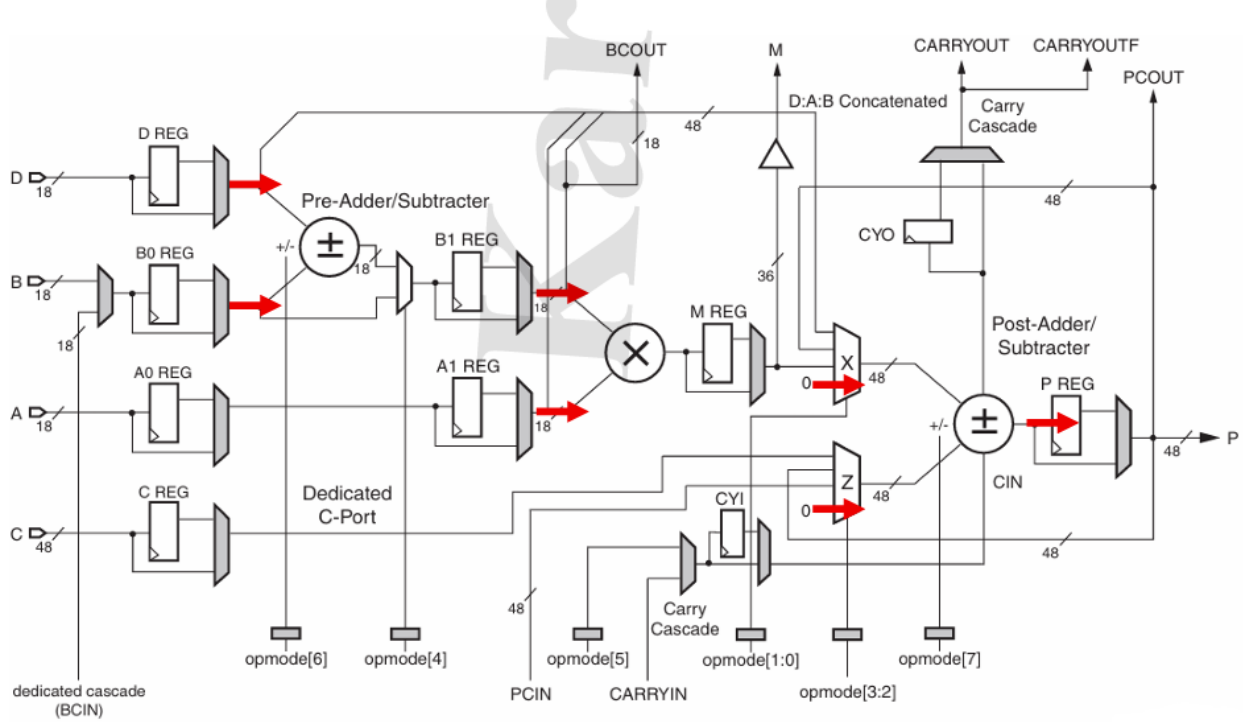


```

50
51 // path 1 test
52 A = 20; B = 10; C = 350; D = 25;
53 BCIN = $random(); CARRYIN = $random(); PCIN = $random(); OPMODE = 8'b1101_1101;
54
55 M_exp = 'h12c; P_exp = 'h32; PCOUT_exp = 'h32; BCOUT_exp = 'hf; CARRYOUT_exp = 0; CARRYOUTF_exp = 0;
56
57 repeat (4) @(negedge CLK);
58
59 if ((M == M_exp) && (P == P_exp) && (PCOUT == PCOUT_exp) && (BCOUT == BCOUT_exp) &&
60     (CARRYOUT == CARRYOUT_exp) && (CARRYOUTF == CARRYOUTF_exp))
61     $display("path 1 test passed");
62 else begin
63     $display("error in path 1");
64     $stop();
65 end
66

```

2.4 Path 2 check

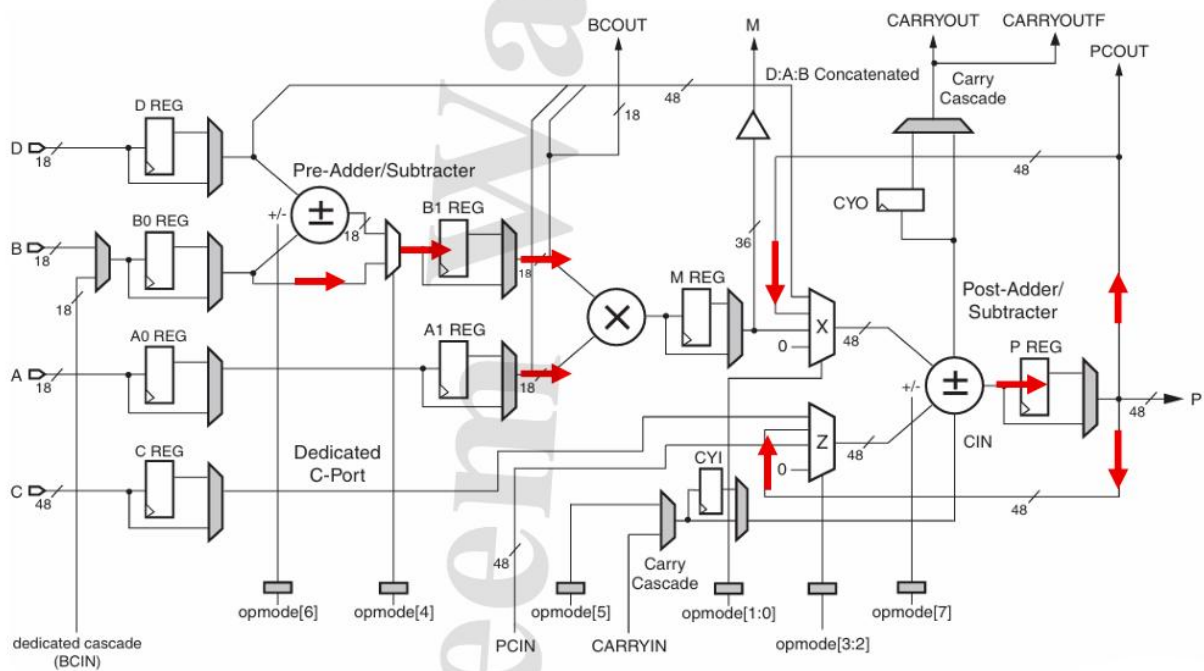


```

66
67 // path 2 test
68 A = 20; B = 10; C = 350; D = 25;
69 BCIN = $random(); CARRYIN = $random(); PCIN = $random(); OPMODE = 8'b0001_0000;
70
71 M_exp = 'h2bc; P_exp = 0; PCOUT_exp = 0; BCOUT_exp = 'h23; CARRYOUT_exp = 0; CARRYOUTF_exp = 0;
72
73 repeat (3) @(negedge CLK);
74
75 if ((M == M_exp) && (P == P_exp) && (PCOUT == PCOUT_exp) && (BCOUT == BCOUT_exp) &&
76     (CARRYOUT == CARRYOUT_exp) && (CARRYOUTF == CARRYOUTF_exp))
77     $display("path 2 test passed");
78 else begin
79     $display("error in path 2");
80     $stop();
81 end
82
83

```

2.5 Path 3 check

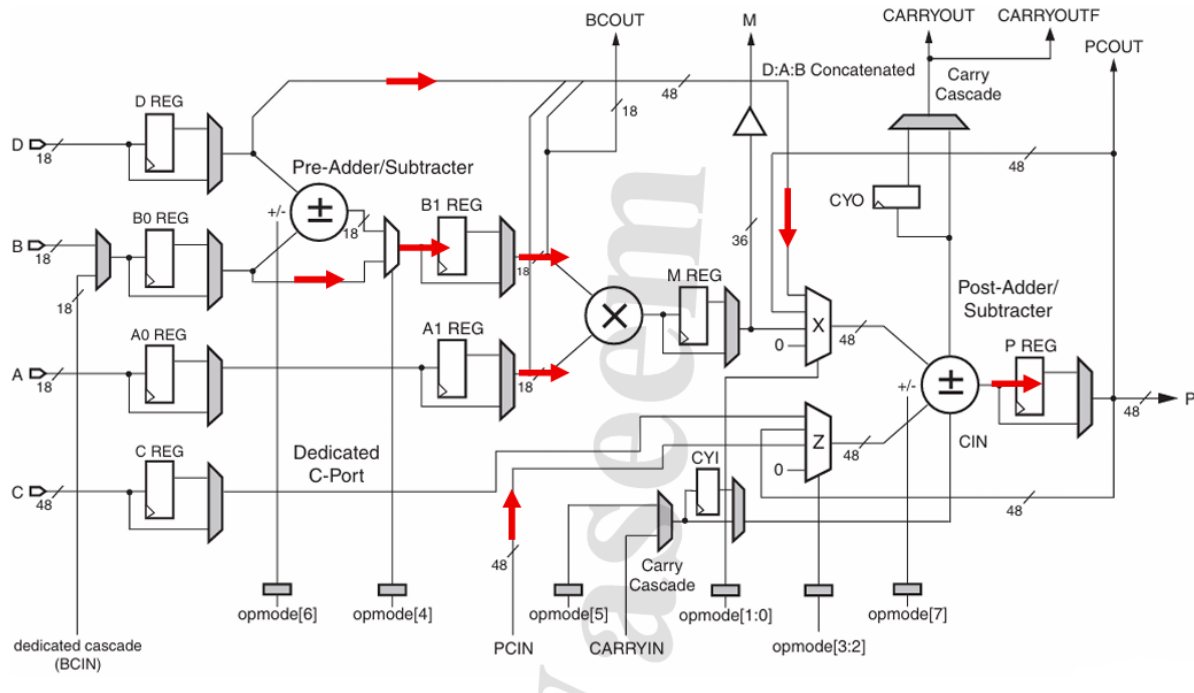


```

84 // path 3 test
85 A = 20; B = 10; C = 350; D = 25;
86 BCIN = $random(); CARRYIN = $random(); PCIN = $random(); OPMODE = 8'b0000_1010;
87
88 M_exp = 'hc8; P_exp = 0; PCOUT_exp = 0; BCOUT_exp = 'ha; CARRYOUT_exp = 0; CARRYOUTF_exp = 0;
89
90 repeat (3) @(negedge CLK);
91
92 if ((M == M_exp) && (P == P_exp) && (PCOUT == PCOUT_exp) && (BCOUT == BCOUT_exp) &&
93     (CARRYOUT == CARRYOUT_exp) && (CARRYOUTF == CARRYOUTF_exp))
94     $display("path 3 test passed");
95 else begin
96     $display("error in path 3");
97     $stop();
98 end
99

```

2.6 Path 4 check



```

100
101 // path 4 test
102 A = 5; B = 6; C = 350; D = 25;
103 BCIN = $random(); CARRYIN = $random(); PCIN = 3000; OPMODE = 8'b10100111;
104
105 M_exp = 'h1e; P_exp = 'hfe6fffec0bb1; PCOUT_exp = 'hfe6fffec0bb1;
106 BCOUT_exp = 'h6; CARRYOUT_exp = 1; CARRYOUTF_exp = 1;
107
108 repeat (3) @(negedge CLK);
109
110 if ((M == M_exp) && (P == P_exp) && (PCOUT == PCOUT_exp) && (BCOUT == BCOUT_exp) &&
111     (CARRYOUT == CARRYOUT_exp) && (CARRYOUTF == CARRYOUTF_exp))
112     $display("path 4 test passed");
113 else begin
114     $display("error in path 4");
115     $stop();
116 end
117
118 $display("TEST PASSED :");
119 $stop();
120
121 end
122
123 endmodule : DSP48A1_tb

```

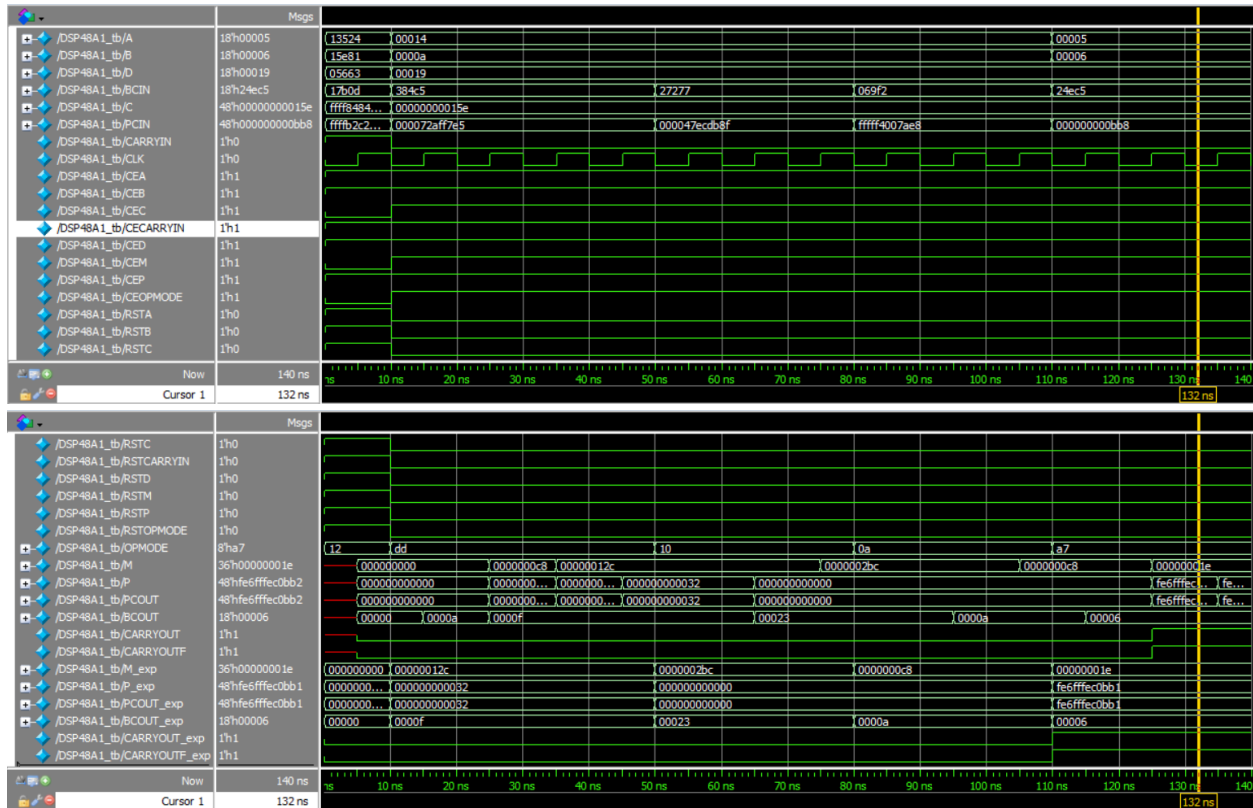
3 Do file

```

1 vlib work
2 vlog reg_mux_stage.v DSP48A1.v DSP48A1_tb.v
3 vsim -voptargs=+acc work.DSP48A1_tb
4 add wave *
5 run -all
6 #quit -sim

```


4 QuestaSim Waveform Snippets



5 Constrains file

```

6  ## Clock signal
7  set_property -dict { PACKAGE_PIN W5   IOSTANDARD LVCMOS33 } [get_ports CLK]
8  create_clock -add -name sys_clk_pin -period 10.00 -waveform {0 5} [get_ports CLK]
9
10
11
12
13
14
15
16  ## Configuration options, can be used for all designs
17  set_property CONFIG_VOLTAGE 1.8 [current_design]
18  set_property CFGBVS VCCO [current_design]
19
20  ## SPI configuration mode options for QSPI boot, can be used for all designs
21  set_property BITSTREAM.GENERAL.COMPRESS TRUE [current_design]
22  set_property BITSTREAM.CONFIG.CONFIGRATE 33 [current_design]
23  set_property CONFIG_MODE SPIx4 [current_design]


```





The remain is commented so it's unused.

I made the CONFIG_VOLTAGE 1.8 instead of 3.3 due to a warning in vivado.

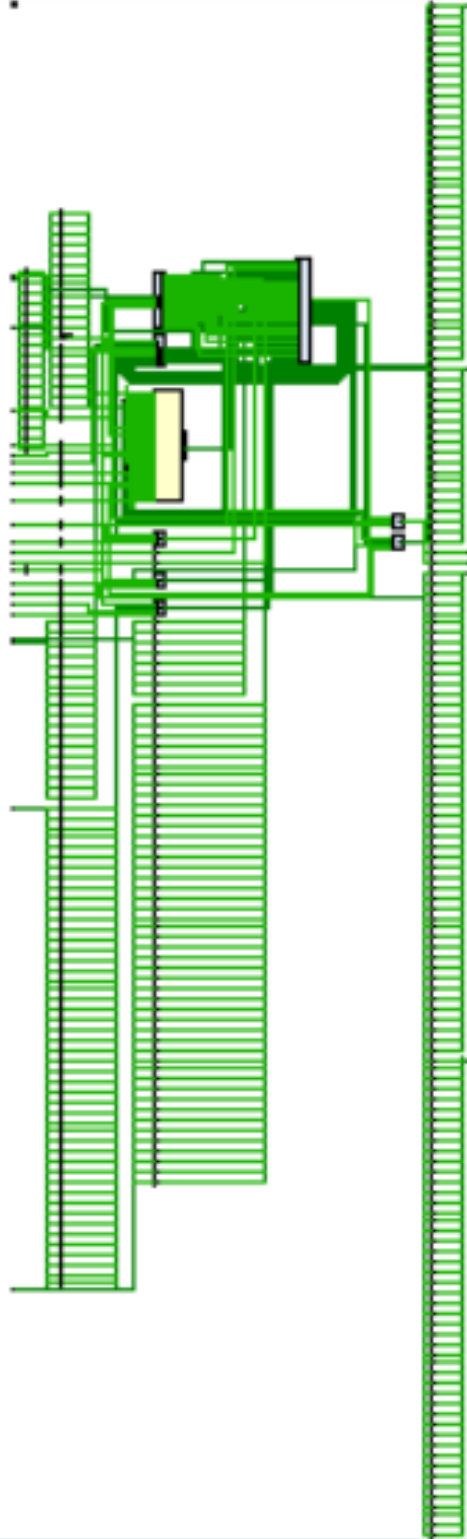
Tcl Console **Messages** x Log Reports Design Runs Debug ? _ □ □

☒ Warning (58)
 ☐ Info (59)
 ☐ Status (19)
 Show All

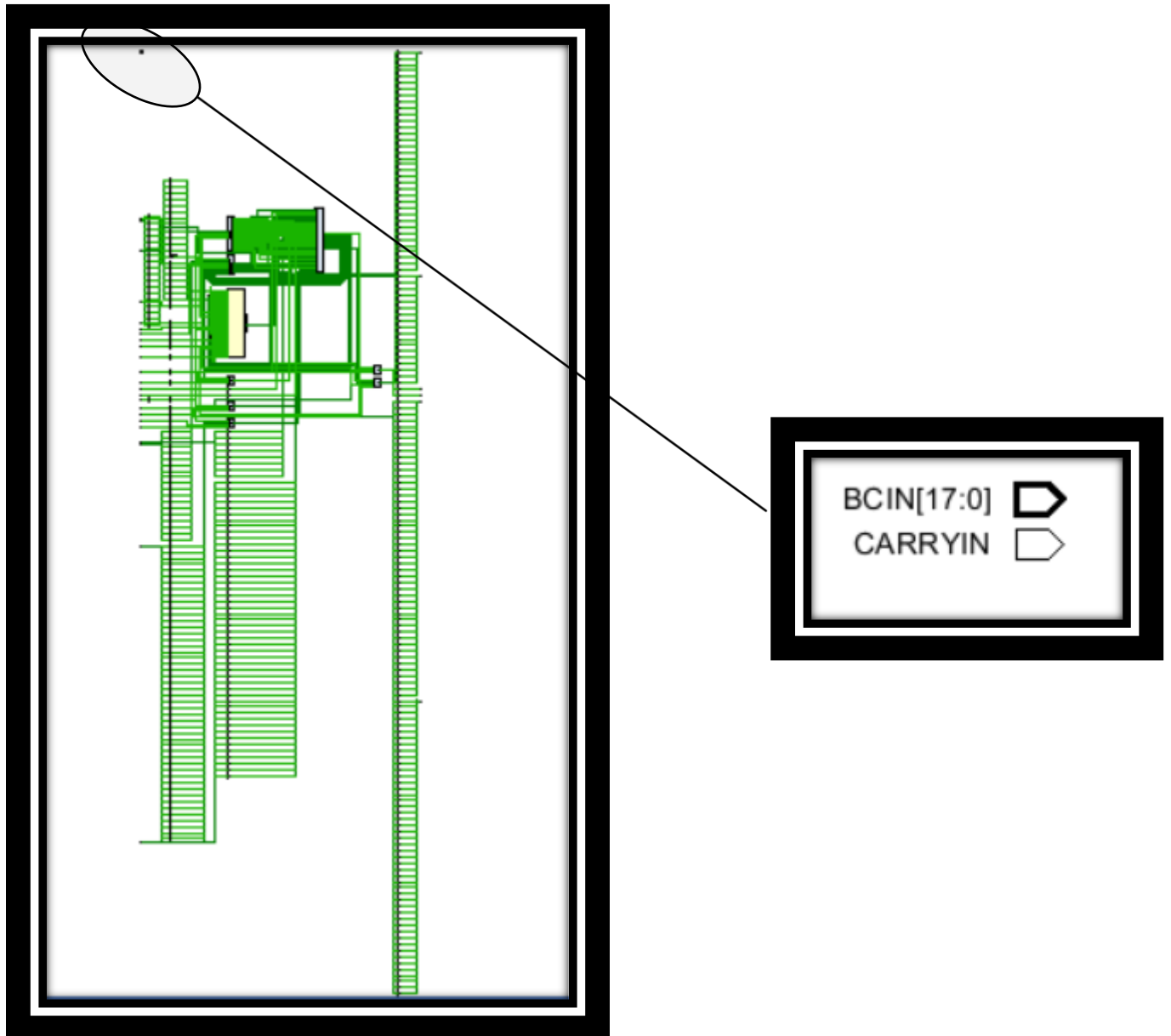
 **Synthesis** (58 warnings)

-  [Synth 8-2490] overwriting previous definition of module DSP48A1 [DSP48A1.v.1]
- >  [Synth 8-3331] design DSP48A1 has unconnected port CARRYIN (37 more like this)
- >  [Synth 8-3332] Sequential element (B0_SIG/data_reg[17]) is unused and will be removed from module DSP48A1. (17 more like this)
-  [Constraints 18-5210] No constraint will be written out.

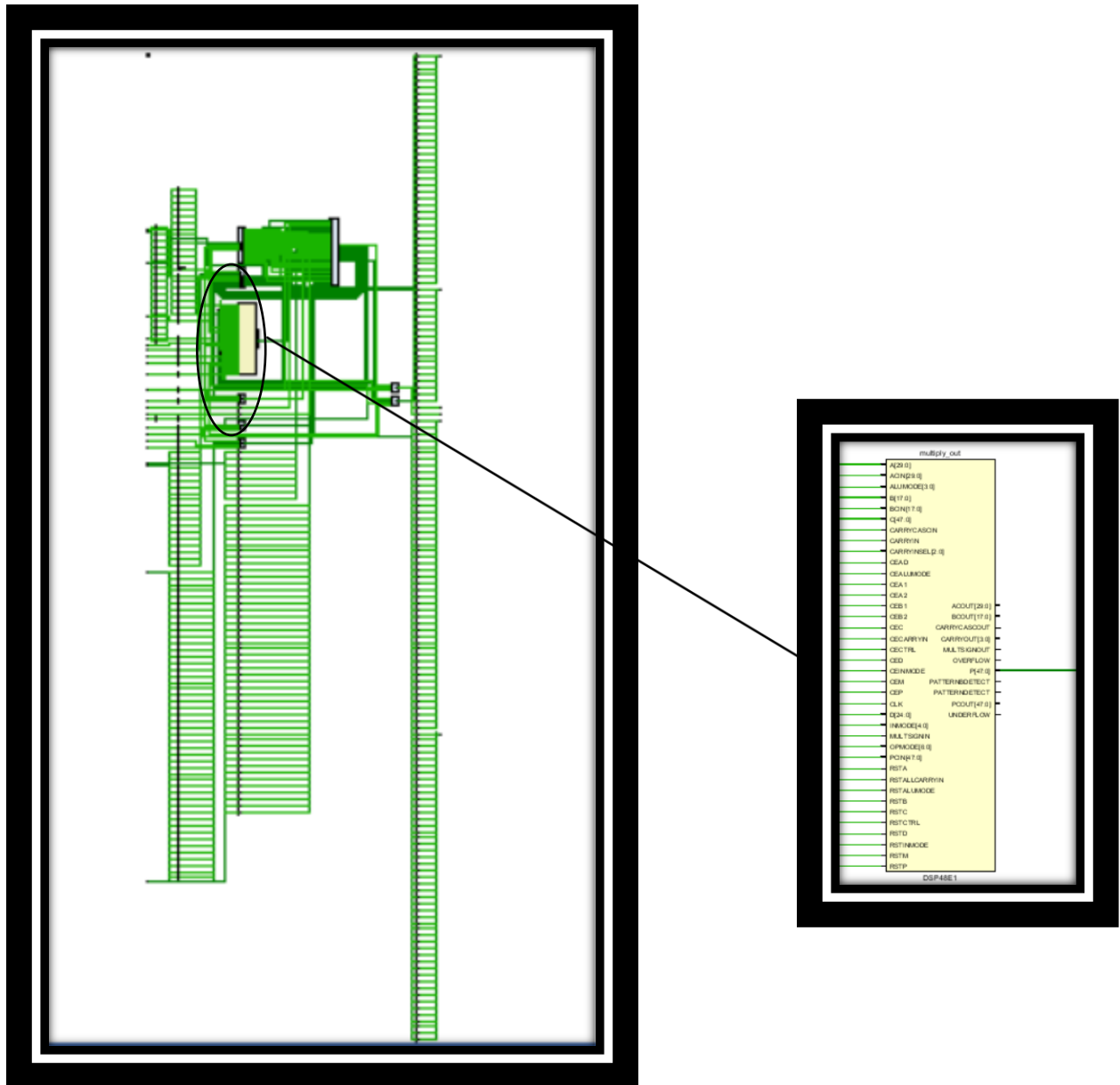
6.2.2 Schematic



Snippets



The unconnected inputs as the default design don't use them



The remains blocks are the registers for the signals in the design.

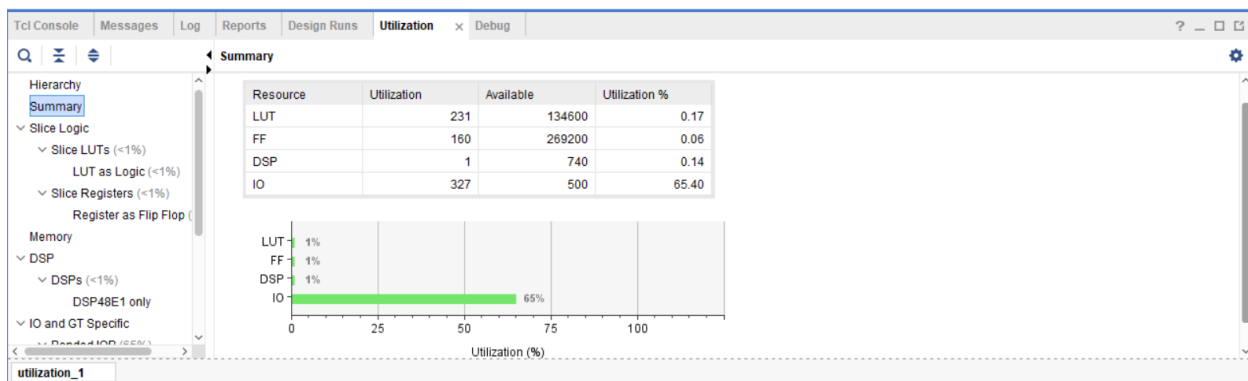
6.2.3 Utilization Report

Tcl Console Messages Log Reports Design Runs Utilization x Debug ? _ □ □

Hierarchy

utilization_1

Name	Slice LUTs (134600)	Slice Registers (269200)	DSPs (740)	Bonded IOB (500)	BUFGCTRL (32)
DSP48A1	231	160	1	327	1
A1_SIG (reg_mux_sta...	0	18	0	0	0
B1_SIG (reg_mux_sta...	0	18	0	0	0
C_SIG (reg_mux_stag...	0	48	0	0	0
CYI_SIG (reg_mux_sta...	1	1	0	0	0
CYO_SIG (reg_mux_st...	0	1	0	0	0
D_SIG (reg_mux_stag...	0	18	0	0	0
OPMODE_SIG (reg_m...	229	8	0	0	0
P_SIG (reg_mux_stag...	0	48	0	0	0



6.2.4 Timing Report

Tcl Console Messages Log Reports Design Runs Timing x Utilization Debug ? _ □ □

Design Timing Summary

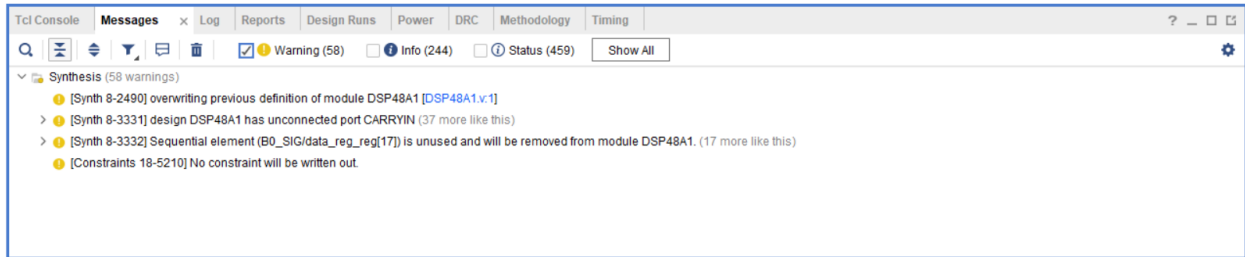
Timing Summary - timing_1

Setup	Hold	Pulse Width
Worst Negative Slack (WNS): 5.925 ns	Worst Hold Slack (WHS): 0.182 ns	Worst Pulse Width Slack (WPWS): 4.500 ns
Total Negative Slack (TNS): 0.000 ns	Total Hold Slack (THS): 0.000 ns	Total Pulse Width Negative Slack (TPWS): 0.000 ns
Number of Failing Endpoints: 0	Number of Failing Endpoints: 0	Number of Failing Endpoints: 0
Total Number of Endpoints: 87	Total Number of Endpoints: 87	Total Number of Endpoints: 162

All user specified timing constraints are met.

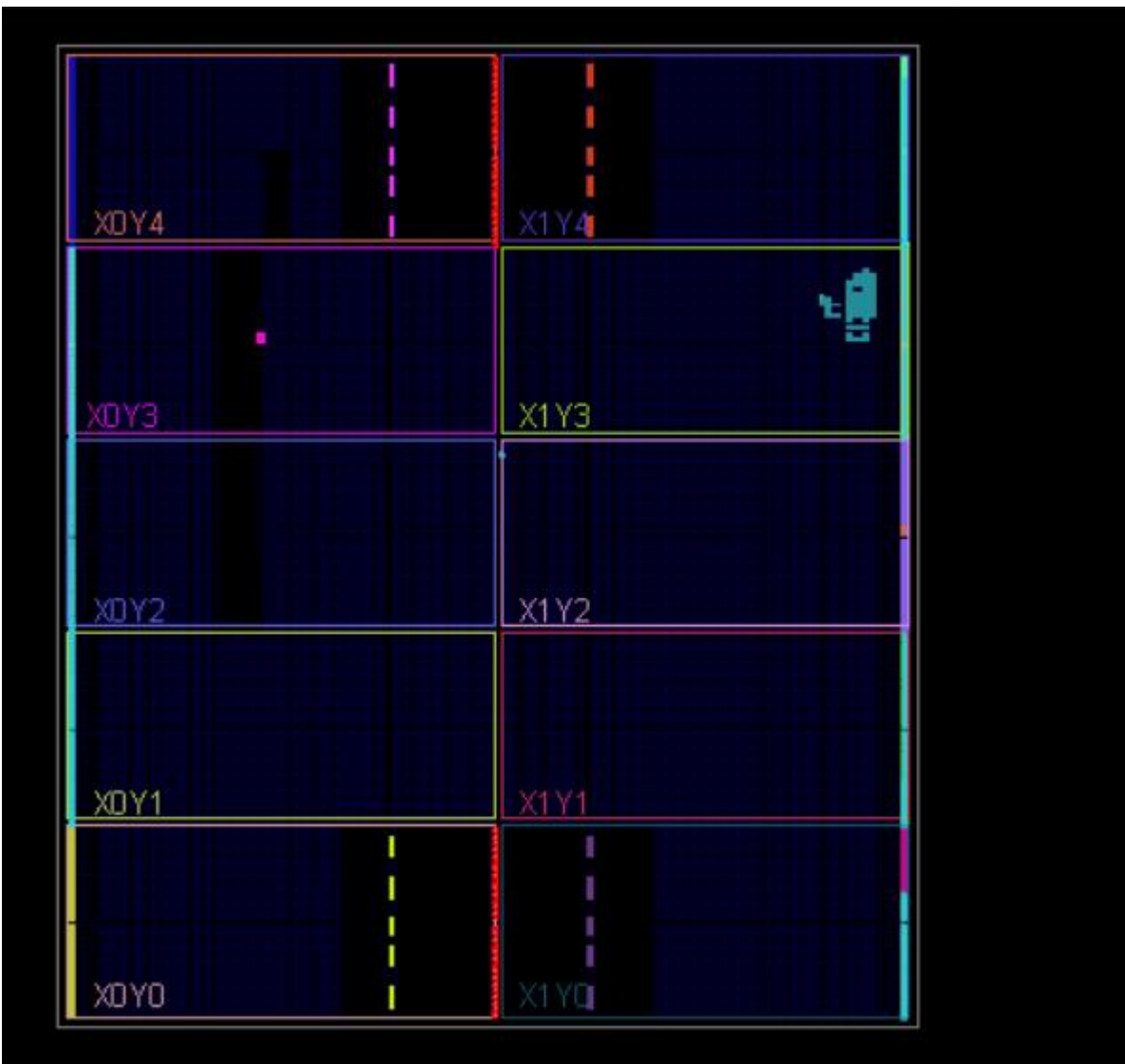
6.3 Implementation

6.3.1 Message tab

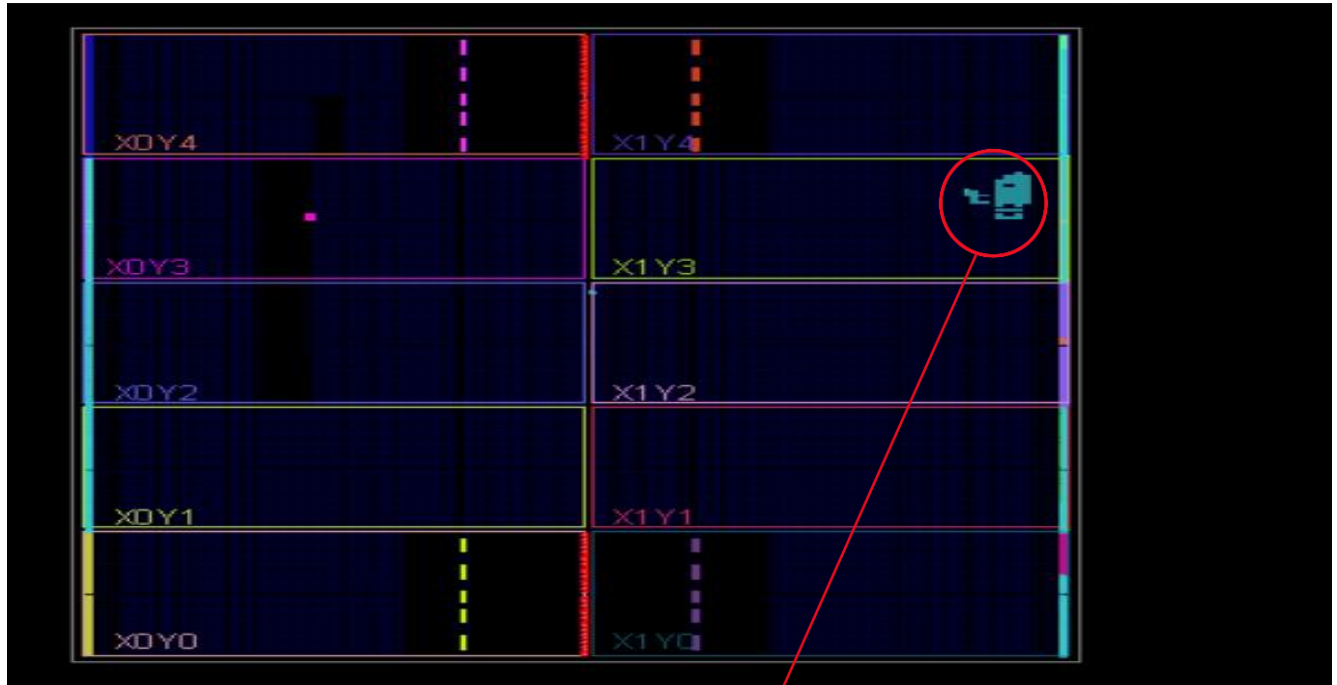


Nothing added.

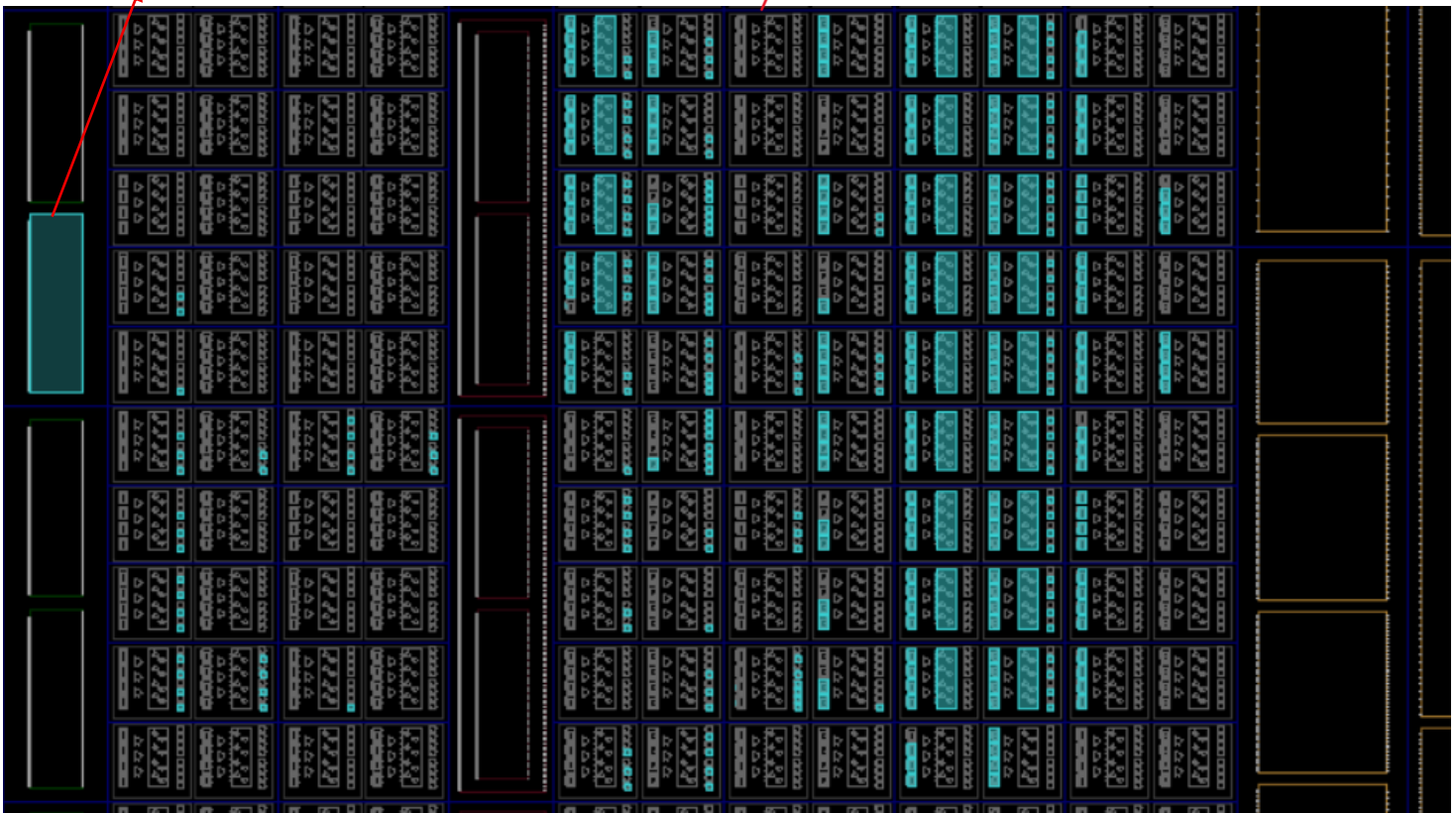
6.3.2 Device



Snippets

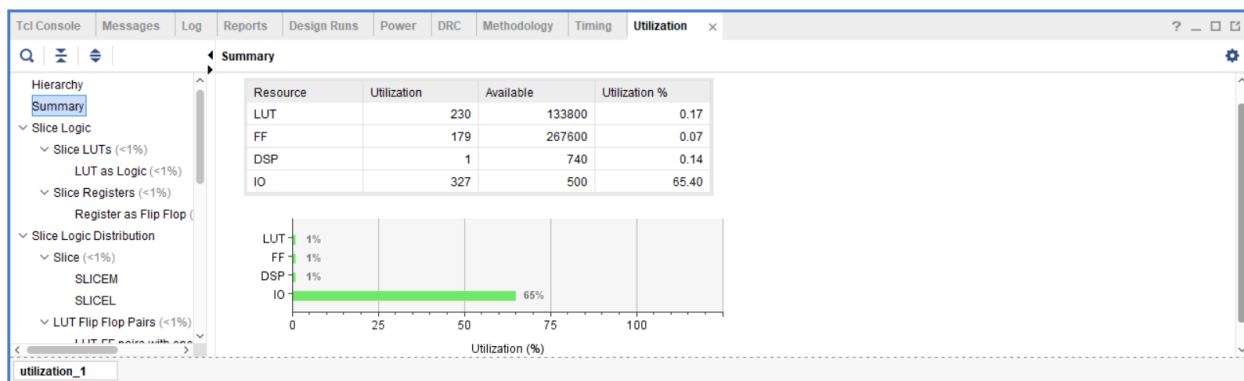


This is the DSP block
used inside FPGA



6.3.3 Utilization Report

Tcl Console Messages Log Reports Design Runs Power DRC Methodology Timing Utilization x ? _ □ ▢										
Hierarchy										
Name	Slice LUTs (133800)	Slice Registers (267600)	Slice (33450)	LUT as Logic (133800)	LUT Flip Flop Pairs (133800)	DSP s (740)	Bonded IOB (500)	BUFGCTRL (32)		
▼ DSP48A1	230	179	99	230	50	1	327	1		
A1_SIG (reg_mux_sta...	0	18	6	0	0	0	0	0		
B1_SIG (reg_mux_sta...	0	36	10	0	0	0	0	0		
C_SIG (reg_mux_stag...	0	48	15	0	0	0	0	0		
CYI_SIG (reg_mux_sta...	1	1	1	1	1	0	0	0		
CYO_SIG (reg_mux_st...	0	2	2	0	0	0	0	0		
D_SIG (reg_mux_stag...	0	18	11	0	0	0	0	0		
OPMODE_SIG (reg_m...	229	8	74	229	0	0	0	0		
P_SIG (reg_mux_stag...	0	48	12	0	0	0	0	0		



6.3.4 Timing Report

Tcl Console Messages Log Reports Design Runs Power DRC Methodology Timing x Utilization ? _ □ ▢										
Design Timing Summary										
General Information										
Timer Settings										
Design Timing Summary										
Clock Summary (1)										
Check Timing (326)										
Intra-Clock Paths										
Inter-Clock Paths										
Other Path Groups										
User Ignored Paths										
Unconstrained Paths										
Setup										
Hold										
Pulse Width										
Worst Negative Slack (WNS): 4.813 ns										
Worst Hold Slack (WHS): 0.261 ns										
Worst Pulse Width Slack (WPWS): 4.500 ns										
Total Negative Slack (TNS): 0.000 ns										
Total Hold Slack (THS): 0.000 ns										
Total Pulse Width Negative Slack (TPWS): 0.000 ns										
Number of Failing Endpoints: 0										
Number of Failing Endpoints: 0										
Number of Failing Endpoints: 0										
Total Number of Endpoints: 106										
Total Number of Endpoints: 106										
Total Number of Endpoints: 181										
All user specified timing constraints are met.										

7 Linting

The screenshot shows two windows from a software interface. The top window is titled "Lint Checks" and has a yellow header bar. It contains a filter bar with a search field "Filter: Type here" and several status buttons: Waived, Fixed, Pending, Uninspected, Bug, Verified. To the right of these buttons, it says "Total : 0 Selected : 0". Below the filter bar is a table with columns: Severity, Status, Check, Alias, Message, Module, Category, State, Owner, and STARC Reference. The table is currently empty. At the bottom of the window is a tab bar with tabs: Transcript, Message Viewer, Lint Checks (which is active), Design Metrics, Design Information, Status History, and Lint Dashboard.

The bottom window is titled "Lint Summary" and has a search field with the placeholder text "(Type Search Text (Press Enter))". Below the search field is a table with two columns: Name and Count. The table contains the following data:

Name	Count
Open(uninspected, pendi...	11 (15)
Warning	5
Info	6 (10)

These warnings have shown as there is a fixed expressions in the muxes in my design but I can ignore these warnings as I intend to do this.