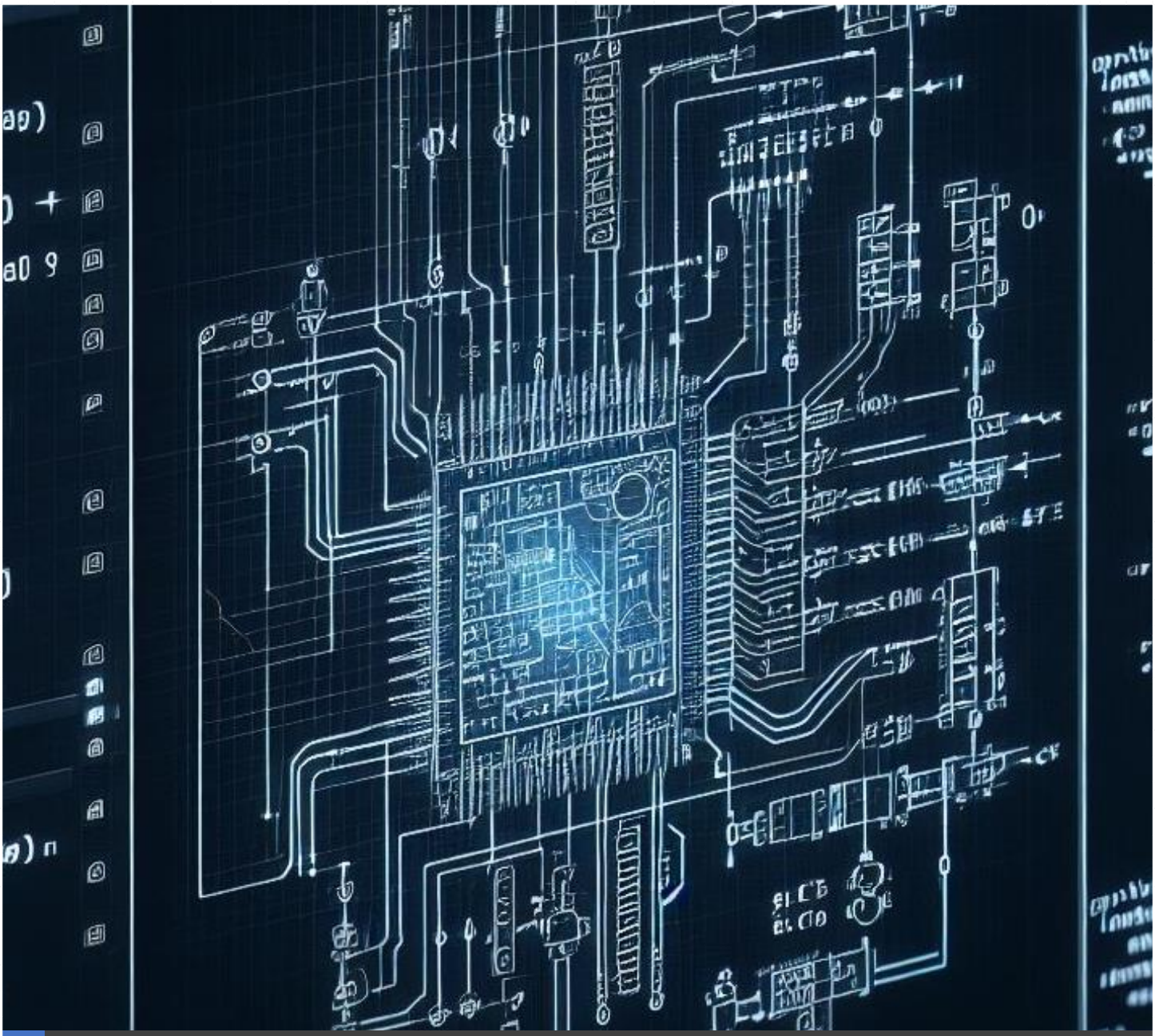

QuestaSim/ModelSim Tutorial

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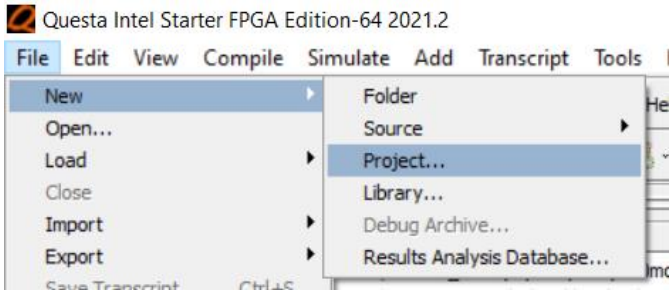
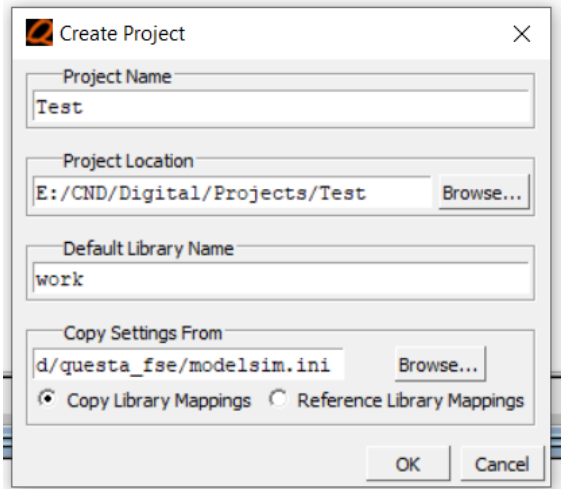
Contents

1. Creating a new project (or opening an existing one):

From "**File → New → Project**" to create a project. (or "**File → Open…**" and select existing project)

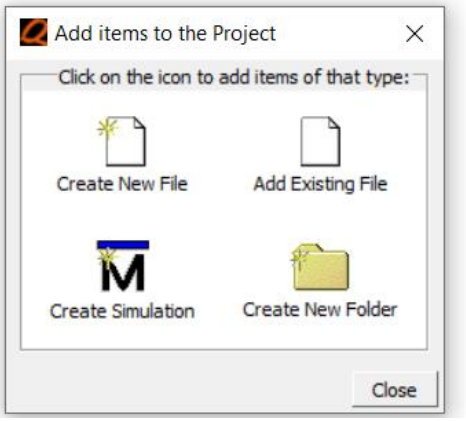


A small window will open. Enter the name for the project and create a folder for it and select it in the project location.

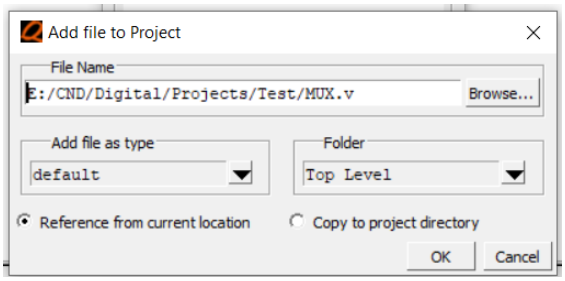


2. Adding Verilog Files:

- For new projects, a small window will open.

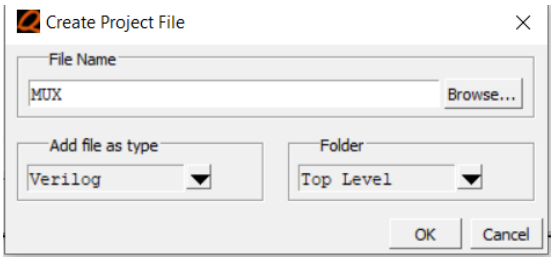


You can **add an existing Verilog file**, if you have one, and you will have two options:

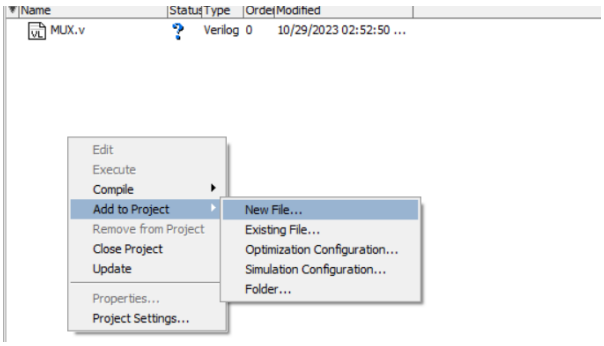


- **Reference from current location**: it will access the file at the location specified without copying the file to the project location. Useful for using the same file with different software (e.g., Quartus).
- **Copy to project directory**: it will make a copy of the file to the project location. The original file will not be affected by any editing to the new file.

Or, you can **create a new file**. Type a name for the file (N.B. if this file contains the top-level module, its name must match the module name) and choose the **file type** to be "**Verilog**".

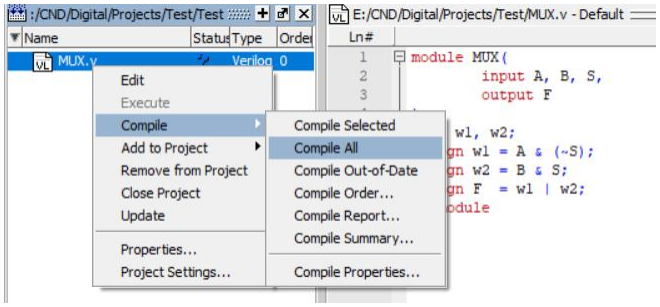


- If you, already, have a project you can add a file by right clicking the project window space and choose "**Add to project**". This also can be done from the "**Project**" menu.

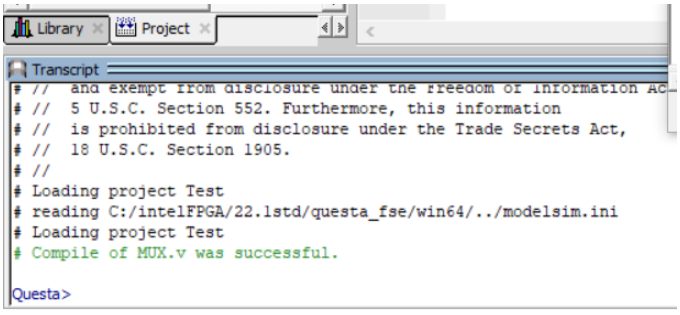


3. Compiling the Design and Checking Errors:

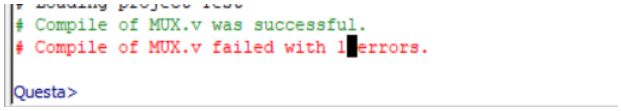
After writing the codes, right click and choose "**Compile**".



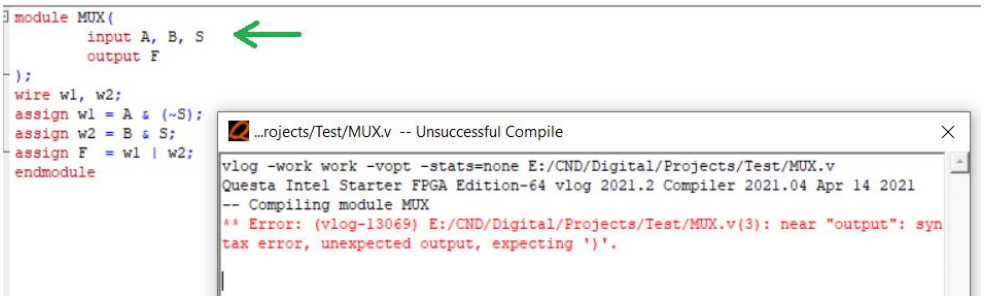
If there are no errors the "**Transcript**" window will output successful with a green font.



If there are errors the "**Transcript**" window will output failed with number of errors with a red font.

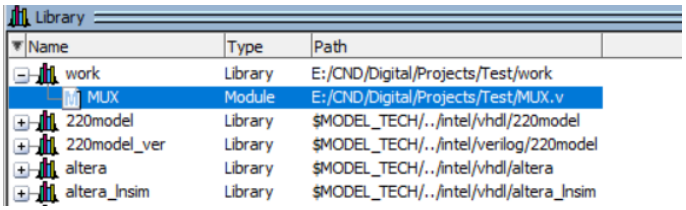


Clicking that line will show a window listing the errors. For example, forgetting the ',' between signals declarations:

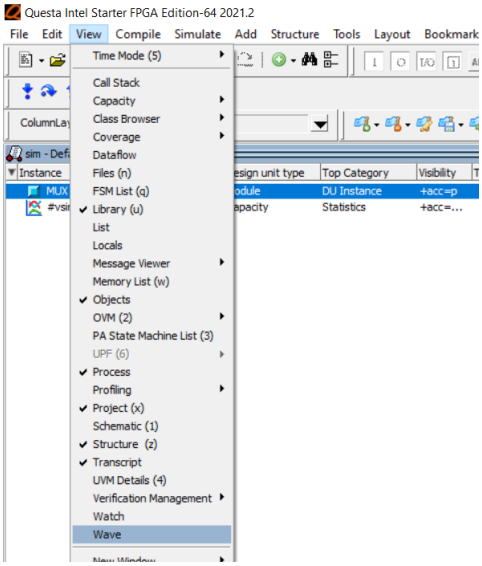


4. Simulating the Compiled Design:

From the "**Library**" window, under "**Work**" library, you will find the compiled modules. Double click the top module (e.g., MUX) to enter the simulation mode.

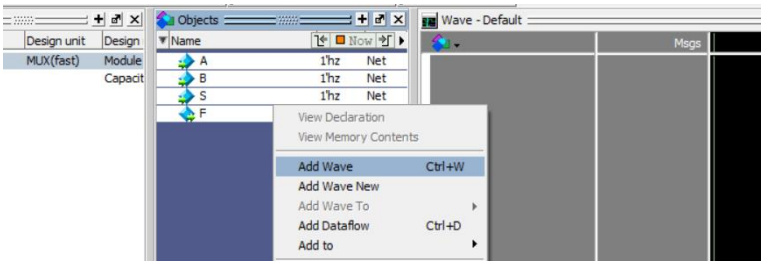


A wave window should open among other sub-windows. If it didn't show up, from "**View → Wave**"

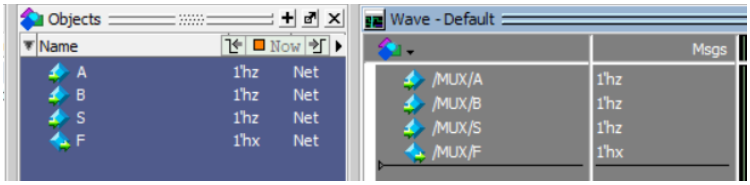


5. Simulation Waveform Creation:

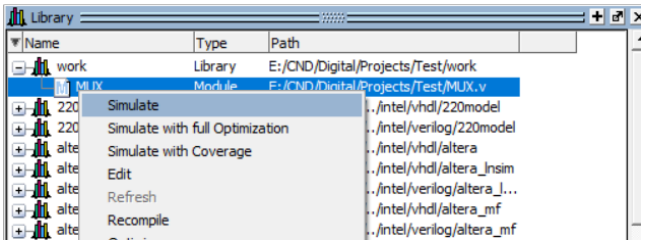
From "**Objects**" window, select the required nets to observe ("**Ctrl** + **A**" to select all) and choose "**Add Wave**".



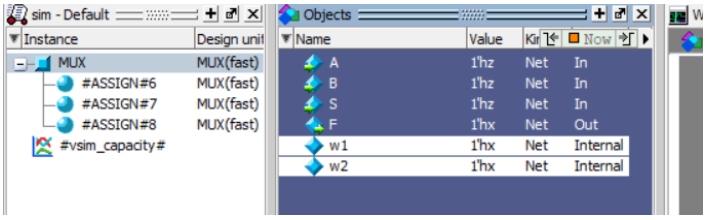
They will show up in the "**Wave**" window.



As you may have noticed, only I/Os are shown in the "**Objects**" window; no inner nets are observed. To be able to observe the inner nets values, when you want to simulate the module, right click and choose "**Simulate**" instead of double clicking.

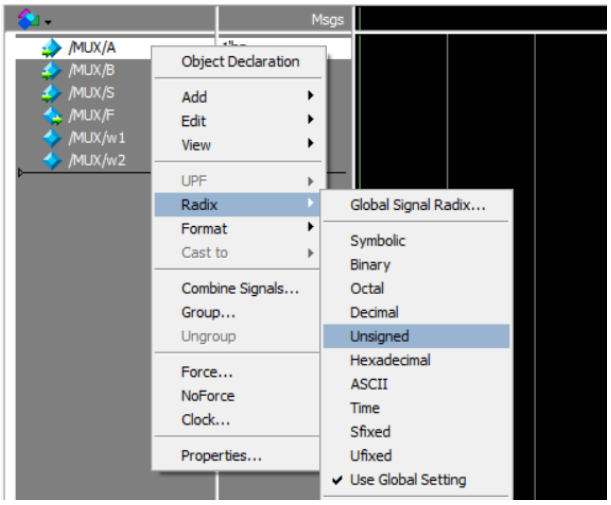


This will make any declared net in the design.

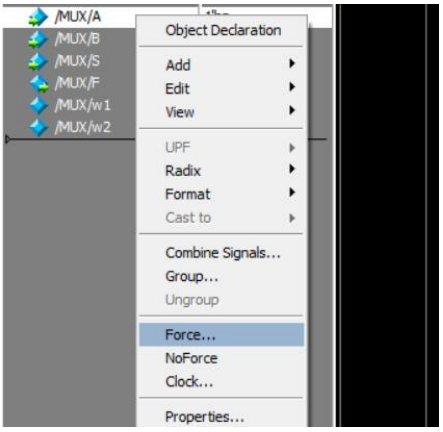


6. Adding Values to the Design Nets:

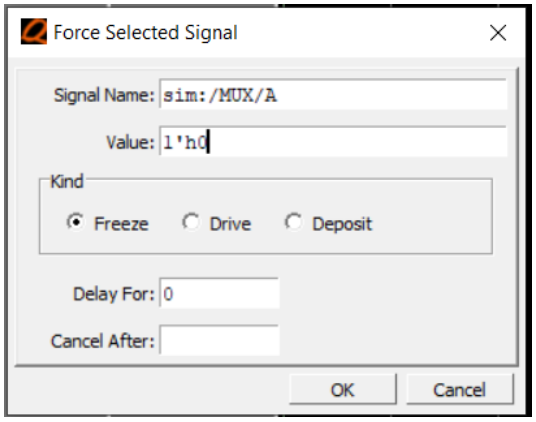
You can change the nets values **radix** for better understanding of them.



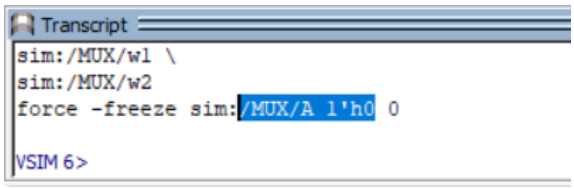
- To add a constant value for an input, choose "**Force**".



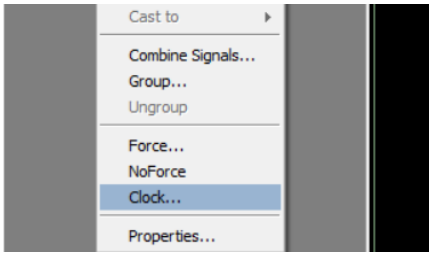
A window will open and you can add the value you want.



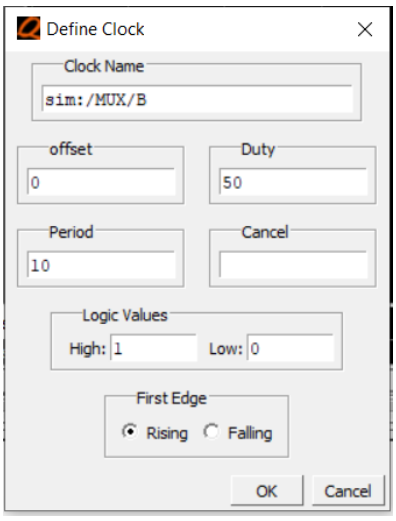
You can also add it from the "**Transcript**" window by typing the command for "**Force**".



- To add an alternating value (Clock), choose "**Clock**" instead of "**Force**". You can also use the force command.



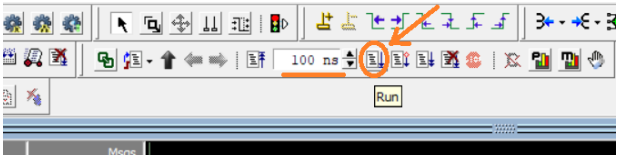
A window will open and you can add the values you want for the **period**, **high**, and **low** logic.



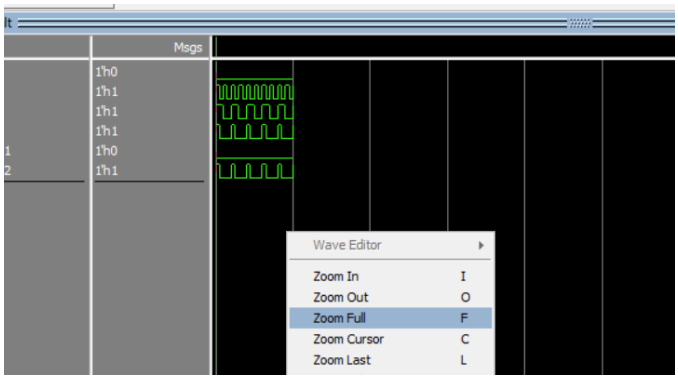
N.B.: Although you can force any net in the design (inner or outputs), it is required to force only the inputs. Forcing other nets (other than the inputs) will override the values calculated by the circuit. This is only helpful for inout signals, or for debugging – if a net calculated value is wrong you can force it to check the validity of the remaining nets.

7. Observing the Waveform:

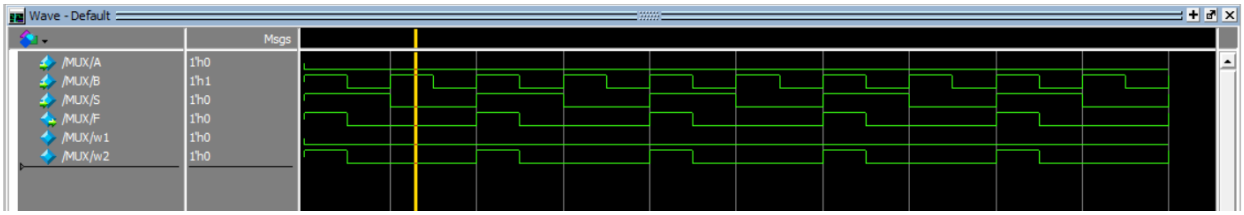
After adding values to inputs, click the "**Run**" button in the toolbar after specifying the simulation time.



The waveform will show up. To make it take the whole window, right click in the wave window and choose "**Zoom Full**" or simply press the "**F**" key on the keyboard.



The waveform will expand and you can trace the values with cursor after clicking in the wave.

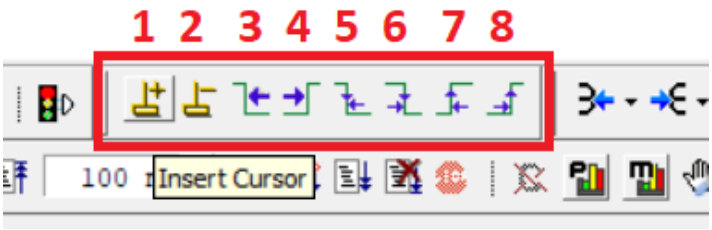


There are various useful tools to help inspect the waveform. These tools are as the following:

1) **Insert Cursor.**
2) **Remove Cursor.**

After selecting a net to inspect:

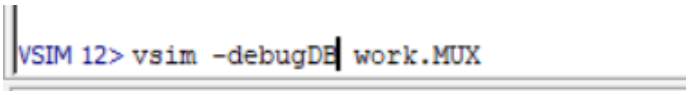
3) **Find Previous Transition.**
4) **Find Next Transition.**
5) **Find Previous Falling Edge.**
6) **Find Next Falling Edge.**
7) **Find Previous Rising Edge.**
8) **Find Next Rising Edge.**



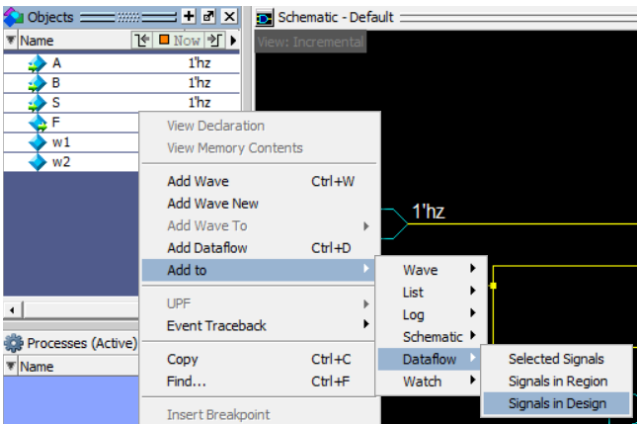
8. Schematic of the Design:

To be able to view the schematic, you have to simulate in debug mode. Simply, in the "**Transcript**" window, type:

"**vsim -debugDB work.**{Module Name}"



And from the "**View**" menu open the "**Schematic**" window. If the "**Schematic**" window is empty, right click in the "**Objects**" window and select "**Add to → Dataflow → Signals in Design**".



The design schematic should show up now.