To account for the offsets in memory for red, green, even blues, and odd blues, we created four new parameters and set them to the memory location given to us in the document. Then, for the data that is being fetched from the SRAM_address, we made sure to add the offset to the address to ensure the requirements were met for the memory. A red buffer was also included to account for the new data being stored as it occurred within 2 clock cycles of the following output. If we ignore this issue, then an extra red line would show up in the previous box. To account for whether the blue values are the even or odd bits, we used the ? operator to check whether the least significant bit of data_counter was 0, if so, the even bits are used. Else, the odd bits are used.

The compilation report says that the main file has 174 registers which does match the registers we counted. This was counted by analyzing which registers were used in the always_ff block in the main file. When looking at the timing analysis conducted, the critical path for this system is from state_bit_0 to SRAM_write_data[7] with a time delay of 8.198ns.

Module (Instance)	Register name	Bits	Description
Top – level experiment 1	SRAM_address	18	Address register used for accessing the external memory
Top - level experiment 1	data_counter	18	This is the counter used to increment the colour address with the SRAM address
define_state	GREEN_START_ADDRESS	18	This is where the G segment of the SRAM starts.
define_state	BLUE_EVEN_START_ADDRESS	18	This is where the even B segment of the SRAM starts.
define_state	BLUE_ODD_START_ADDRESS	18	This is where the odd B segment of the SRAM starts.
Top - level experiment 1	VGA_sram_data[0]	16	Buffer register - holds the red data for the pixels before it is ready to be transferred to the VGA controller
Top - level experiment 1	VGA_sram_data[1]	16	Buffer register - holds the green data for the pixels before it is ready to be transferred to the VGA controller
Top - level experiment 1	VGA_sram_data[2]	16	Buffer register - holds the blue data for the pixels before it is ready to be transferred to the VGA controller

VGA_controller	VGA_red	8	Outputs red pixels
VGA_controller	VGA_green	8	Outputs green pixels
VGA_controller	VGA_blue	8	Outputs blue pixels
Top - level experiment 1	Red_buf	8	Register that stores the previous value of the second red value before it is overwritten
Top - level experiment 1	state	4	The state register which is used by finite state machine which organizes the transfer of data going to and from the external SRAM and to the VGA controller