A diagram of a circuit

Description automatically generated

There is 2 ICs to control the four 7-segment LEDs, both are 74HC573 latch (U19) and (U20).

1. The 74HC573 latch

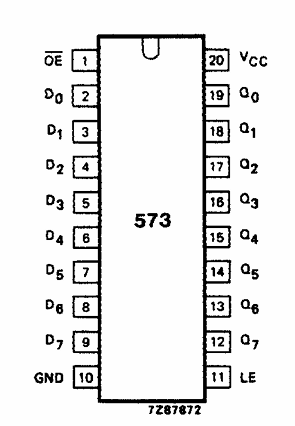
**Reminder:**

The 74HC573 is an octal D-type latch with 3-state outputs, meaning it has 8 D-type latches that can temporarily store data and pass it to the outputs when needed

* D-flipflop is edge-triggered, meaning that it’s require clock signal to pass the input data to output pin when triggered.
* D-type latch is level triggered, meaning that it uses enable signal (instead of clock signal) to lock a input data to output pin when enabled. After the desired data is locked, the enable pin goes Low to preserve the desired data at the output.

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**There are only 2 enable/control signals:**

**+ LE: Active HIGH latch signal**

**+ OE: Active LOW buffer enable signal**

When “LE” is HIGH, the latch is transparent meaning that the data at D0 to D7​ flows directly to the internal latches and is updated continuously.

When the “LE” goes to LOW, the latch stop updating new input, effectively locking the previous input to output Q pins

The output Qs of latche are passed through a tri-state buffer controlled by the OE signal, which decided whether the output Qs of latch appear at the output Q0 to Q7 pins of the IC or not.

When the OE signal is disable (HIGH), the output pins will be High-Impedance (High-Z), i.e typical output of the buffers when not enabled.

**The OE pins of both latch on the experiment kit are hardware to GND to be always ACTIVE**

1. U19

The U19 latch passes the segment signals A, B ,C ,D, E, F, G, DP of the 7-segment LEDs, which are shared by all four 7-segment LEDs.

This latch uses the nLE0 signal to update contents

**The 7-segment LEDs are Common Anode display, meaning that all the segments signal have to common 5V pins, you must output logic low to the corresponding segment pins to complete the circuit and Lit the LED on and logic high to turn them off (no voitage difference).**

1. U20

Since the 7-segment LEDs are Common Anode, this latch passes 4 signals the these common Anode pin for the power supply of the LEDs, which effectively selecting the LEDs we want to display

This latch uses the nLE1 signal to update contents, make sure only 1 output is HIGH at a time (one-hot signal), to control individual LED.

The output signal are (LEDs from left to right):

These outputs pins used to control the BJTs to allow 5V source to the Common Anode pins of the 7-segments LEDs