DESIGN AND IMPLEMENTATION OF FPGA BASED 32-BIT WALLACE AND SYSTOLIC MULTIPLIERS

[1]P. Vamsi Krishna, [2]K.Nirosha, [3]G.Amala, [4]N.Manikanta, [5]J. Venkata Suman

[1,2,3,4]UG Students, [5]Assistant Professor
Department of ECE, GMR Institute of Technology, Rajam.

Abstract: **Now a days in VLSI technology size, power, speed and cost are the main design considerations in any circuits. As the number of added operations in normal multipliers are more which results in increase in delay. Therefore the circuits designed with normal multipliers will consume more power and possess less speed. Multipliers play a vital role in digital signal processing applications. In this paper, design and implementation of FPGA based 32 bit Wallace multiplier and Systolic multiplier has been done. These multipliers were designed using Verilog HDL, simulation and synthesis is done in both RTL compiler using Xilinx Vivado and implemented on Zynq 7000 series FPGA board.**

Keywords: **Systolic Multiplier, Wallace Multiplier, Verilog HDL, FPGA, Digital Signal Processing**

I. INTRODUCTION

Performance is recognized as one of the critical parameter in digital system design field, especially in digital signal processing (DSP) applications. Multipliers play an essential role in digital processing systems and various other applications such as Multiply Accumulate (MAC) unit, ALU, FIR filters, Microprocessors, Digital Signal Processors, etc., Moreover, high speed multipliers are the key to improve overall efficiency of the digital system. Generally multiplier is the slowest element in the system and requires more area, less power and long latency. Therefore multiplier design has been an important part in efficient VLSI system design. Multiplication is an important fundamental function in arithmetic logic operation. Hardware computational performance of a DSP system is limited by its multiplication performance and since, multiplication dominates the execution time of most DSP algorithms therefore area efficient, high speed and low power multiplier is much desired [1-4].

With advances in VLSI technology, many researchers have tried and are trying to design various multipliers which offer either of the following design targets high speed, low power consumption, regularity of layout and hence less area as combination of them in one multiplier thus making them suitable for compact VLSI implementation.

An efficient multiplier should have following characteristics:
Speed: Multiplier should perform operation at high speed.
Area: A multiplier should occupy less number of slices and LUTs.
Power: Multiplier should consume less power.

II. LITERATURE SURVEY

M. Aravind Kumar, O.Ranga Rao proposed a paper "Performance Evaluation of Different Multipliers in VLSI using VHDL" in which the performance analysis is done for different multipliers such as array multiplier, Vedic multiplier and booth multiplier. The FPGA implementation is done and performance characteristics such as area, power and delay are done. Finally, these are compared and performance characteristics are analysed [5].

K. B. Jagannatha, H. S. Lakshmisagar and G. R. Bhaskar proposed a paper "FPGA and ASIC implementation of 16-bit Vedic multiplier using Urdhva triyakbhyam sutra" in which the design of Multiply Accumulate Unit (MAC) using Vedic Multiplier is the Ancient Indian Vedic Mathematics technique that has been modified as per technology for improving the performance of mathematical computations. The ASIC implementation is done and the performance characteristics are analysed [6].

In this paper, design and FPGA implementation of 32 bit Wallace and Systolic multipliers have been done. Higher order bit multipliers were designed using lower order bit multipliers. These 32 bit multipliers were designed using Verilog code, simulation and synthesis is done in both RTL compiler using Xilinx Vivado and implemented on Zynq 7000 series FPGA board.

III. MULTIPLIERS

a) WALLACE TREE MULTIPLIER:

Wallace tree reduces the number of partial products to be added into two final intermediate results. The Wallace tree basically multiplies two unsigned integers. A Wallace tree is an efficient hardware implementation of a digital circuit that multiplies two integers, devised by an Australian Computer Scientist Chris in 1964.

The Wallace tree has three steps such as partial product generation stage, partial product reduction stage and partial product addition stage.

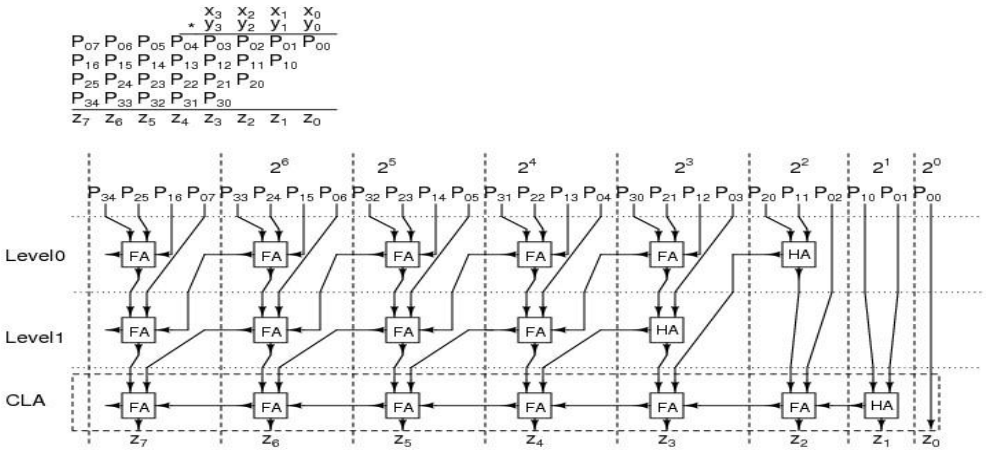

Figure 1: Wallace tree multiplier

Wallace tree multiplier has quite a few considerable advantages over the other multiplier designs which typically include high power, faster computation with less delay.

b) SYSTOLIC MULTIPLIER:

A Systolic array is a homogenous network which consists of cells or nodes. Every node it stores a partial result obtained from the received data of upstream and it is passed to the downstream. The Systolic arrays were invented by Richard P. Brent and H. T. Kung, and further they have developed them into greatest common divisors of polynomials as well as integers. These Systolic arrays were classified into four categories likewise single instruction single data(SISD), single instruction Multiple data (SIMD), Multiple instruction single data (MISD), Multiple instruction Multiple data (SIMD).

This Systolic array consists of rows and columns of data processing units called nodes. After processing each node shares the information with other nodes. The data flowing in the array among different data processing units flows in different directions.

A Systolic array can be used for matrix multiplication. A single matrix is sent in a queue from top array to down array, the other matrix given in a column is sent from left to right. There after some garbage values are sent until each unit has seen one complete row and one complete column. Finally the result is stored in the array.

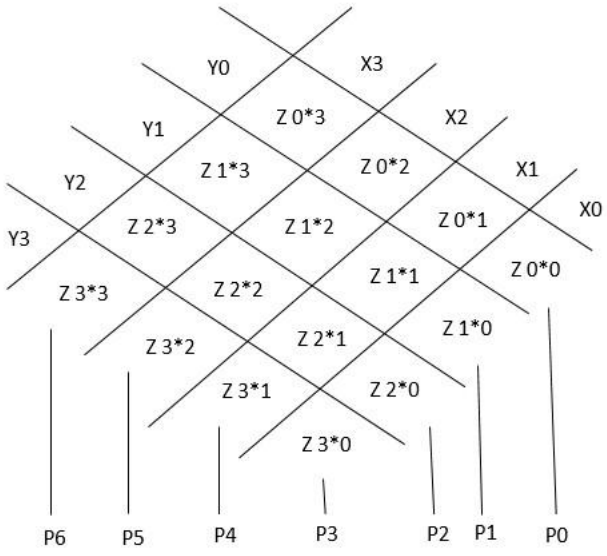

Figure 2 4 X 4 Systolic Multiplication

IV. DESIGN OF PROPOSED MULTIPLIERS

a) Implementation of 8-bit multiplier using 4-bit multiplier:

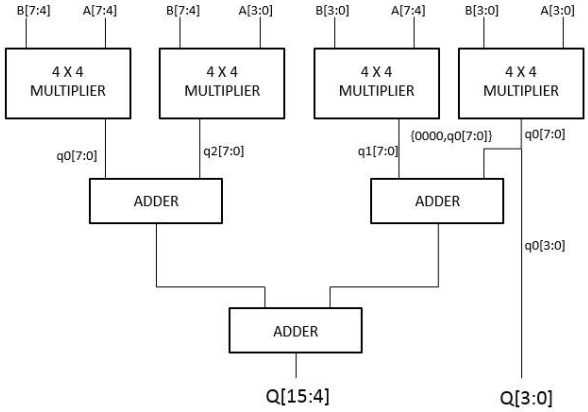

Figure 3 Block diagram of implementation of 8-bit using 4-bit multiplier

b) Implementation of 32-bit multiplier using 16-bit multiplier:

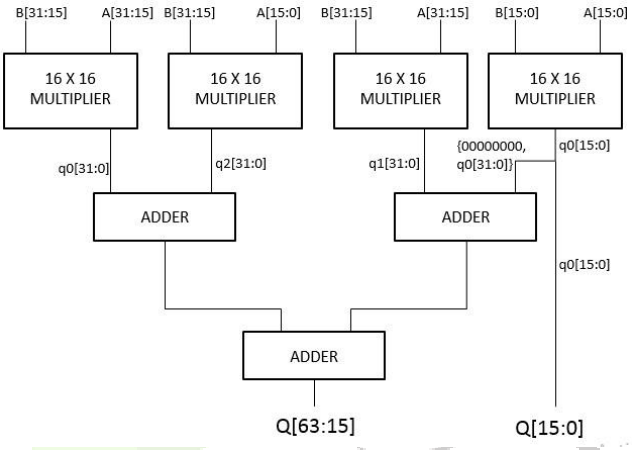

Figure 4 Block diagram of implementation of 32-bit using 16-bit multiplier

V. SIMULATION RESULTS AND DISCUSSION

The proposed 32 bit Systolic and Wallace multipliers simulation is done using Xilinx Vivado and implementation is done on Zynq 7000 series FPGA board. The below simulation result table 1 describes the performance comparison of 32 bit Systolic and Wallace multipliers based on parameters such as used number of slices, LUT's, I/O and total power consumed.

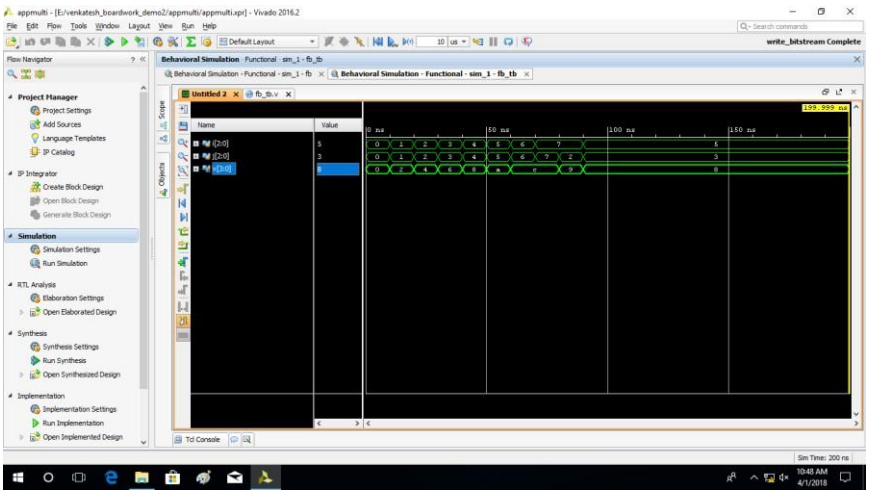

Figure 5 Simulation waveform of 32-bit Systolic multiplier

In the above mentioned Figure 5. Shows the waveform of 32 bit systolic multiplier obtained from the simulation of the proposed design in Xilinx Vivado.

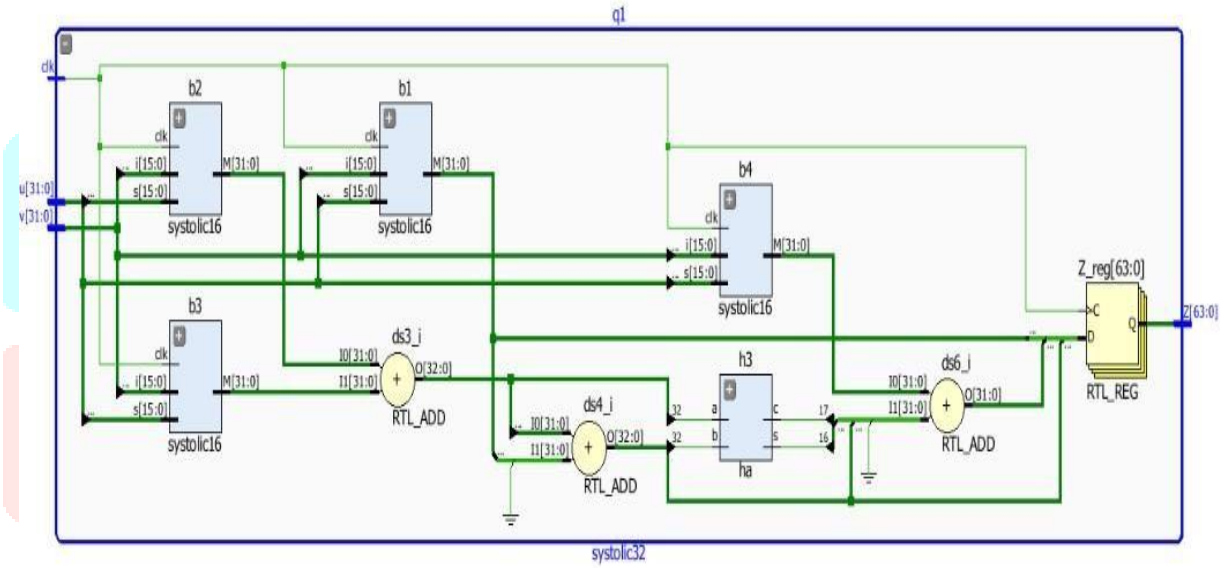

Figure 6 RTL Schematic of 32-bit Systolic multiplier

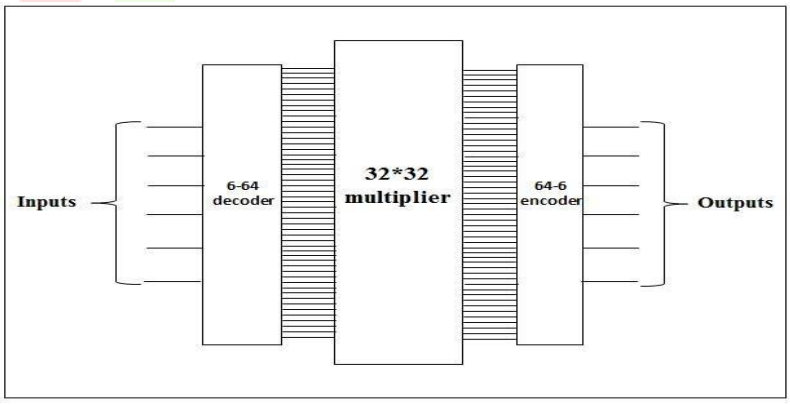

Figure 7 Block diagram of 32 bit multiplier for implementation on Zynq FPGA board

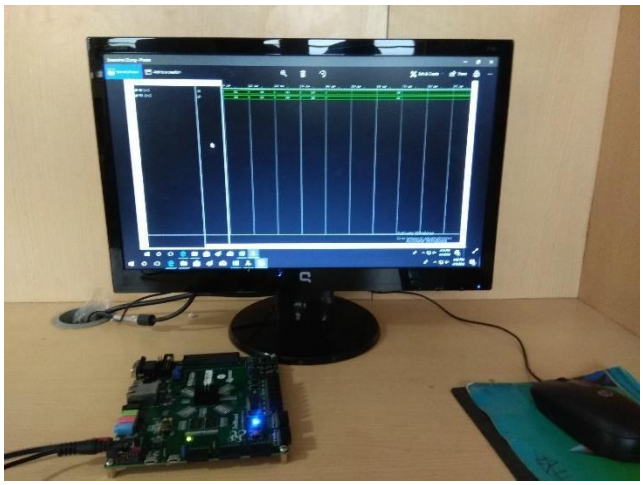

Figure 8 Hardware setup of FPGA implementation for 32 bit multiplier

Table 1: Performance comparison of 32 bit Multipliers

32 BIT MULTIPLIERS	SLICES	LUT'S	I/O	CONSUMED POWER (mW)
SYSTOLIC	2264/53200	1511/53200	129/200	2306
WALLACE	2200/53200	1430/53200	129/200	2180

VI. CONCLUSION AND FUTURE SCOPE

The simulation results of this proposed 32 bit Systolic and Wallace multipliers are quite good. From the simulation results, it is determined that Wallace multiplier is more efficient compared to systolic multiplier. The performance comparison is done based on obtained parameters such as LUT's, Slices, I/O and total consumed power that we get after the FPGA implementation. Further, these multipliers can be used to design multiply and accumulate (MAC) unit which has wide scope in digital signal processing applications.

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