RV32I Base Instruction Set

Instruction Formats

31	27	26	25	24	20	19		15	14	12	11		7	6		0	
$\frac{\text{funct7}}{\text{funct7}}$				1	rs2	rs1			funct3		rd		opcode			R-type	
		$\overline{\mathrm{imm}}$			rs1			funct3		rd		opcode			I-type		
	imm[11:5]			1	rs2	rs1			funct3		imm[4:0]		opcode			S-type	
	imm[12 10:5]			1	rs2		rs1		funct3		imm[4:1 11]		opcode			B-type	
	imm[31:12]											rd			opcode		U-type
	imm[20 10:1 11 19:12]														opcode		J-type

Instructions

31	27	26	25	24	20	19	15	14	12	11	7	6		0	
					[31:12]					rd)110111		LUI
					[31:12]					rd			0010111		AUIPC
				n[20 10]	0:1 11 1					rd			101111		JAL
		$\operatorname{imm}[$	11:0]			rs	1	000		rd			1100111		JALR
	mm[12				s2	rs		000		imm[4:1]			100011		BEQ
	mm[12				s2	rs	1	001		imm[4:1]			100011		BNE
	mm[12				s2	rs	1	100		imm[4:1]			100011		BLT
	mm[12				s2	rs		101		imm[4:1]			1100011		BGE
	mm[12				s2	rs		110		imm[4:1]			100011		BLTU
i	mm[12	10:5]		r	s2	rs	1	111		imm[4:1]	11]		100011		BGEU
		imm[rs	1	000		rd			0000011		LB
		$\mathrm{imm}[$				rs	1	001		rd			0000011		LH
		$\mathrm{imm}[$				rs	1	010		rd			0000011		LW
		$\mathrm{imm}[$				rs	1	100		rd			0000011		LBU
		$\mathrm{imm}[$	11:0]			rs	1	101		rd			0000011		LHU
	imm[1]			r	s2	rs	1	000		imm[4:0			0100011		SB
	imm[1]			r	s2	rs	1	001		imm[4:0	0]	(0100011		SH
	imm[1]	1:5]		r	s2	rs	1	010		imm[4:0	0]		0100011		SW
		imm[11:0]			rs	1	000)	rd		(0010011		ADDI
		imm[11:0]			rs	1	010)	rd		(0010011		SLTI
		imm[11:0]			rs	1	011		rd		(0010011		SLTIU
		imm[11:0]			rs	1	100)	rd		(0010011		XORI
		imm[11:0]			rs	1	110)	rd		(0010011		ORI
		imm[11:0]			rs	1	111		rd		(0010011		ANDI
	00000	00		r	s2	rs	1	000)	rd		()110011		ADD
	01000	00		r	s2	rs	1	000)	rd		()110011		SUB
	00000	00		r	s2	rs	1	001	L	rd		()110011		SLL
	00000	00		r	s2	rs	1	010)	rd		()110011		SLT
	00000	00		r	s2	rs	1	011	L	rd		()110011		SLTU
	00000	00		r	s2	rs	1	100)	rd		()110011		XOR
	00000	00		r	s2	rs	1	101	L	rd		()110011		SRL
	01000	00		r	s2	rs	1	101	L	rd		()110011		SRA
	00000	00		r	s2	rs	1	110)	rd		()110011		OR
	00000	00		r	s2	rs	1	111		rd		()110011		AND
fn	n	pr	ed		succ	rs	1	000)	rd		(0001111		FENCE
	00000	00		00	000	000	000	000)	00000		1	1110011		ECALL
	00000	00		00	001	000	000	000)	00000		1	1110011		EBREAK
	00000	00		sh	amt	rs	1	001		rd		(0010011		SLLI
	00000	00		sh	amt	rs	1	101		rd		(010011		SRLI
	01000	00		sh	amt	rs	1	101		rd		(0010011		SRAI
	10000	01		10	011	rs	1	000)	$^{ m rd}$		(0001111		FENCE.TS
	00000	00		10	000	000	000	000)	00000		(0001111		PAUSE