

# INSTRUCTION SET ARCHITECTURE

## Computer Architecture Lab Course Project

K Samhith 13CS01032

The following is the Instruction Set Architecture :

- Each instruction is 16 bits long.
- There are 8 registers available.
- There are 16 instructions in total.
- To support the proper addressing of these the op-code is 4 bit long and the register operand addressing is given a length of 3 bits.
- There are 4 types of instructions : R, I-1,I-2, J.
- The jump conditional and unconditional instructions are PC Relative.  
(i.e. After the instruction  $PC = PC + 1 + PC \text{ RELATIVE ADDRESS BIT}$ ).

### R Type Instructions :

Opcode (4)	Register-1 (3)	Register-2 (3)	Register-3 (3)	Spare (3)
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The following instructions are a part of this type :

Operation	opcode	Sample instruction	Machine code
Addition	ADD	ADD \$R1,\$R2,\$R3	1100010011001000
Multiplication	MUL	MUL \$R1,\$R2,\$R3	1101010011001000
And	AND	AND \$R1,\$R2,\$R3	1110010011001000
Exit	EXIT	EXIT	1111111111111111

Subtraction	SUB	SUB \$R1,\$R2,\$R3	1001010011001000
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### I-1Type Instructions :

Opcode (4)	Register-2 (3)	Register-1 (3)	Constant (6)
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The following instructions are a part of this type :

Operation	Opcode	Sample Instruction	Machine Code
Shift Left	SLL	SLL \$R1,\$R2,#20	1000010001010100
Sub Immediate	SUBI	SUBI \$R1,\$R2,+20	1010010001010100
Add Immediate	ADDI	ADDI \$R1,\$R2,+20	0100010001010100
Mult Immediate	MULI	MULI \$R1,\$R2,+20	0101010001010100
Load Word	LWI	LWI \$R1,\$R2,+20	0110010001010100
Store Word	SWI	SWI \$R1,\$R2,+20	0111010001010100

### I-2 Type Instructions :

Opcode (4)	Register-1 (3)	Register-2 (3)	PC Relative (6)
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The following instructions are a part of this type :

Operation	Opcode	Sample Instruction	Machine Code
Jump Equals	JE	JE \$R1,\$R2,#20	0000001010010100
Jump Not Equals	JNE	JNE \$R1,\$R2,#20	0001001010010100
Jump Less than	JL	JL \$R1,\$R2,#20	0010001010010100
Jump Greater than	JG	JG \$R1,\$R2,#20	001100101-010100

### J-Type Instruction :

Opcode (4)	Amount to be shifted relative to the next Program Counter (12)
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Only the jump instruction is a part of this type.

Jump Unconditional	J	J #20	1011000000010100
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*Register 1* : The first register which appears in the instruction.

*Register 2* : The second register which appears in the instruction.