

Operation	Opcode	Reg dst	ALU source	ALU OP	Memory read	Memory write	Reg write
AND	0001	0	0	00	0	0	1
OR	0010	0	0	01	0	0	1
ADD	0011	0	0	10	0	0	1
SUB	0100	0	0	11	0	0	1
ADDi	0011	1	1	10	0	0	1
SUBi	0100	1	1	11	0	0	1