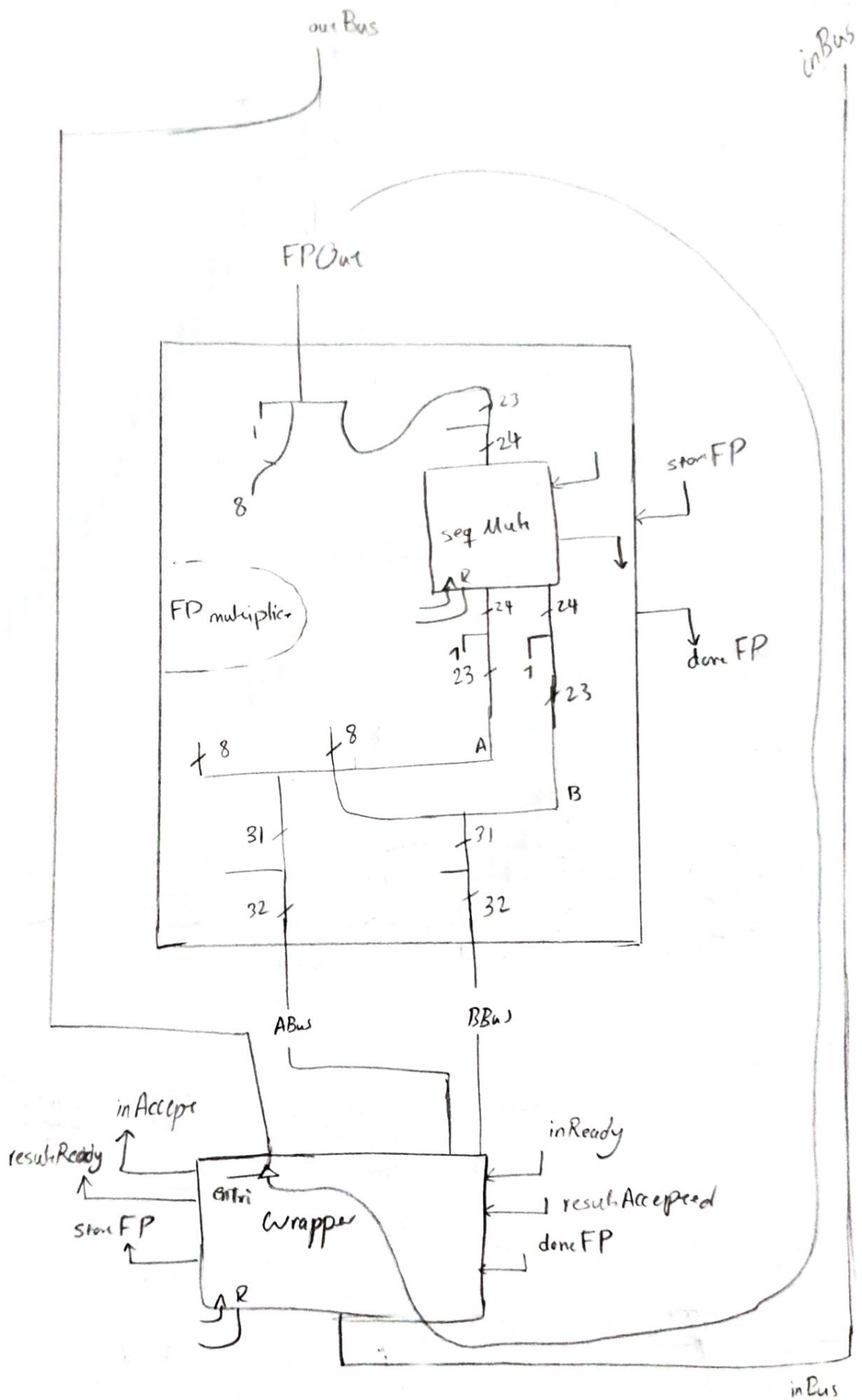
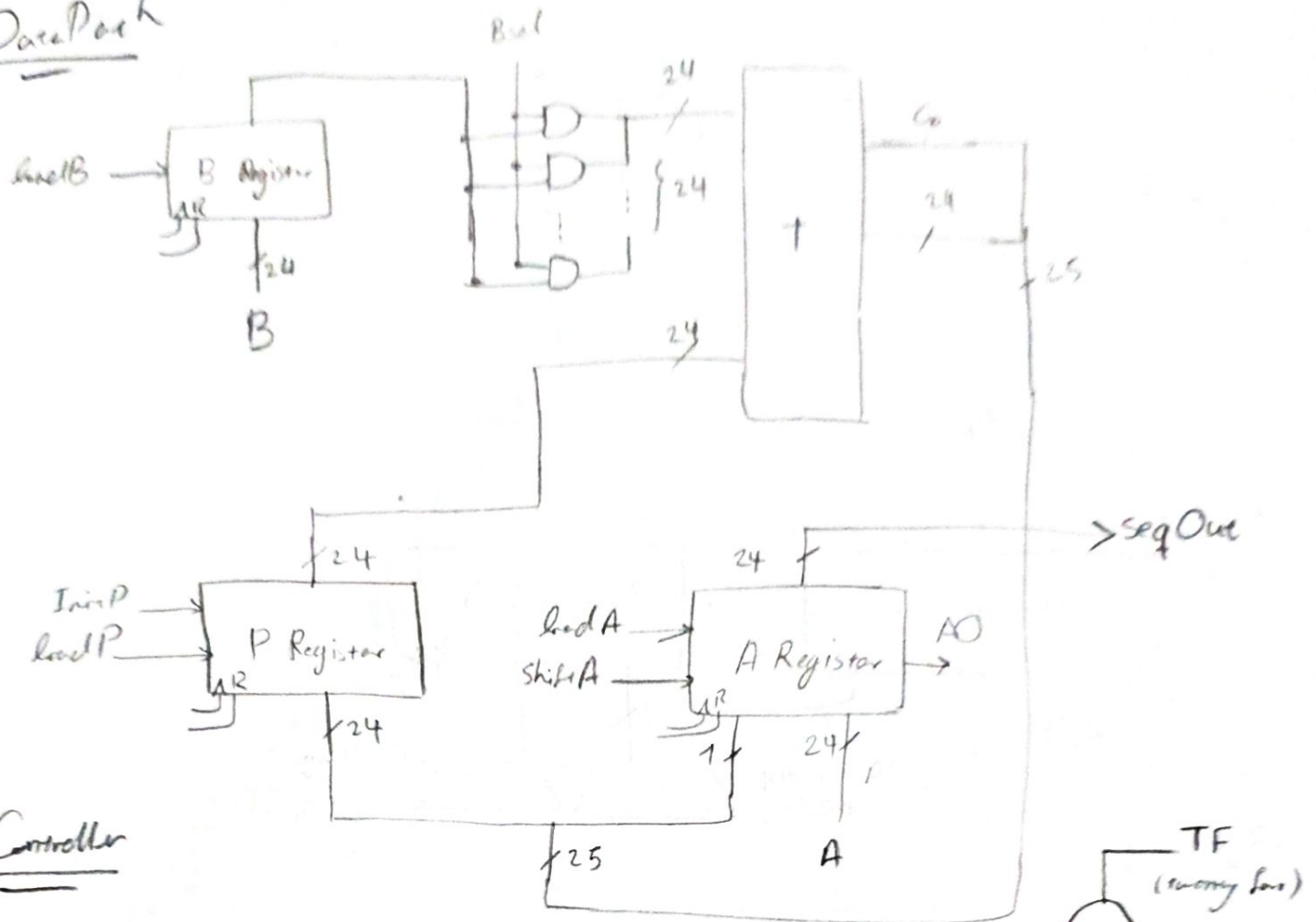


a) hierarchical block diagram

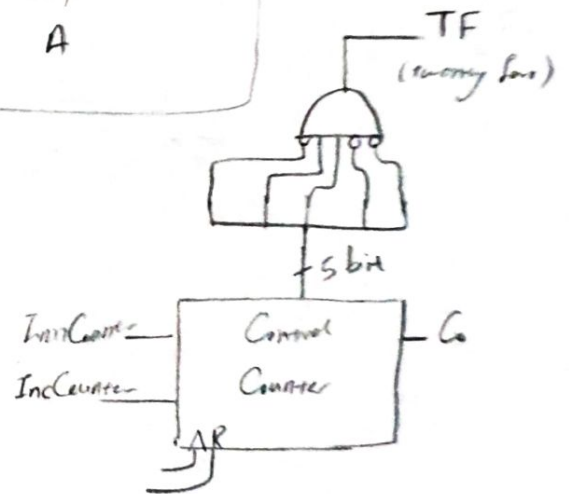
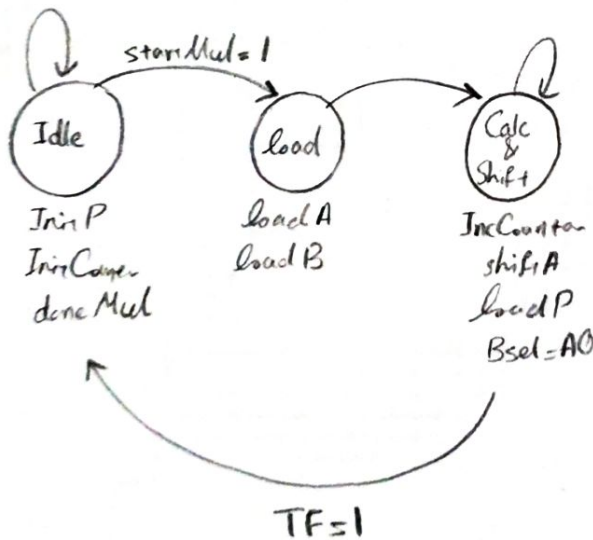


b) The Complete Design of the Sequential Multiplexer

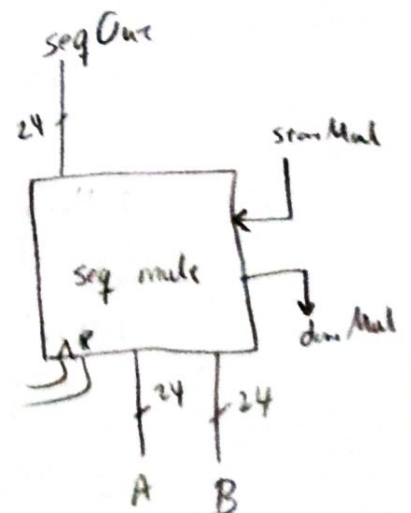
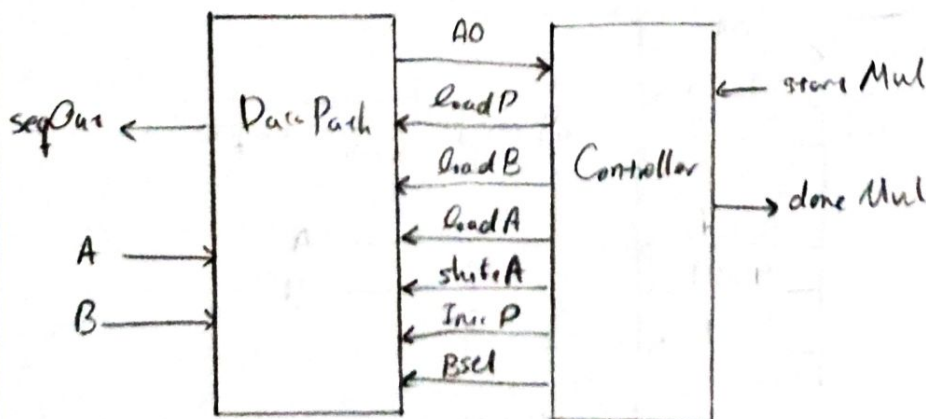
Data Path



Controller



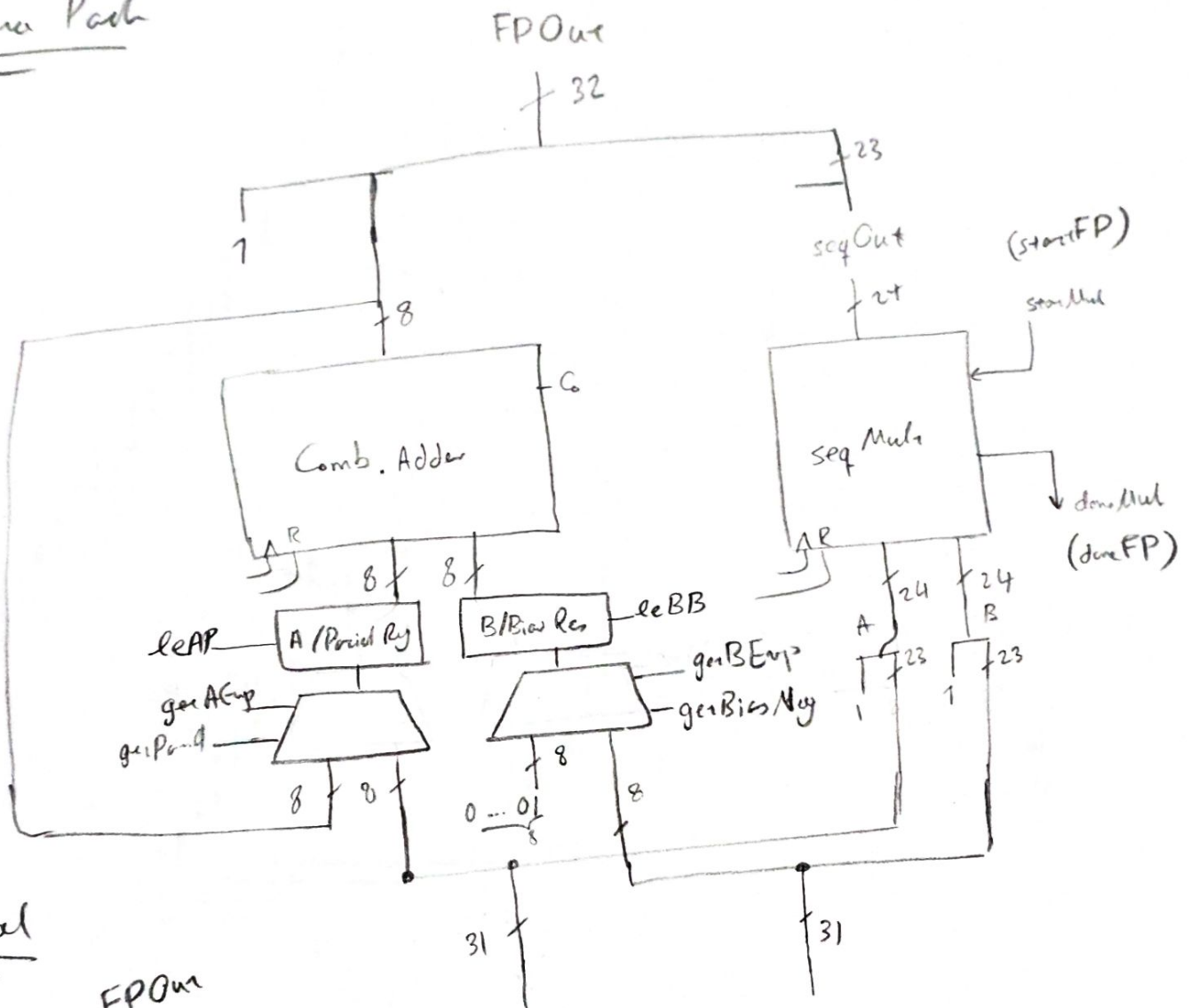
Final



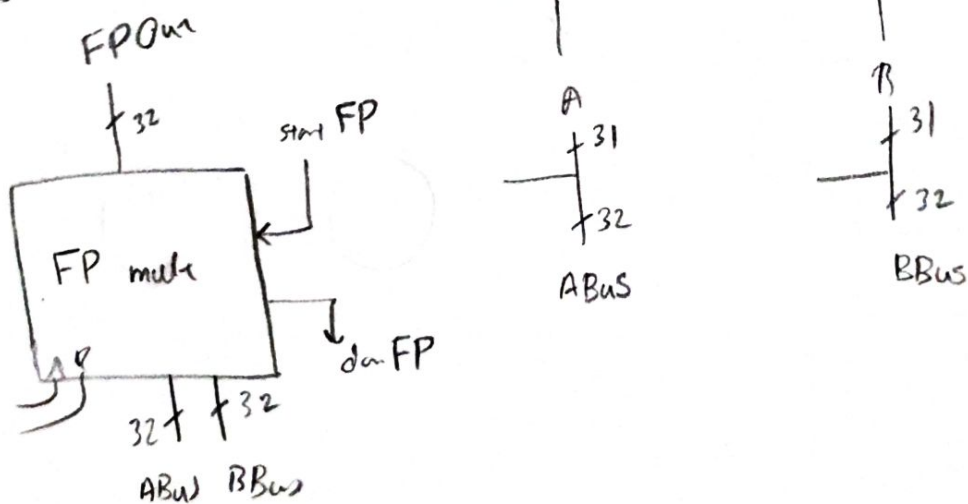
c) The DataPath of FP Multiplier Engine

The sequential multiplier generates output after 24 clocks while this number for combinational adder is 4 as a result startFP issues startMul and doneMul issues doneFP.

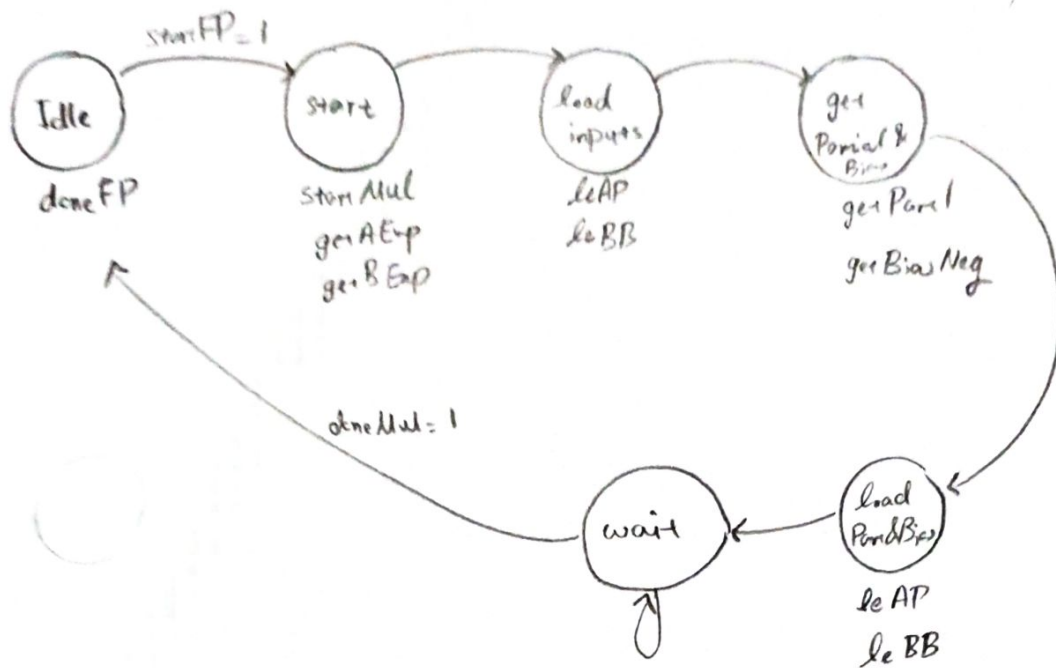
Data Path



Final

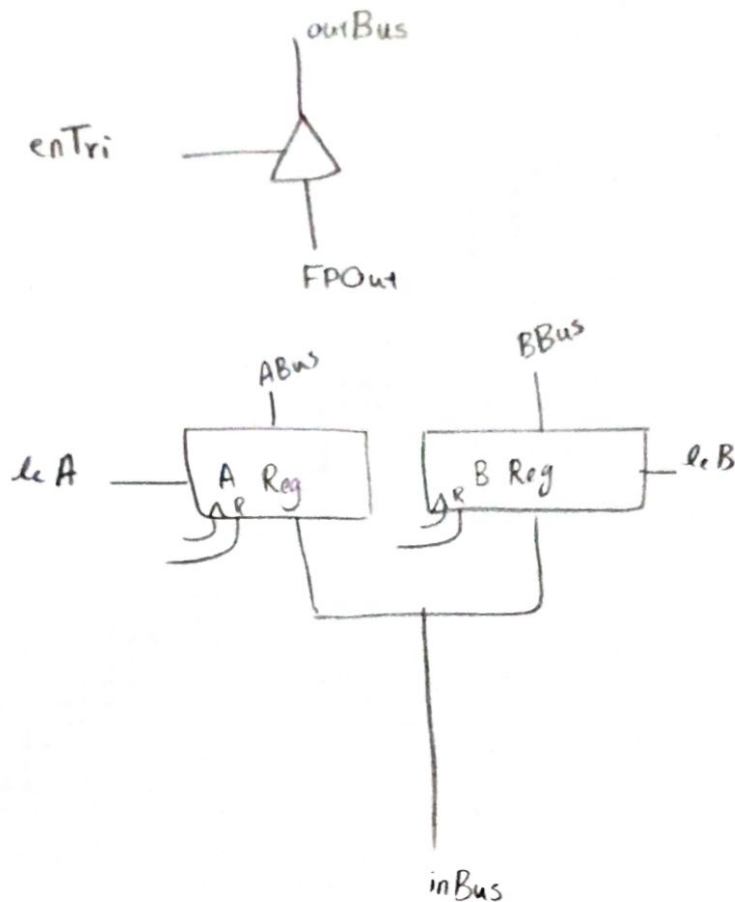


C-2) The Controller of FP multiplication:

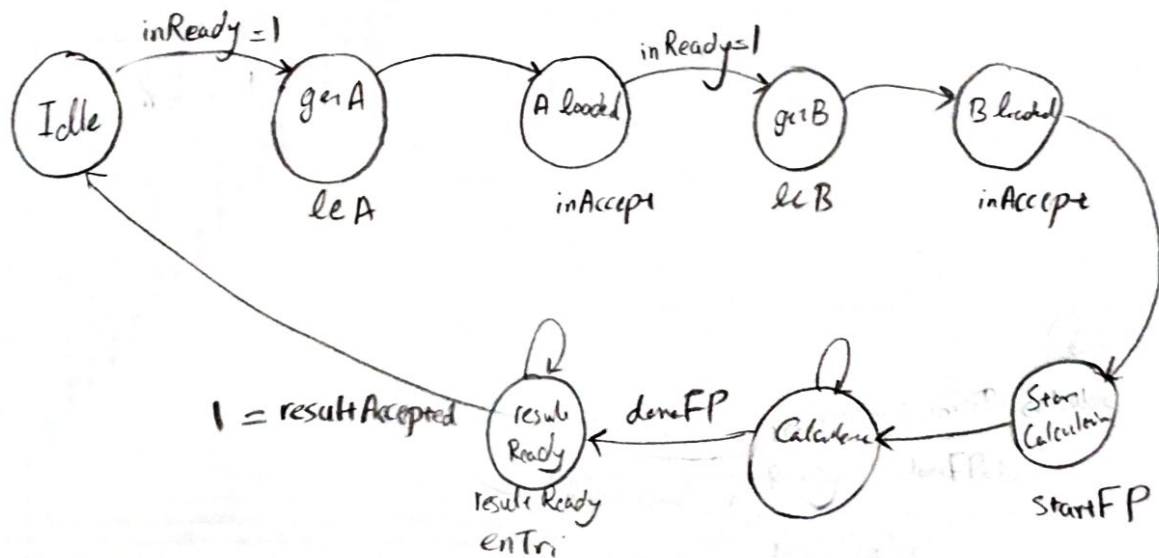


d) the wrappers:

Data Path



Controller



Final

