Digital Systems 1 – Computer Assignment 5
Samira Hajizadeh - 810198378
Part A)

The behavioral SystemVerilog description of the Moore machine that detects 10010:

```
Ln#
1   `timescale 1ns/1ns
2   module Q1(input Clock, j, Reset, output logic w);
3           //10010
4           logic [2:0] state;
5           parameter a=3'b000, b=3'b001, c=3'b010, d=3'b011, e=3'b100, f=3'b101;
6           always @(posedge Clock, posedge Reset) begin
7                   if(Reset) begin state<=a; w<=0; end
8                   else begin
9                           case (state)
10                                  a: if(j==1) begin w<=0; state<=b; end
11                                     else begin w<=0; state<=a; end
12                                  b: if(j==0) begin w<=0; state<=c; end
13                                     else begin w<=0; state<=b; end
14                                  c: if(j==0) begin w<=0; state<=d; end
15                                     else begin w<=0; state<=b; end
16                                  d: if(j==1) begin w<=0; state<=e; end
17                                     else begin w<=0; state<=a; end
18                                  e: if(j==0) begin w<=0; state<=f; end
19                                     else begin w<=0; state<=b; end
20                                  f: if(j==0) begin w<=1; state<=d; end
21                                     else begin w<=1; state<=b; end
22                                  default: state<=a;
23                          endcase
24                  end
25          end
26  endmodule
27
```

i) The System Verilog code of the test bench:

```
Ln#
1   `timescale 1ns/1ns
2   module moore_TB();
3
4           logic j;
5           logic clock;
6           logic reset = 0;
7           logic w;
8           logic w2;
9           Q1 m(clock, j, reset, w);
10
11          initial begin
12                  clock = 0;
13                  forever #50ns clock = ~clock;
14          end
15
16          initial begin
17                  #100ns j = 0;
18                  #100ns reset = 1;
19                  #100ns reset = 0;
20                  #100ns j = 1;
21                  #100ns j = 0;
22                  #100ns j = 0;
23                  #100ns j = 1;
24                  #100ns j = 0;
25                  #100ns j = 0;
26                  #100ns j = 1;
27                  #100ns j = 0;
28                  #100ns j = 0;
29                  #100ns j = 0;
30                  #100ns j = 1;
31                  #100ns j = 0;
32                  #100ns j = 0;
33                  #100ns $stop;
34          end
35
36  endmodule
```

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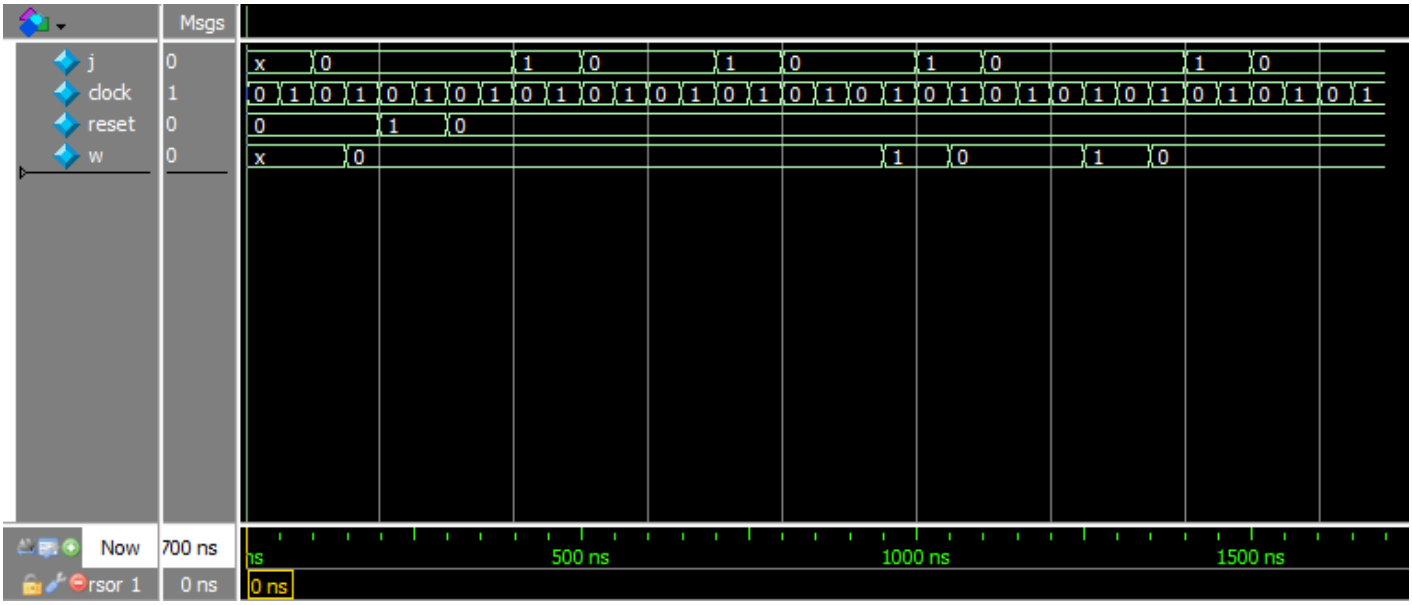
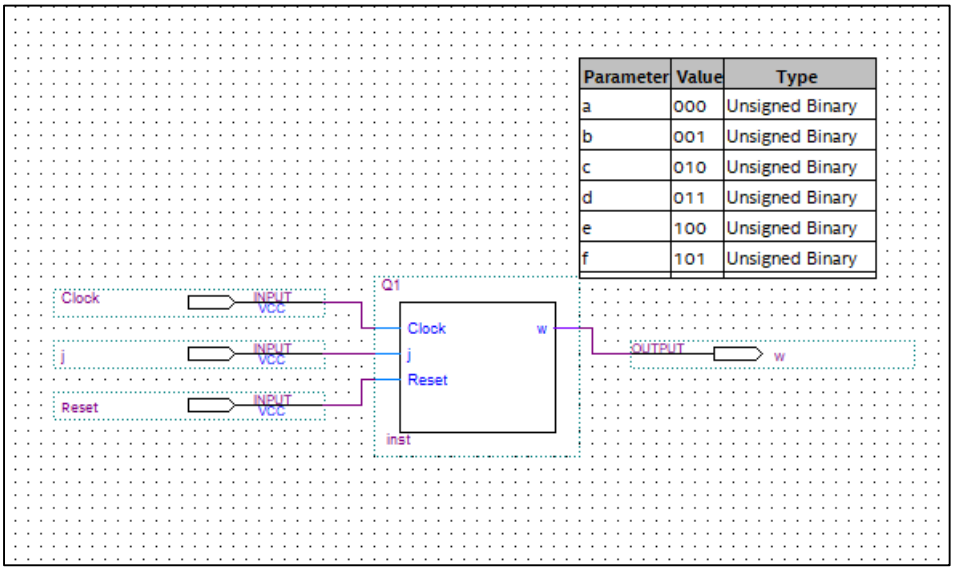
The output waveform which validates the System Verilog code:



After all parts of the sequence is detected, as the next clock rises and the positive edge written in the sensitivity list is triggered, the output becomes one and stays the same until the next clock rise. Due to the design of the test bench, the sequence is also detected in t = 1250.

A-ii) The created symbol of the moore machine:



The flow summary of the compilation of the symbol:

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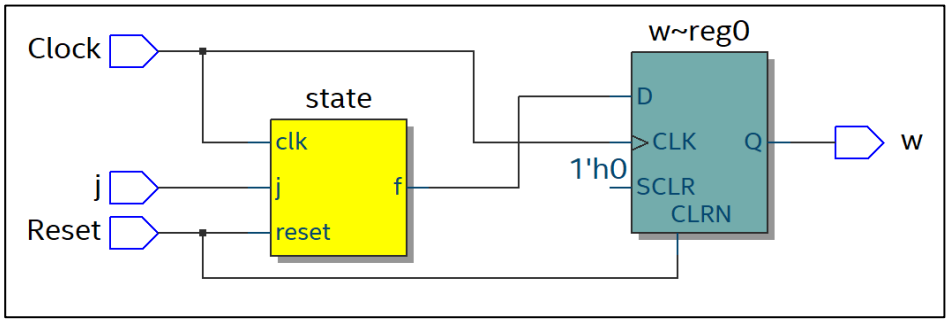
Flow Summary

<<Filter>>

Flow Status	Successful - Mon Jun 14 18:59:56 2021
Quartus Prime Version	20.1.0 Build 711 06/05/2020 SJ Lite Edition
Revision Name	Q1
Top-level Entity Name	Q1
Family	Cyclone IV E
Device	EP4CE6E22A7
Timing Models	Final
Total logic elements	6 / 6,272 (< 1 %)
Total registers	6
Total pins	4 / 92 (4 %)
Total virtual pins	0
Total memory bits	0 / 276,480 (0 %)
Embedded Multiplier 9-bit elements	0 / 30 (0 %)
Total PLLs	0 / 2 (0 %)

The number of logic elements used is another word for the number of cells.



Post mapping view:

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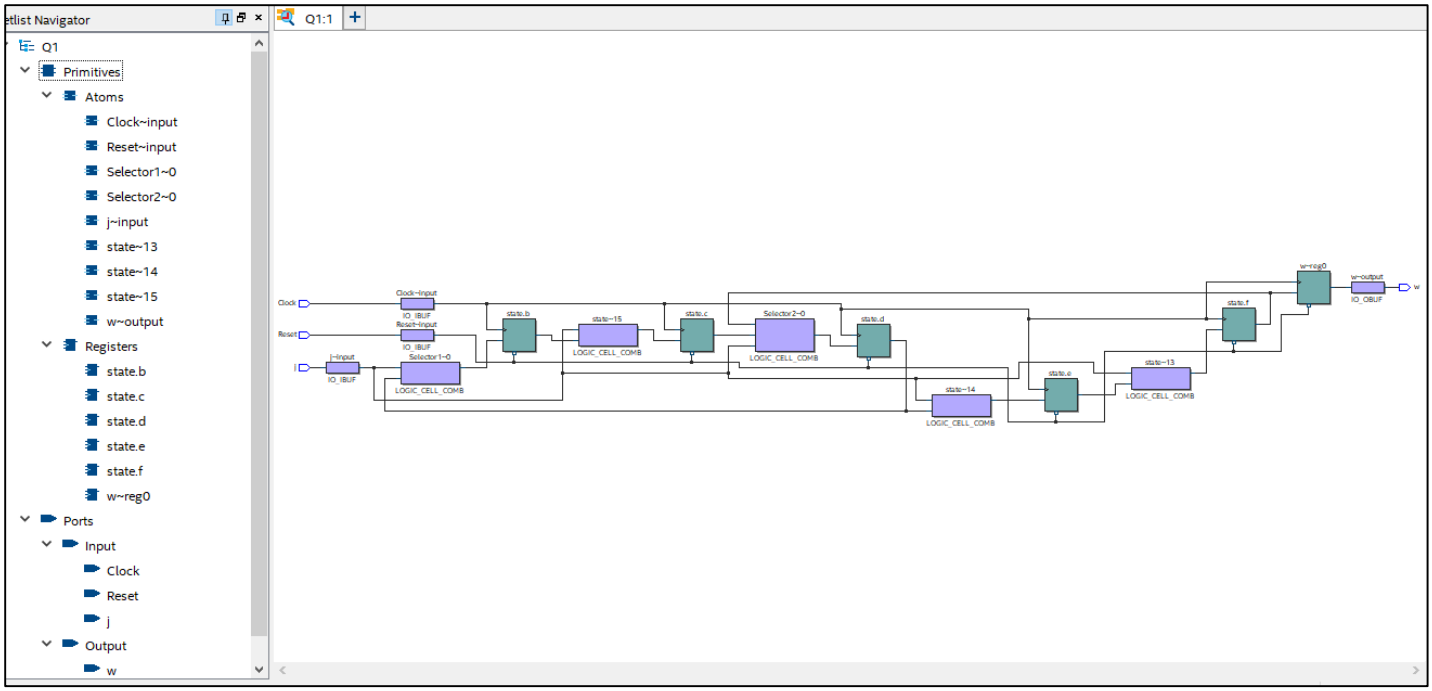
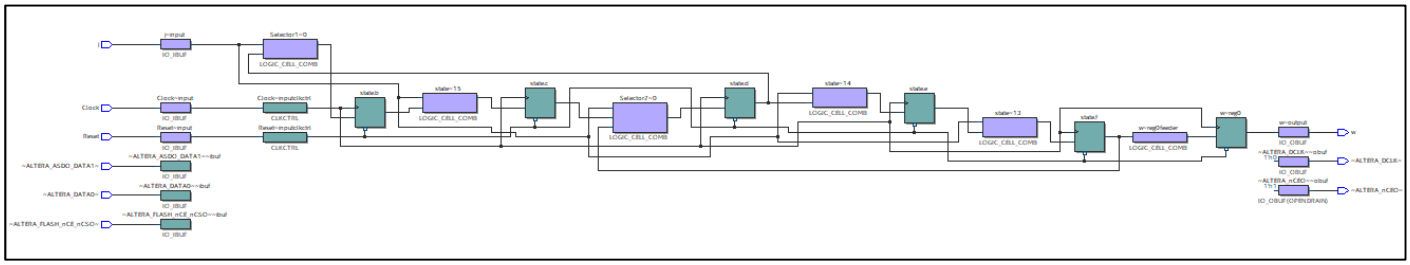
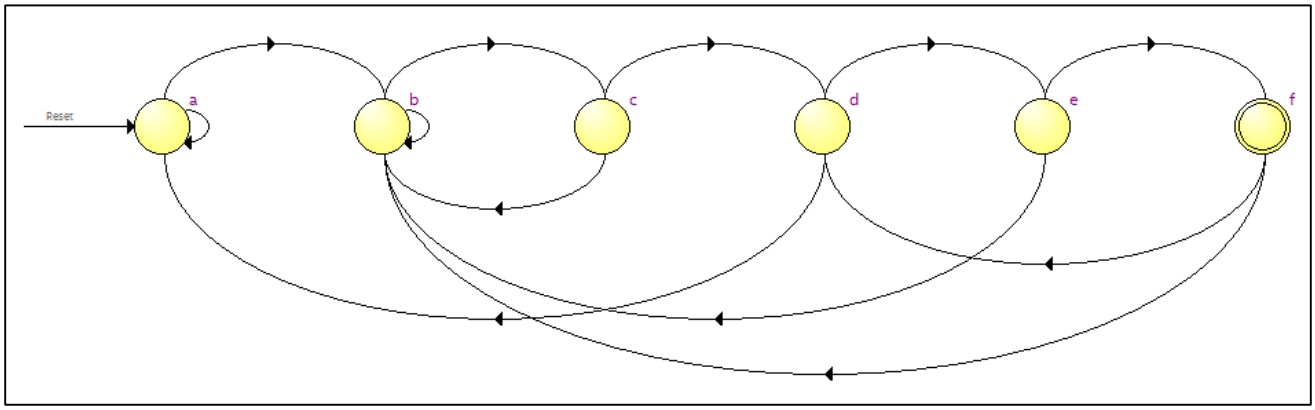


Post-fitting view:



State machine view:



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Transitions and Encoding:

	Source State	Destination State	Condition
1	a	a	(!j)
2	a	b	(j)
3	b	c	(!j)
4	b	b	(j)
5	c	d	(!j)
6	c	b	(j)
7	d	e	(j)
8	d	a	(!j)
9	e	f	(!j)
10	e	b	(j)
11	f	d	(!j)
12	f	b	(j)

	Name	f	e	d	c	b	a
1	a	0	0	0	0	0	0
2	b	0	0	0	0	1	1
3	c	0	0	0	1	0	1
4	d	0	0	1	0	0	1
5	e	0	1	0	0	0	1
6	f	1	0	0	0	0	1

Timings:

	Clock Name	Type	Period	Frequency	Rise	Fall	Duty Cycle	Divide by	Multi
1	Clock	Base	1.000	1000.0 MHz	0.000	0.500			

	Pin	I/O Standard	10-90 Rise Time	90-10 Fall Time
1	Clock	2.5 V	2000 ps	2000 ps
2	Reset	2.5 V	2000 ps	2000 ps
3	j	2.5 V	2000 ps	2000 ps
4	~ALTERA_ASDO_DATA1~	2.5 V	2000 ps	2000 ps
5	~ALTERA_FLASH_nCE_nCSO~	2.5 V	2000 ps	2000 ps
6	~ALTERA_DATA0~	2.5 V	2000 ps	2000 ps

A-iii) In order to instantiate from the output of the synthesize, its name was changed to Q1_2.

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```
29
30    `timescale 1 ps/ 1 ps
31
32    module Q1_2 (
33            Clock,
34            j,
35            Reset,
36            w);
37    input   Clock;
38    input   j;
39    input   Reset;
40    output  w;
41
42    // Design Ports Information
43    // w    =>  Location: PIN_33,    I/O
```

Wave | Q1.sv | Q1_TB.sv | Q1.svo

The picture of the updated test bench:

```
Ln#
 1    `timescale 1ns/1ns
 2    module moore_TB();
 3
 4            logic j;
 5            logic clock;
 6            logic reset = 0;
 7            logic w;
 8            logic w2;
 9            Q1 m(clock, j, reset, w);
10            Q1_2 m2(clock, j, reset, w2);
11
12            initial begin
13                    clock = 0;
14                    forever #50ns clock = ~clock;
15            end
16
17            initial begin
18                    #100ns j = 0;
19                    #100ns reset = 1;
20                    #100ns reset = 0;
21                    #100ns j = 1;
22                    #100ns j = 0;
23                    #100ns j = 0;
24                    #100ns j = 1;
25                    #100ns j = 0;
26                    #100ns j = 0;
27                    #100ns j = 1;
28                    #100ns j = 0;
29                    #100ns j = 0;
30                    #100ns j = 0;
31                    #100ns j = 1;
32                    #100ns j = 0;
33                    #100ns j = 0;
34                    #100ns $stop;
35            end
36
37    endmodule
38
```

The output waveform of the test bench:

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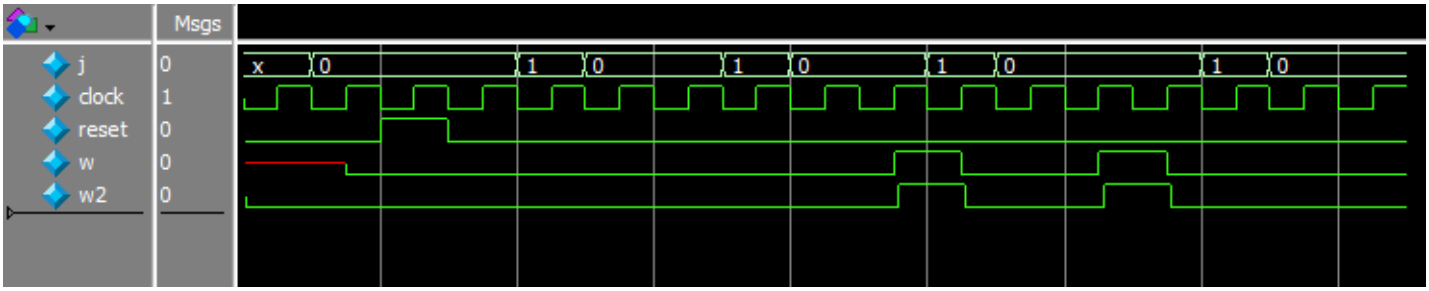

As seem in the picture the output of the post-synthesize module has output delay. in other words, contrarily to ‘w’ that alters instantaneously as the given delay in test bench is finished, ‘w2’ changes a 6ns delay on top of the given one. The reason for this is that the System Verilog code is assigned to a cycloneiv-family hardware and contains its specified gate delays.

Part B)

The behavioral SystemVerilog description of the Mealy machine that detects 10010:

```
1   `timescale 1ns/1ns
2
3   module Q2(input Clock, j, Reset, output logic w);
4           //10010
5           logic [2:0] state;
6           parameter a=3'b000, b=3'b001, c=3'b010, d=3'b011, e=3'b100;
7           always @(posedge Clock, posedge Reset) begin
8                   if(Reset) begin state<=a; w<=0; end
9                   else begin
10                          case (state)
11                                  a: if(j==1) begin w<=0; state<=b; end
12                                     else begin w<=0; state<=a; end
13                                  b: if(j==0) begin w<=0; state<=c; end
14                                     else begin w<=0; state<=b; end
15                                  c: if(j==0) begin w<=0; state<=d; end
16                                     else begin w<=0; state<=b; end
17                                  d: if(j==1) begin w<=0; state<=e; end
18                                     else begin w<=0; state<=a; end
19                                  e: if(j==0) begin w<=1; state<=c; end
20                                     else begin w<=0; state<=b; end
21                                  default: state<=a;
22                          endcase
23                  end
24          end
25  endmodule
26
```

i) The System Verilog code of the test bench:

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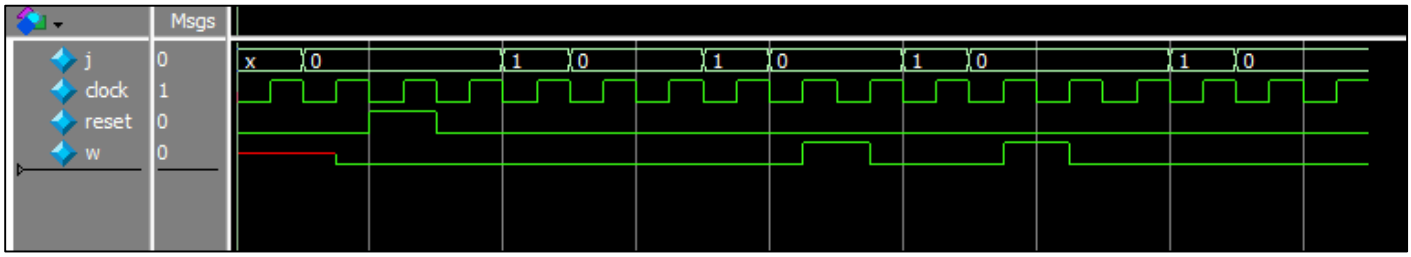
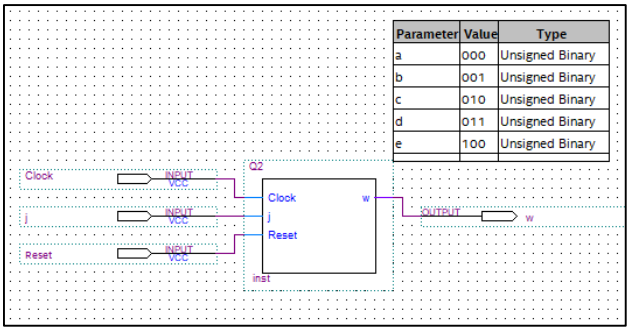
```
1   `timescale 1ns/1ns
2   module mealy_TB();
3
4           logic j;
5           logic clock;
6           logic reset = 0;
7           logic w;
8           Q2 m(clock, j, reset, w);
9
10          initial begin
11                  clock = 0;
12                  forever #50ns clock = ~clock;
13          end
14
15          initial begin
16                  #100ns j = 0;
17                  #100ns reset = 1;
18                  #100ns reset = 0;
19                  #100ns j = 1;
20                  #100ns j = 0;
21                  #100ns j = 0;
22                  #100ns j = 1;
23                  #100ns j = 0;
24                  #100ns j = 0;
25                  #100ns j = 1;
26                  #100ns j = 0;
27                  #100ns j = 0;
28                  #100ns j = 0;
29                  #100ns j = 1;
30                  #100ns j = 0;
31                  #100ns j = 0;
32                  #100ns $stop;
33          end
34
35  endmodule
36
```

The output waveform which validates the System Verilog code:



After all parts of the sequence is detected, the output becomes one immediately and stays the same until the next clock rise. Due to the design of the test bench, the sequence is also detected in t = 1150.

A-ii) The created symbol of the mealy machine:



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The flow summary of the compilation of the symbol:

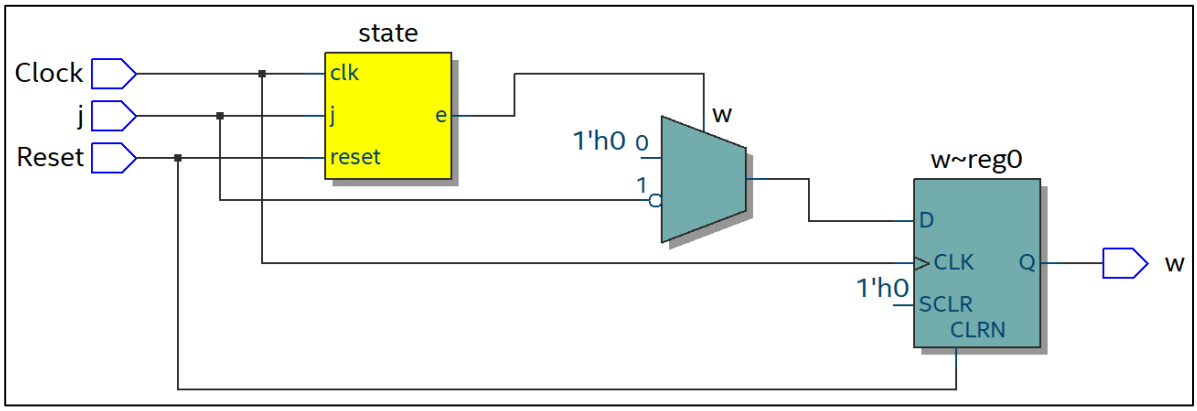
Flow Summary

<<Filter>>

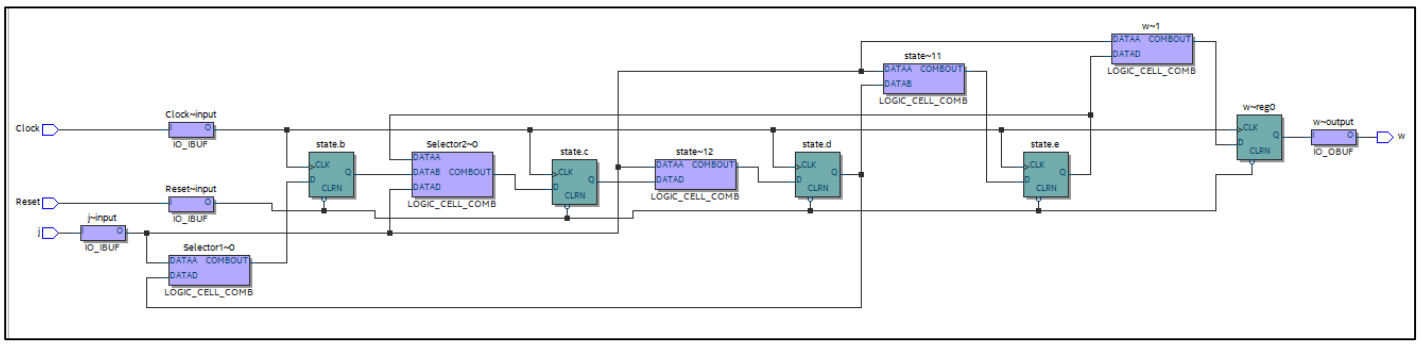
Flow Status	Successful - Mon Jun 14 21:27:24 2021
Quartus Prime Version	20.1.0 Build 711 06/05/2020 SJ Lite Edition
Revision Name	Q2
Top-level Entity Name	Q2
Family	Cyclone IV E
Device	EP4CE6E22A7
Timing Models	Final
Total logic elements	5 / 6,272 (< 1 %)
Total registers	5
Total pins	4 / 92 (4 %)
Total virtual pins	0
Total memory bits	0 / 276,480 (0 %)
Embedded Multiplier 9-bit elements	0 / 30 (0 %)
Total PLLs	0 / 2 (0 %)

The number of logic elements used is another word for the number of cells.

RTL viewer:



Post mapping view:



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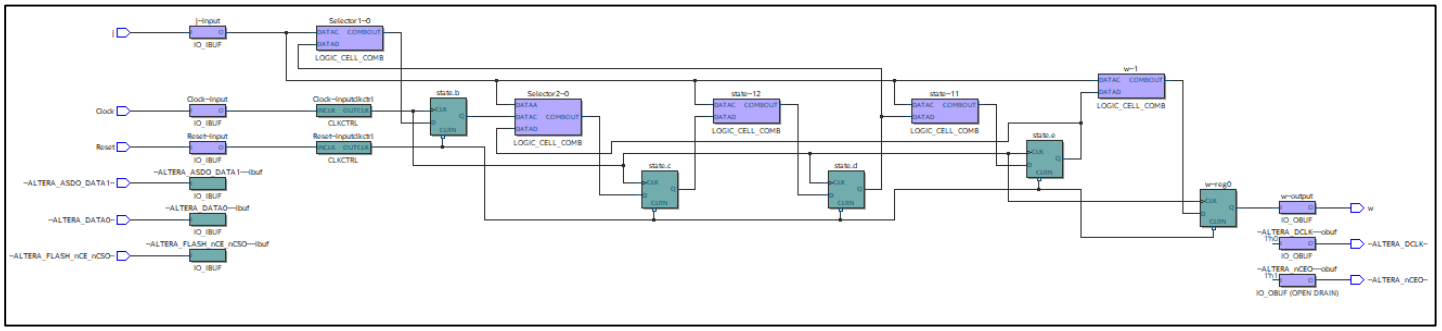
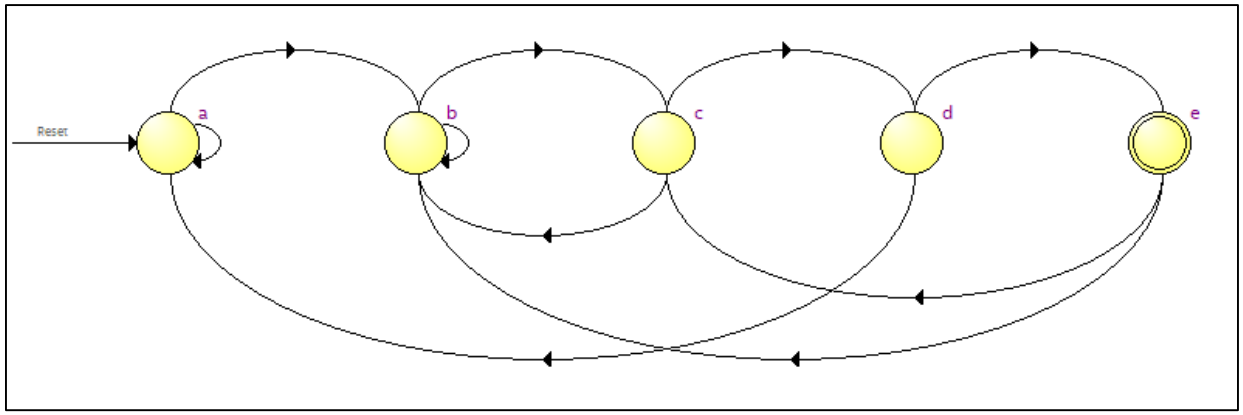
Post-fitting view:



State machine view:



Transitions and Encoding:

	Source State	Destination State	Condition
1	a	b	(j)
2	a	a	(!j)
3	b	b	(j)
4	b	c	(!j)
5	c	b	(j)
6	c	d	(!j)
7	d	e	(j)
8	d	a	(!j)
9	e	b	(j)
10	e	c	(!j)

	Name	d	c	b	a	e
1	a	0	0	0	0	0
2	b	0	0	1	1	0
3	c	0	1	0	1	0
4	d	1	0	0	1	0
5	e	0	0	0	1	1

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Samira Hajizadeh - 810198378

Timings:

Clocks

<<Filter>>

	Clock Name	Type	Period	Frequency	Rise	Fall	Duty Cycle	Divide by	Multi
1	Clock	Base	1.000	1000.0 MHz	0.000	0.500			

	Pin	I/O Standard	10-90 Rise Time	90-10 Fall Time
1	j	2.5 V	2000 ps	2000 ps
2	Clock	2.5 V	2000 ps	2000 ps
3	Reset	2.5 V	2000 ps	2000 ps
4	~ALTERA_ASDO_DATA1~	2.5 V	2000 ps	2000 ps
5	~ALTERA_FLASH_nCE_nCSO~	2.5 V	2000 ps	2000 ps
6	~ALTERA_DATA0~	2.5 V	2000 ps	2000 ps

A-iii) In order to instantiate from the output of the synthesize, its name was changed to Q2_2.

```
`timescale 1 ps/ 1 ps

module Q2_2 (
        Clock,
        j,
        Reset,
        w);
input   Clock;
input   j;
input   Reset;
output  w;
```

The picture of the updated test bench:

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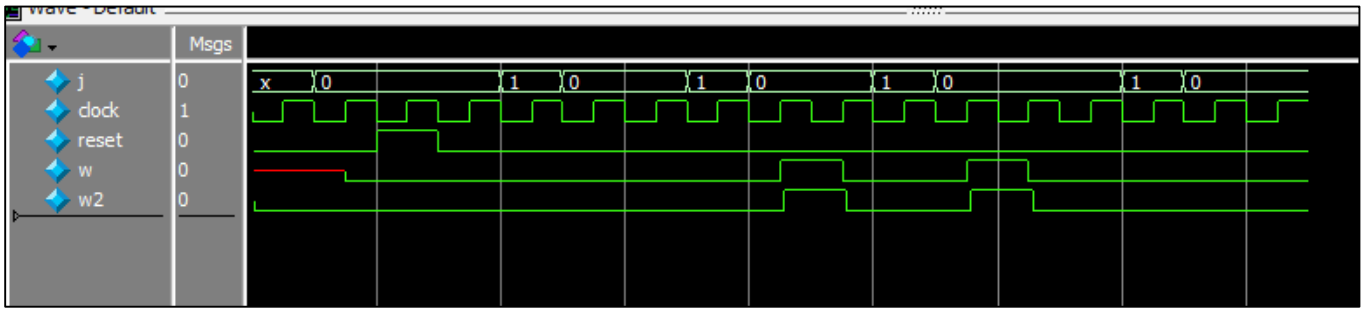
```
1   `timescale 1ns/1ns
2   module mealy_TB();
3
4           logic j;
5           logic clock;
6           logic reset = 0;
7           logic w;
8           logic w2;
9           Q2 m(clock, j, reset, w);
10          Q2_2 m2(clock, j, reset, w2);
11
12          initial begin
13                  clock = 0;
14                  forever #50ns clock = ~clock;
15          end
16
17          initial begin
18                  #100ns j = 0;
19                  #100ns reset = 1;
20                  #100ns reset = 0;
21                  #100ns j = 1;
22                  #100ns j = 0;
23                  #100ns j = 0;
24                  #100ns j = 1;
25                  #100ns j = 0;
26                  #100ns j = 0;
27                  #100ns j = 1;
28                  #100ns j = 0;
29                  #100ns j = 0;
30                  #100ns j = 0;
31                  #100ns j = 1;
32                  #100ns j = 0;
33                  #100ns j = 0;
34                  #100ns $stop;
35          end
36
37  endmodule
38
```

The output waveform of the test bench:



As seem in the picture the output of the post-synthesize module has output delay. in other words, contrarily to ‘w’ that alters instantaneously as the given delay in test bench is finished, ‘w2’ changes a 6 ns delay on top of the given one. The reason for this is that the System Verilog code is assigned to a cycloneiv-family hardware and contains its specified gate delays.

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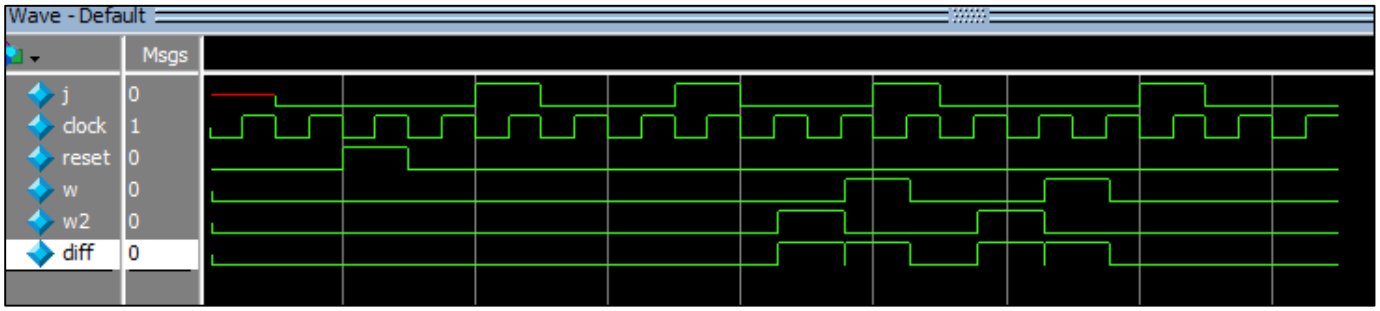
Part c)

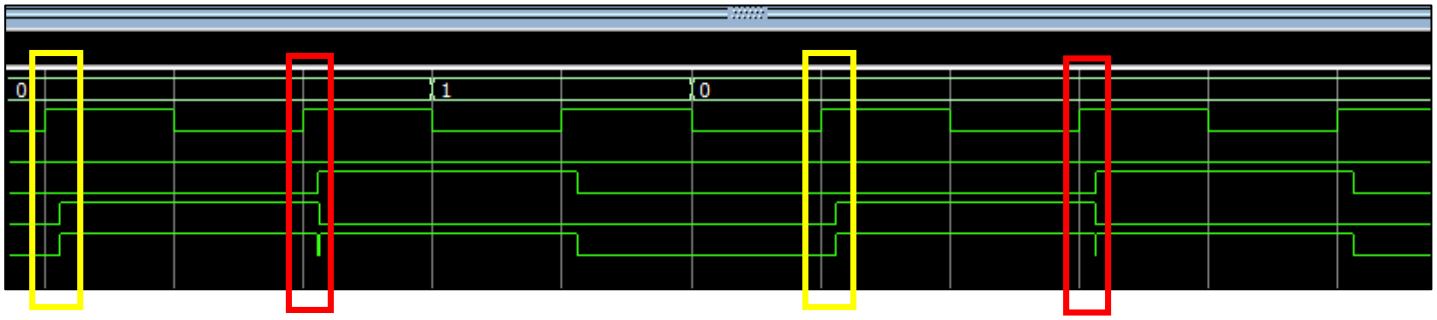
C-i) The SystemVerilog description of the test bench:

```
`timescale 1ns/1ns
module combined_TB();

        logic j;
        logic clock;
        logic reset = 0;
        logic w;
        logic w2;
        logic diff;
        Q1_2 m(clock, j, reset, w);
        Q2_2 m2(clock, j, reset, w2);

        assign diff = w^w2;
        initial begin
                clock = 0;
                forever #50ns clock = ~clock;
        end
        initial begin
                #100ns j = 0;
                #100ns reset = 1;
                #100ns reset = 0;
                #100ns j = 1;
                #100ns j = 0;
                #100ns j = 0;
                #100ns j = 1;
                #100ns j = 0;
                #100ns j = 0;
                #100ns j = 1;
                #100ns j = 0;
                #100ns j = 0;
                #100ns j = 0;
                #100ns j = 1;
                #100ns j = 0;
                #100ns j = 0;
                #100ns $stop;
        end

endmodule
```

The output waveform of the test bench:



C-ii) Better view of the differences:



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When there is a difference between the outputs of the machines, the last line becomes one. Among all the times that the last line is one in the red boxes there is an area that the difference cannot be ignored because the equality is a mere result of the delay and the real outputs are different. (the area starts from the white lines inside the box until when last line becomes zero).

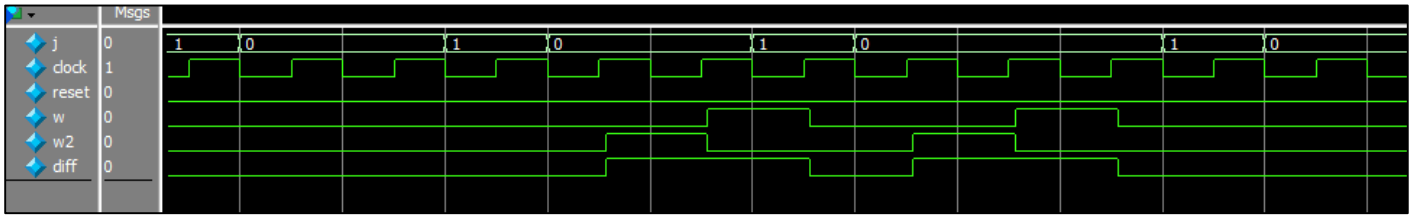
Note: an are in the yellow boxes should be considered as difference but it is not; due to the machine delays.

C-iii) By putting the assignment statement inside an always and forever statement on top of adding a 6ns delay to it, the problem with the red boxes get resolved.

The updated part of the test bench:

```
assign diff = w|w2;
initial begin
        clock = 0;
        forever #50ns clo
end
```

The output waveform:



Explanation: As for the design of the machine, we know that their value beyond the gate delays cannot be one simultaneously, therefore we can use an OR gate instead of an XOR gate so that the problem gets solved.