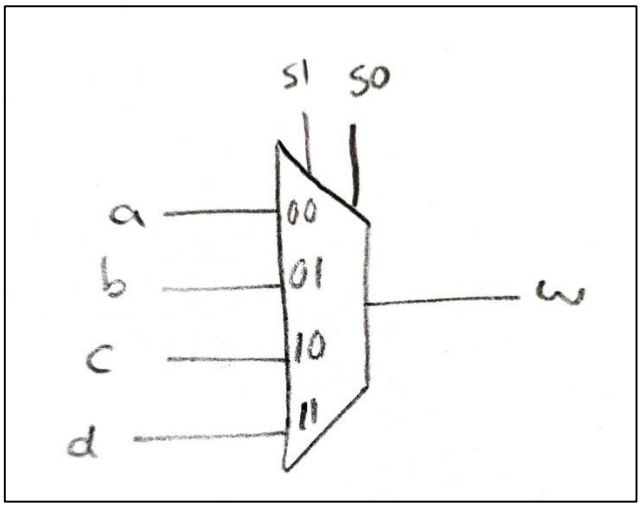
Digital Systems 1 – CA2
Samira Hajizadeh 810198378

Question 1

A)



B) As indicated in the last computer assignment, the calculated to 0 and to 1 delays are 28 and 32 respectively.

C)

```
Ln#
1   `timescale 1ns/1ns
2   module MUX4to1(a, b, c, d, s0, s1, w);
3
4           input a, b, c, d, s0, s1;
5           output w;
6
7           assign #(32,28) w = s1 ? (s0 ? d : c) : (s0 ? b : a);
8
9   endmodule
10
```

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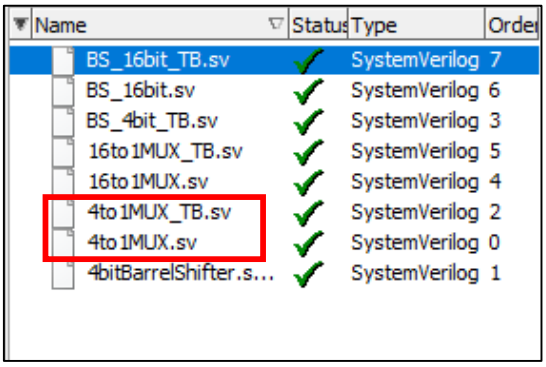
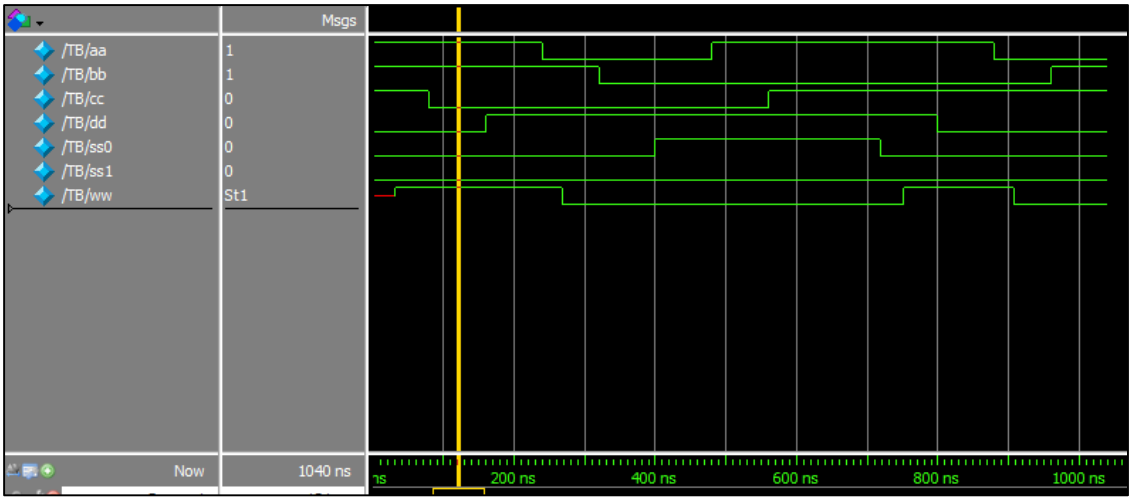
```
Ln#
 1  `timescale 1ns/1ns
 2  module TB();
 3          logic aa=1, bb=1, cc=1, dd=0, ss0=0, ss1=0;
 4          wire ww;
 5          MUX4to1 mux(aa, bb, cc, dd, ss0, ss1, ww);
 6          initial begin
 7          #1080 cc=0;
 8          #80 dd=1;
 9          #80 aa=0;
10          #80 bb=0;
11          #80 ss0=1;
12          #80 aa=1;
13          #80 cc=1;
14          #80 aa=1;
15          #80 ss0=0;
16          #80 dd=0;
17          #80 aa=0;
18          #80 bb=1;
19
20          #80 $stop;
21          end
22
23  endmodule
```

D)



E)



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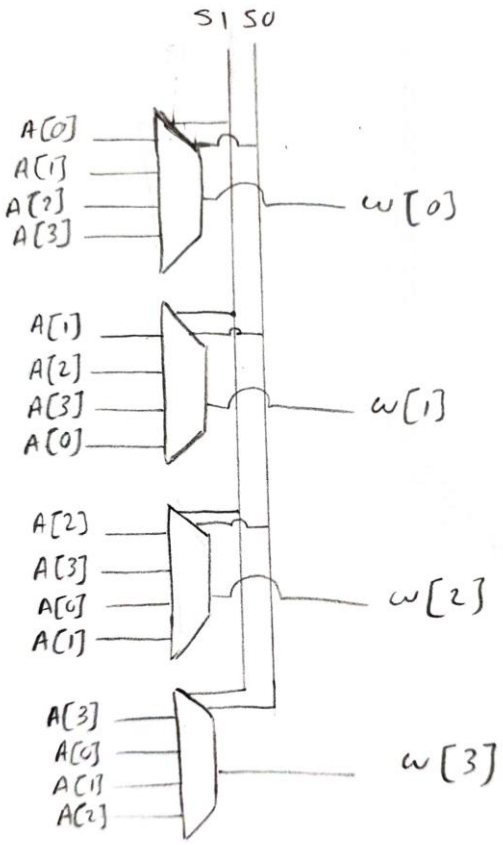
Question 2

A)



B) multiplexers delays are: (32, 28)

Four multiplexers produce the results. If all of A array's members are not the same and s0 and s1 are not equal to 0, then there will be a to 0 change in at least one of the multiplexers.

Worst case delay: 32

C)

```
Ln#
 1  `timescale 1ns/1ns
 2  module BS_4bit(input [1:0] s, [3:0] A, output [3:0] w);
 3
 4          MUX4to1 mux1(A[0], A[1], A[2], A[3], s[0], s[1], w[0]),
 5                  mux2(A[1], A[2], A[3], A[0], s[0], s[1], w[1]),
 6                  mux3(A[2], A[3], A[0], A[1], s[0], s[1], w[2]),
 7                  mux4(A[3], A[0], A[1], A[2], s[0], s[1], w[3]);
 8
 9  endmodule
10
```

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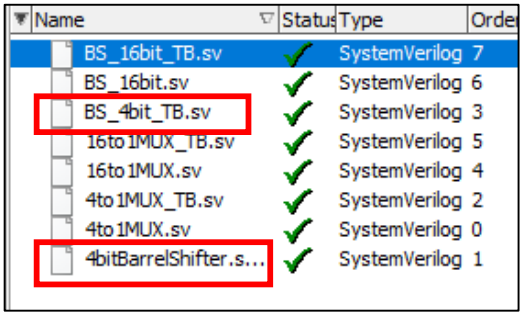
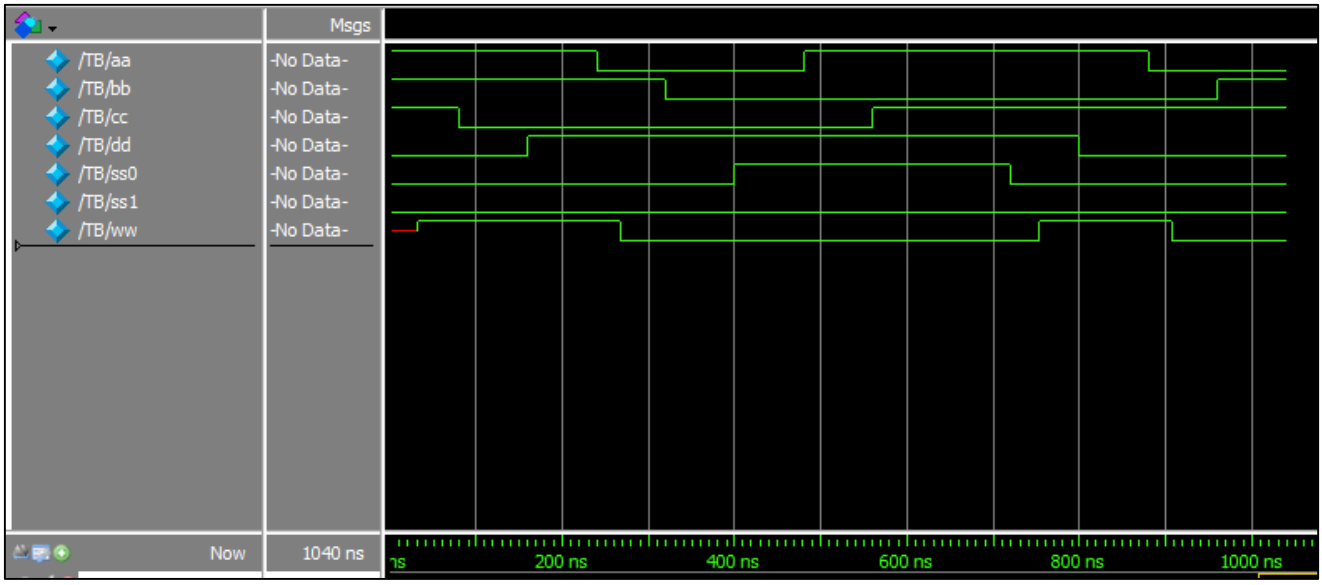
D)

```
Ln#
 1  `timescale 1ns/1ns
 2  module BS_4bit_TB();
 3          logic [3:0]A=0111;
 4          logic [1:0]s=00;
 5          wire [3:0] w;
 6
 7          BS_4bit BS4bit(s , A , w);
 8
 9          initial begin
10          #80 s[0]=1;
11          #80 A[3]=1;
12          #80 A[0]=0;
13          #80 s[0]=1;
14          #80 A[1]=0;
15          #80 A[2]=1;
16          #80 s[1]=1;
17          #80 A[0]=1;
18          #80 s[0]=0;
19
20          #80 $stop;
21          end
22
23  endmodule
```



E)



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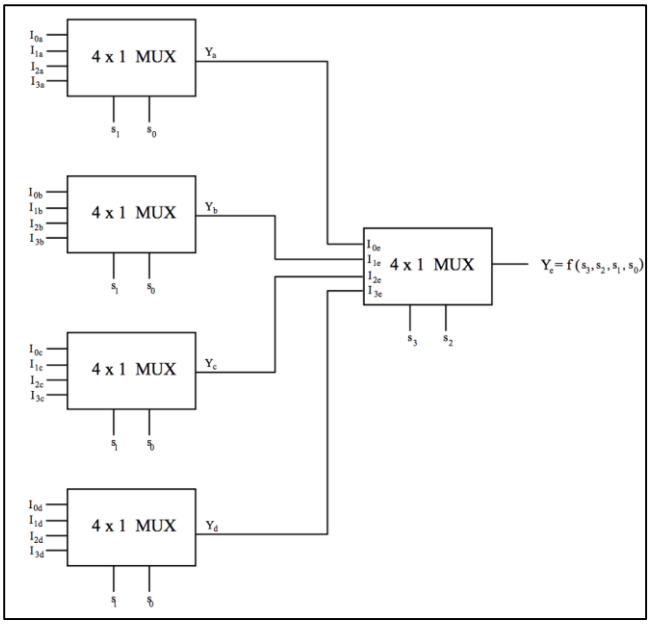
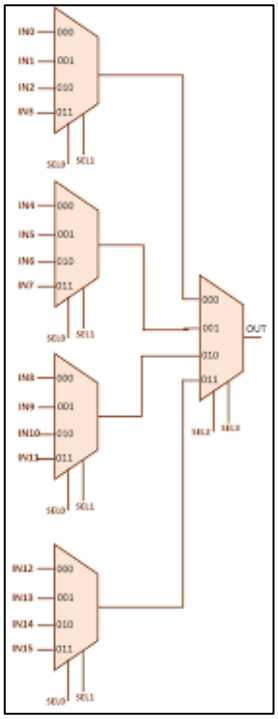
Question 3

A)





B) multiplexers delays are: (32, 28)

If s0=s1=s2=s3=1, then the output is set to the fifteenth output. By changing in15 from 0 to 1 the total delay will be 2 to 1 delays: 2 * 32 = 64

By going from s0=s1=s2=s3=in15=1 to in15=0 we will have two to 0 delays: 2 * 28 = 56

Worst case delay: To 0 = 64, T0 1 = 56

C)

```
Ln#
 1   `timescale 1ns/1ns
 2   module MUX16to1(A, s, w);
 3
 4           input [15:0] A;
 5           input [3:0] s;
 6           output w;
 7           wire y1, y2, y3, y4;
 8
 9           MUX4to1 mux1(A[0], A[1], A[2],  A[3], s[0], s[1], y1),
10                   mux2(A[4], A[5], A[6],  A[7], s[0], s[1], y2),
11                   mux3(A[8], A[9],A[10], A[11], s[0], s[1], y3),
12                   mux4(A[12],A[13],A[14],A[15], s[0], s[1], y4),
13                   mux5(y1, y2, y3, y4, s[2], s[3], w);
14
15  endmodule
```

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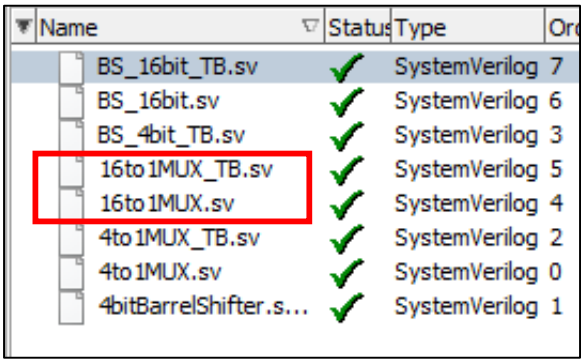
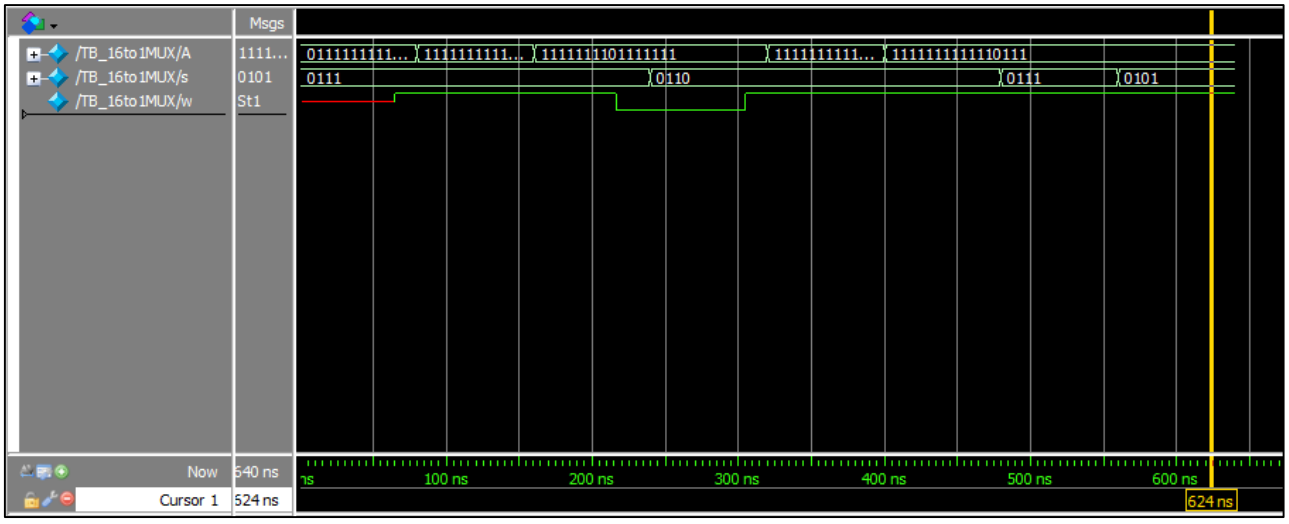
```
Ln#
 1  `timescale 1ns/1ns
 2  module TB_16to1MUX();
 3
 4          logic [15:0]A= 'b0111111111111111;
 5          logic [3:0]s=1111;
 6          wire w;
 7
 8          MUX16to1 mux(A, s, w);
 9
10          initial begin
11          #80 A[15]=1;
12          #80 A[7]=0;
13          #80 s[0]=0;
14          #80 A[7]=1;
15          #80 A[3]=0;
16          #80 s[0]=1;
17          #80 s[1]=0;
18
19          #80 $stop;
20          end
21
22  endmodule
23
```

D)



E)



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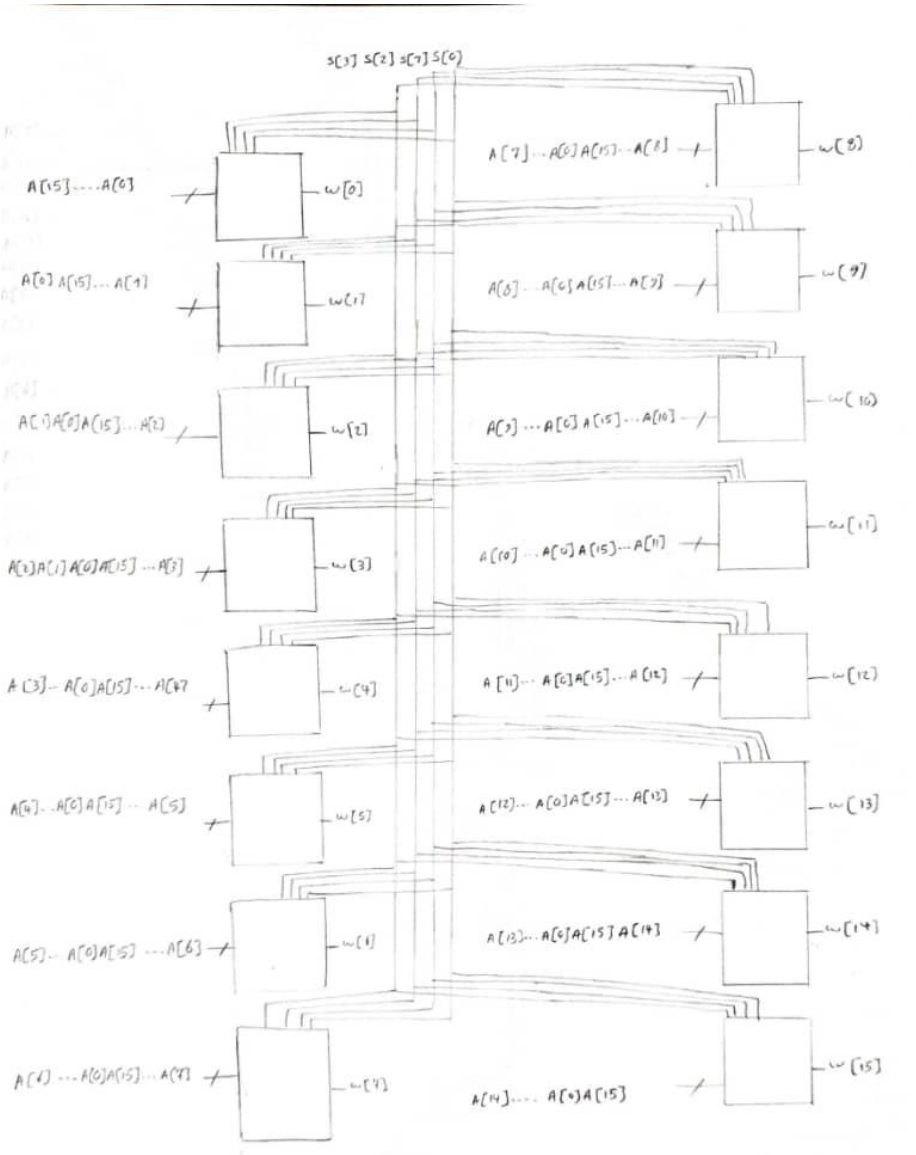
Question 4

A)



B)

16 16-to-1 multiplexers operate simultaneously, therefore the worst case delay is equal to to-1 delay of multiplexer: 64

C)

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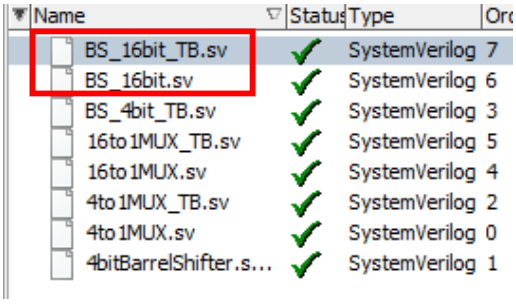
```
Ln#
 1  `timescale 1ns/1ns
 2  module BS_16bit(input [15:0] A, [3:0] s, output [15:0] w);
 3
 4          MUX16to1 mux1(A[15:0], s, w[0]),
 5                   mux2({A[0], A[15:1]}, s, w[1]),
 6                   mux3({A[1:0], A[15:2]}, s, w[2]),
 7                   mux4({A[2:0], A[15:3]}, s, w[3]),
 8                   mux5({A[3:0], A[15:4]}, s, w[4]),
 9                   mux6({A[4:0], A[15:5]}, s, w[5]),
10                   mux7({A[5:0], A[15:6]}, s, w[6]),
11                   mux8({A[6:0], A[15:7]}, s, w[7]),
12                   mux9({A[7:0], A[15:8]}, s, w[8]),
13                   mux10({A[8:0], A[15:9]}, s, w[9]),
14                   mux11({A[9:0], A[15:10]}, s, w[10]),
15                   mux12({A[10:0], A[15:11]}, s, w[11]),
16                   mux13({A[11:0], A[15:12]}, s, w[12]),
17                   mux14({A[12:0], A[15:13]}, s, w[13]),
18                   mux15({A[13:0], A[15:14]}, s, w[14]),
19                   mux16({A[14:0], A[15]}, s, w[15]);
20
21 endmodule
22
```

```
Ln#
 1  `timescale 1ns/1ns
 2  module BS_16bit_TB();
 3
 4          logic [15:0]A= 'b1111111111111110;
 5          logic [3:0]s=1111;
 6          wire [15:0]w;
 7
 8          BS_16bit bs(A, s, w);
 9
10          initial begin
11          #80 A[0]=1;
12          #80 A[7]=0;
13          #80 s[0]=0;
14          #80 A[7]=1;
15          #80 A[3]=0;
16          #80 s[0]=1;
17          #80 s[1]=0;
18
19          #80 $stop;
20          end
21
22 endmodule
23
```

D)



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E)