EE214 Experiment 1 Report

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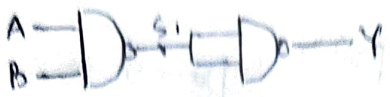
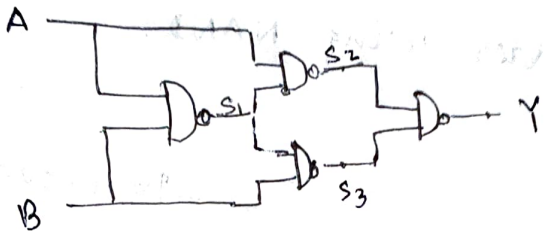
1(a) Design of AND Using NAND.



$S_1 = \overline{(A.B)}$

$Y = \overline{(S_1.S_1)} = \bar{S}_1 = A.B$

1(b) Design of XOR using NAND.



$S_1 = \overline{(A.B)} = \bar{A}+\bar{B}$

$S_2 = \overline{(A.(\bar{A}+\bar{B}))}$

$= \overline{(A\bar{B})} = \bar{A}+B$

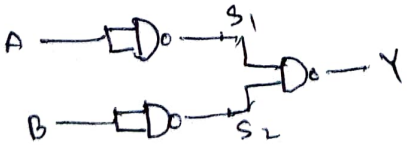
$S_3 = \overline{((\bar{A}+\bar{B}).B)} = \overline{(\bar{A}.B)} = A+\bar{B}$

$Y = \overline{(S_2.S_3)} = \overline{(\bar{A}+B).(A+\bar{B})}$

$= \overline{(\bar{A}+B)} + \overline{(A+\bar{B})}$

$= A\bar{B} + \bar{A}.B$

1(c) Design of OR gate using NAND.

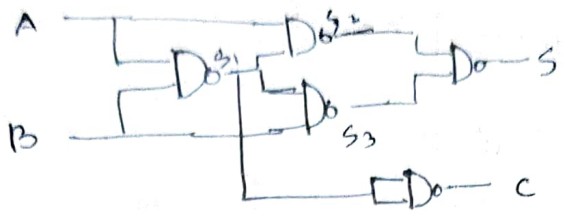


$S_1 = \overline{(A.A)} = \bar{A}$

$S_2 = \overline{(B.B)} = \bar{B}$

$Y = \overline{(S_1.S_2)} = \overline{(\bar{A}.\bar{B})} = A+B$

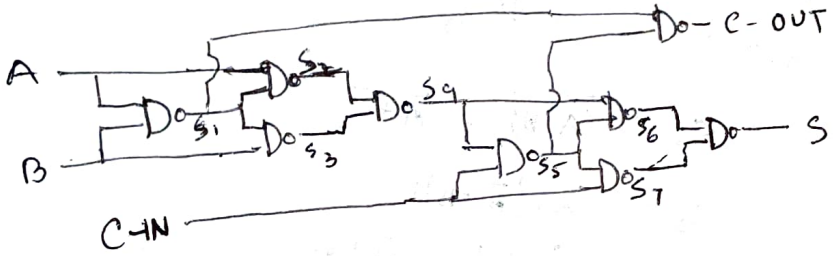
2. (a) Half Adder using NAND



$S = A \oplus B$ (XOR gate as designed before)

$C = \overline{(\overline{A.B})} = A.B$

(b) Full Adder using NAND



$S = A \oplus B \oplus (C\text{-}IN)$

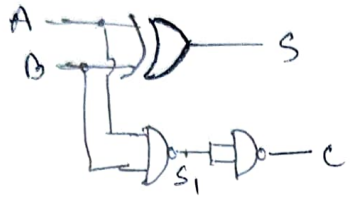
~~$C\text{-}OUT = \overline{(A.B).C + (A.B).(C\text{-}IN)}$~~ ✗

~~$= (A.B) + C\text{-}IN$~~

$C\text{-}OUT = \overline{\left(\overline{(A.B)}.\overline{(C\text{-}IN.(A \oplus B))}\right)}$

$= A.B + (C\text{-}IN).(A \oplus B)$

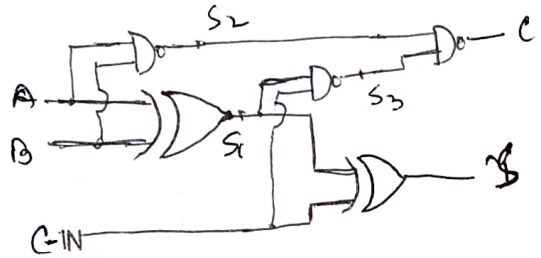
3. (a) Usage of XOR designed & before ~~to use~~ along with NAND for half adder.



$S = A \oplus B$

$C = \overline{(\overline{A \cdot B})} = A \cdot B$

(b) Using XOR designed before ~~to use~~ along with NAND for full adder.



$C = A \cdot B + C\text{-}IN \cdot (A \oplus B)$

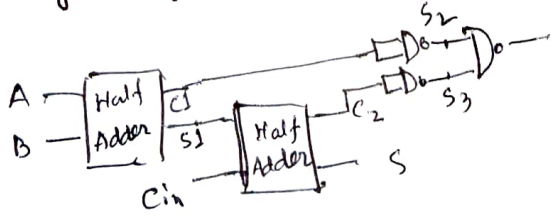
$= \overline{(\overline{A \cdot B}) \cdot (\overline{C\text{-}IN \cdot (A+B)})}$

$S = A \oplus B \oplus C\text{-}IN$

$C = \overline{\left(\overline{(A \cdot B)} \cdot \overline{(C\text{-}IN \cdot (A \oplus B))}\right)}$

$= A \cdot B + C\text{-}IN \cdot (A \oplus B)$

Using half-adder.



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Full Adder Circuit

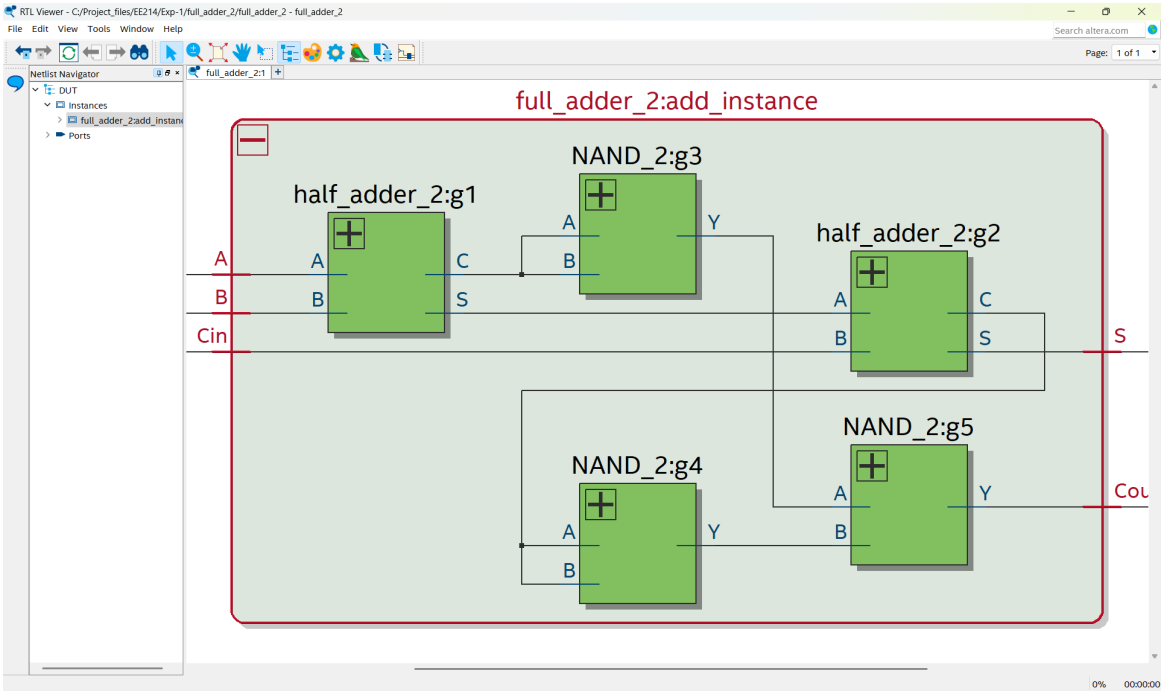

Figure 1: Full Adder Netlist

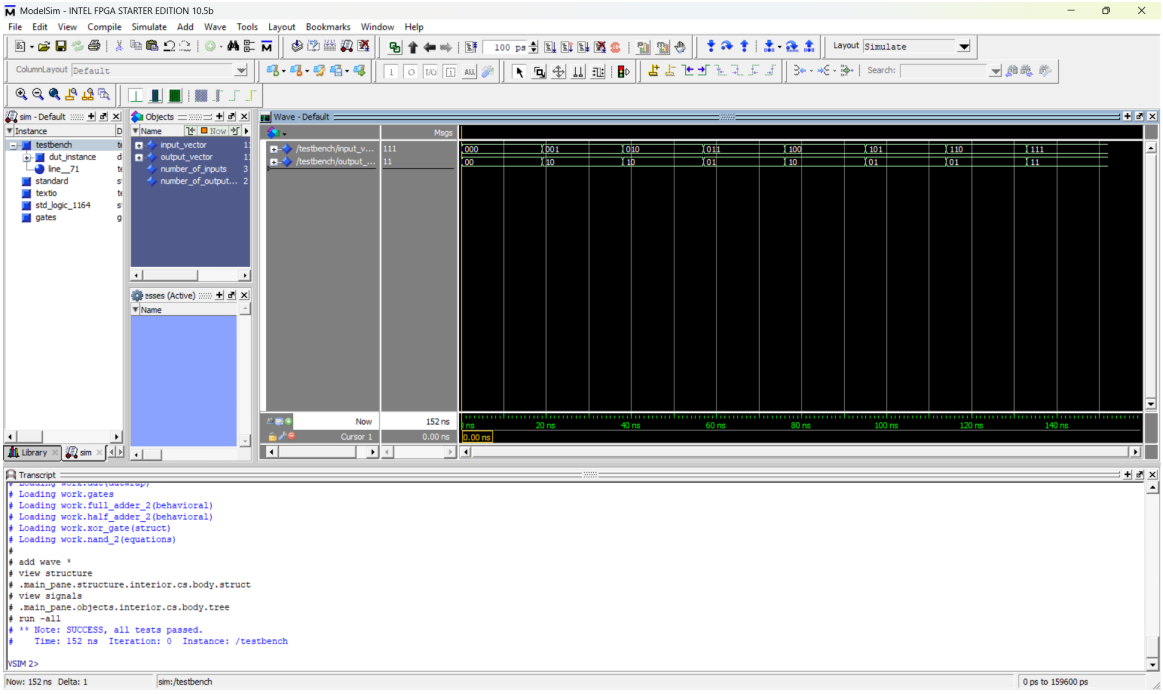

Figure 2: Full Adder Simulation

Half Adder Circuit

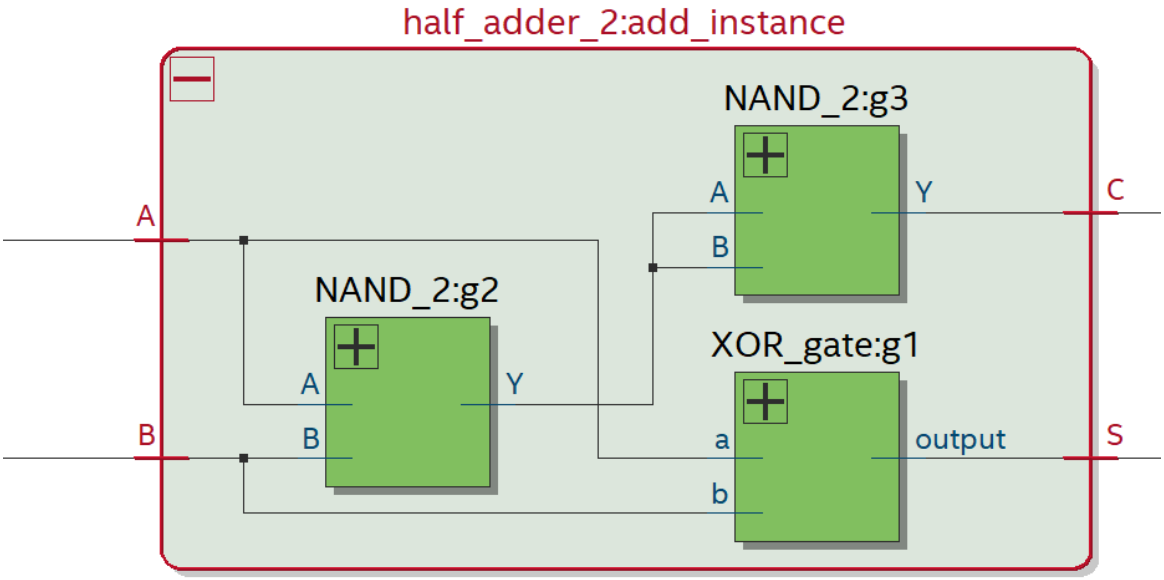

Figure 3: Half Adder Netlist

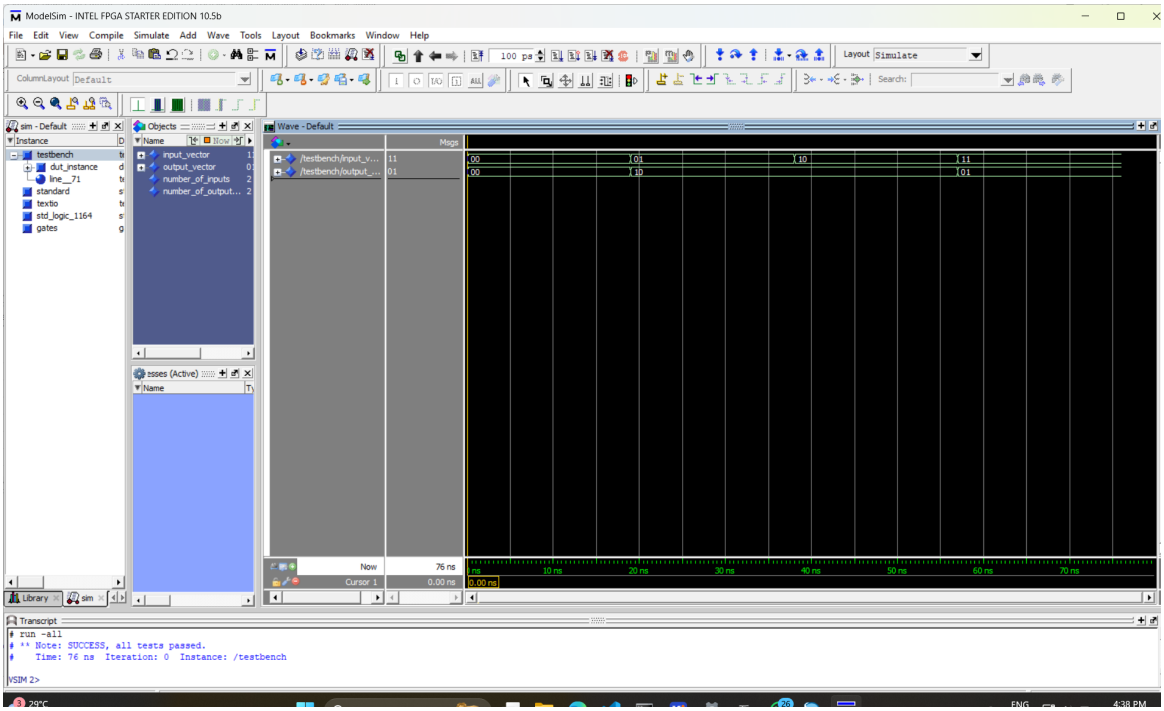

Figure 4: Half Adder Simulation

NAND-based AND Gate

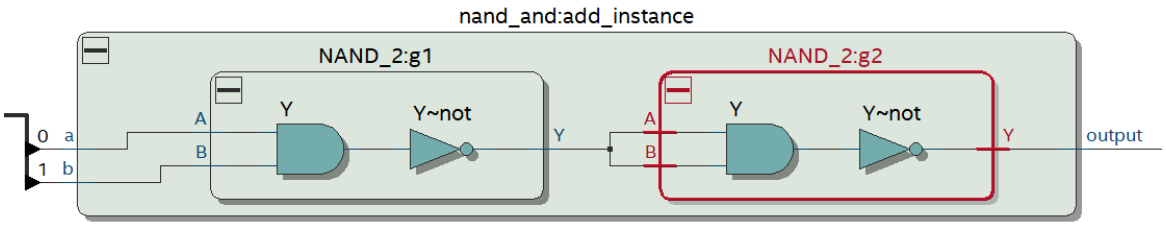

Figure 5: NAND-based AND Gate Netlist

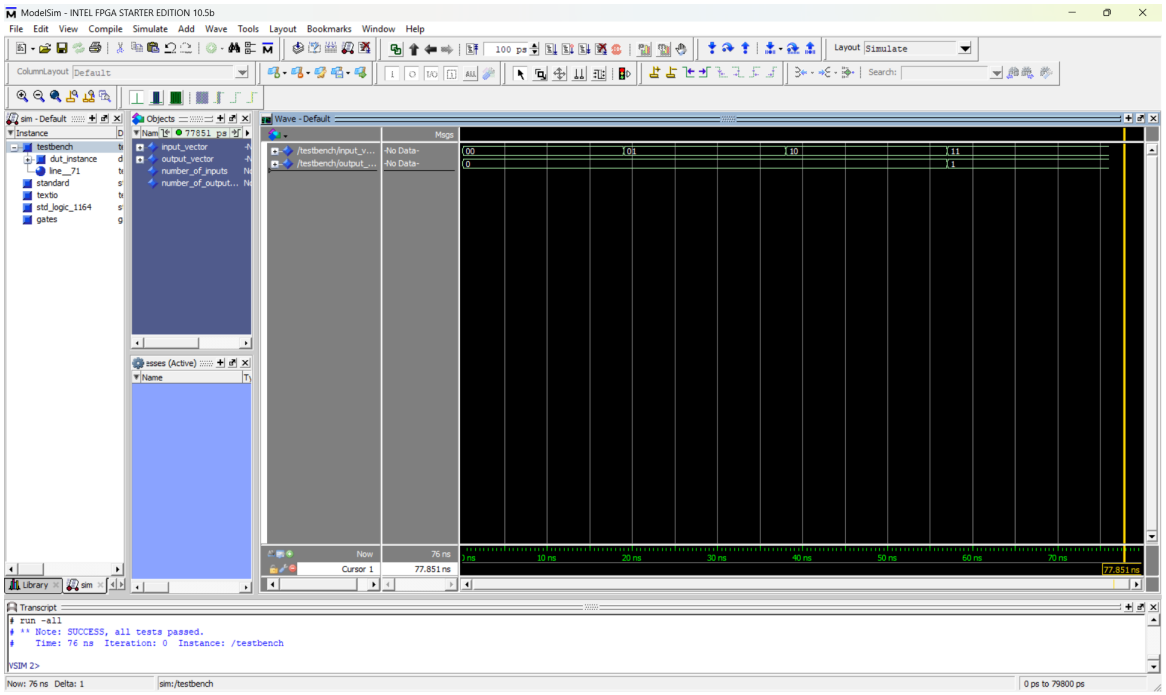

Figure 6: NAND-based AND Gate Simulation

NAND-based OR Gate

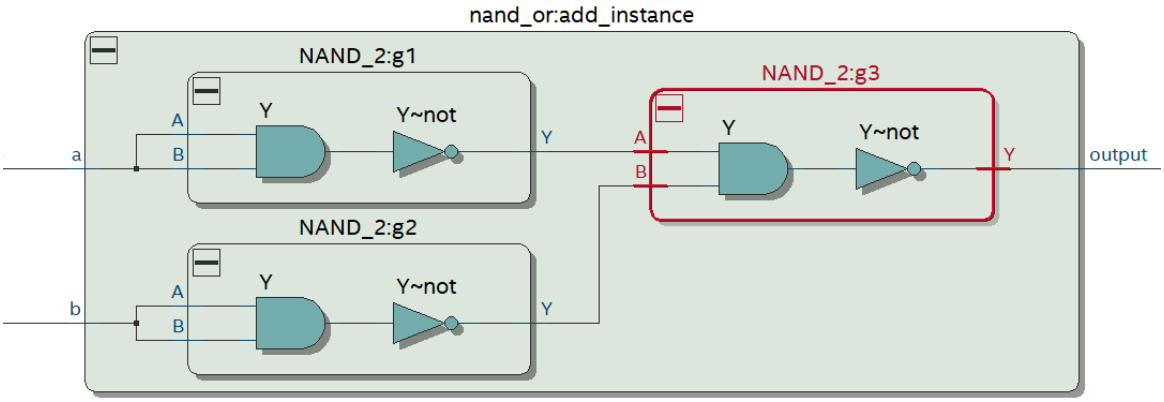

Figure 7: NAND-based OR Gate Netlist

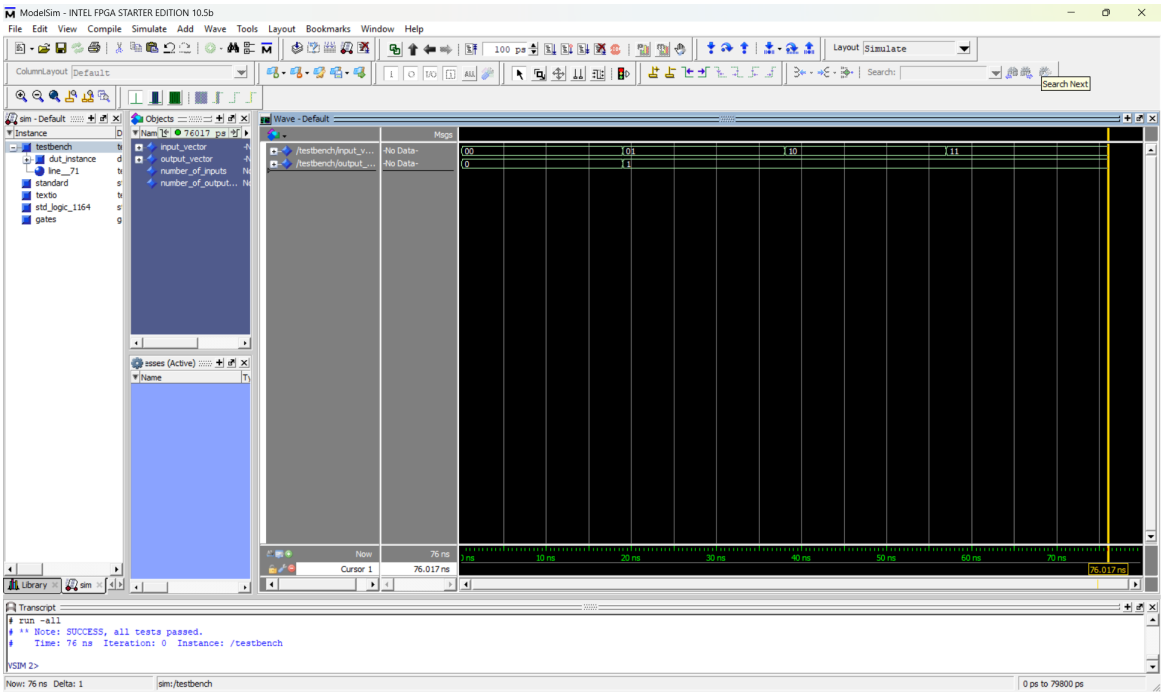

Figure 8: NAND-based OR Gate Simulation

NAND-based XOR Gate

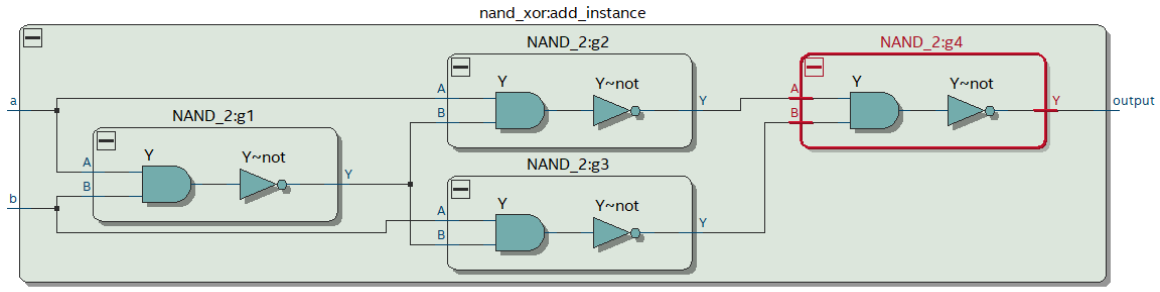

Figure 9: NAND-based XOR Gate Netlist

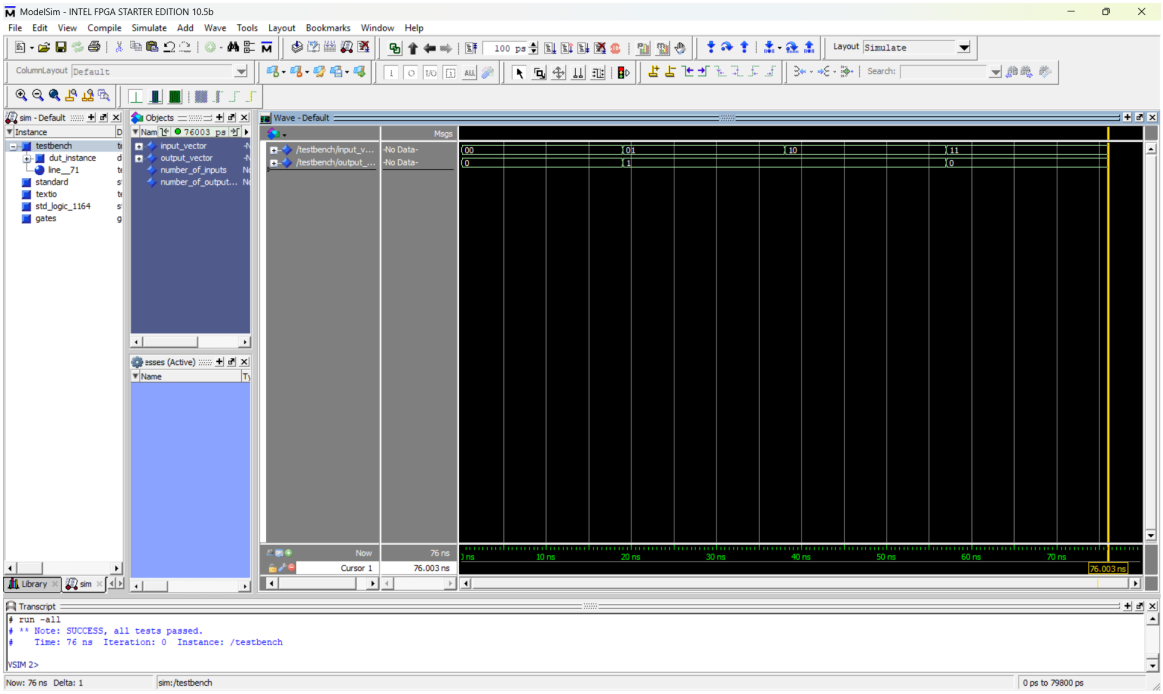

Figure 10: NAND-based XOR Gate Simulation