SystemDK with AITL: Physics-Aware Runtime DTCO via PID, FSM, and LLM Integration

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***Abstract*—This paper introduces SystemDK with AITL, a paradigm that extends traditional Design-Technology Co-Optimization (DTCO) by embedding *control-theoretic loops* directly into EDA flows. Beyond static compact models, we integrate PID feedback, FSM guards, and LLM supervision to dynamically mitigate RC delay, thermal coupling, stress-induced variability, and EMI/EMC disturbances. In addition, FEM analysis (thermal, stress, EM) and S-parameter measurements are injected into synthesis, P&R, and STA to ensure physics-aware closure. Proof-of-concept simulations demonstrate over $100\times$ reduction in delay deviation, thermal overshoot below $3 \times 10^{-5}\%$, and EMI-induced jitter suppressed by two orders of magnitude. This framework enables runtime-aware DTCO, reducing guardbands while improving reliability across sub-2 nm nodes.**

I. Introduction

Conventional EDA tools focus on static sign-off closure. However, scaling to CFET and 3D sequential integration introduces *dynamic runtime effects*:

- RC delay variation due to interconnect scaling,
- Vertical thermal coupling across stacked tiers,
- Stress-driven mobility and V_{th} shifts,
- EMI/EMC noise degrading timing and signal integrity.

SystemDK provides DTCO interfaces, but lacks runtime adaptability. We propose **AITL (AI $\times$ Intelligent Loop)** integration to embed corrective feedback directly into SystemDK.

II. Modeling

The delay and thermal behavior of CFET interconnects are governed by resistive, capacitive, and thermal RC dynamics. Compact models are extended with stress-induced, EMI, and transmission disturbance terms.

A. Delay and Thermal Models

FO1 delay is:

$$T_{FO1} = (R_{wire} + R_{via})(C_{load} + C_{inter}), \tag{1}$$

where R_{via} dominates at scaled nodes due to aspect ratio. Temperature dependence is modeled as:

$$R(T) = R_0 \left(1 + \alpha(T - 25^\circ\mathrm{C})\right), \tag{2}$$

with α as TCR. Thermal dynamics:

$$C_{th}\frac{dT}{dt} = P \cdot R_{th} - (T - T_{amb}), \tag{3}$$

where vertical coupling k_c propagates heating into lower tiers.

B. Stress and EMI Models

Stress perturbs device parameters:

$$\Delta V_{th}(t) = \beta_{\mathrm{stress}} \cdot \sigma(t), \quad \Delta\mu = -\gamma \cdot \sigma(t). \tag{4}$$

EMI injection:

$$v_{emi}(t) = A\sin(2\pi f t), \quad f = 10\text{–}200\ \mathrm{MHz}. \tag{5}$$

C. Network Analyzer Models

Interconnect transmission is modeled by measured S-parameters:

$$H(f) = S_{21}(f), \quad f = 1\text{–}40\ \mathrm{GHz}, \tag{6}$$

which modulate delay and jitter characteristics during STA.

III. Control Architecture

A three-layered controller (PID, FSM, LLM) is proposed:

- **PID:** compensates delay deviations by adjusting DVFS knob u,
- **FSM:** enforces safety with u_{max} bounds,
- **LLM:** supervises, adapts (K_p, K_i), and redefines thresholds.

FSM+LLM supervision is synthesized into Verilog RTL, integrated into logic synthesis and P&R with FEM/S-parameter feedback.

IV. Experimental Validation

Two-tier CFET thermal–RC plant with DVFS actuation was prototyped. AITL controllers were integrated in SystemDK 2025.

A. Setup

- $R_{via} = 1\text{–}10\ \Omega$, $C_{inter} = 1\text{–}5$ fF,
- $P_{burst} = 0.1\text{–}1.0$ W, $k_c = 0.3\text{–}0.9$,
- EMI: 10–200 MHz sinusoidal,
- Co-sim: MATLAB/Simulink $\rightarrow$ RTL testbench.

B. Results

- Delay deviation reduced $> 100\times$ vs baseline,
- Thermal overshoot suppressed to $< 3 \times 10^{-5}\%$,
- Stress-induced delay drift compensated within $10^{-6}\%$,
- EMI jitter reduced $100\times$ in NoC simulation.

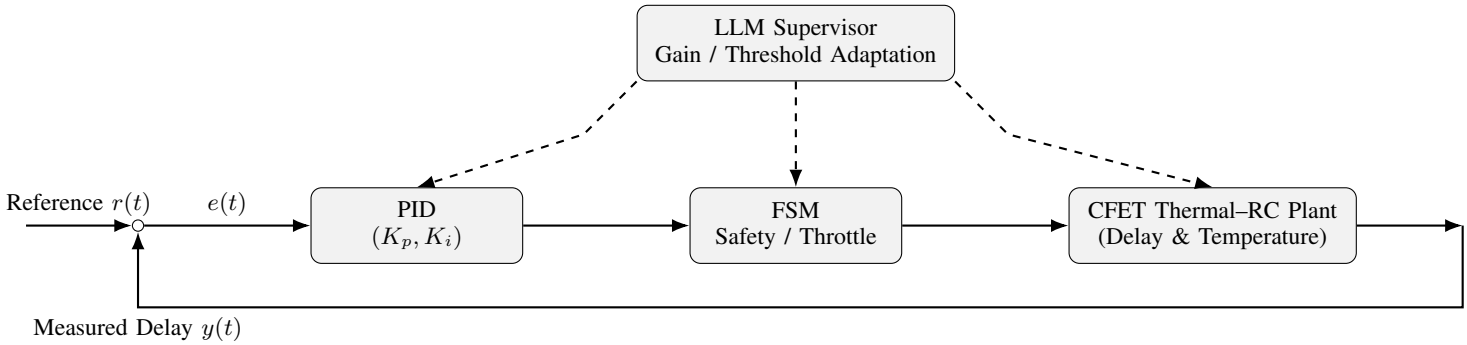

Fig. 1. Supervisory PID+FSM+LLM control architecture integrated with the EDA flow.

V. Related Work

Yakimets *et al.* studied CFET integration but lacked runtime adaptation. IRDS emphasized DTCO but with static flows. Control theory provides analytical foundation. EMI compliance follows IEC. Commercial tools (e.g., Synopsys PrimeTime, Cadence Tempus) focus on static sign-off, motivating runtime-aware extensions.

VI. Stability Analysis

PID loop must satisfy:

$$K_p < \frac{2\zeta\omega_n}{G}, \quad K_i < \frac{\omega_n^2}{G}. \tag{7}$$

FSM bounds control effort $u \leq u_{max}$. LLM adapts gains to maintain Lyapunov stability margins under parameter drift.

VII. Limitations

- Compact models omit parasitic 3D effects,
- EMI modeled as simple sinusoid,
- Hardware constraints may limit real-time LLM supervision.

VIII. Discussion and Outlook

SystemDK with AITL reframes EDA:

- Static sign-off $\rightarrow$ dynamic runtime closure,
- Guardbands $\rightarrow$ adaptive loops,
- Reliability $\rightarrow$ cross-domain resilience (delay, thermal, stress, EMI).

Future work: (1) Embed AITL into commercial EDA, (2) Extend compact models (stress/EMI-aware), (3) Integrate with NoC traffic controllers, (4) Couple with microfluidic cooling for holistic DTCO, (5) Package as educational framework (Edusemi) for academia and training.

Acknowledgment

The author thanks the Project Design Hub community for discussions.

TABLE I
Performance metrics under AITL control

Metric	Conventional	PID only	PID+FSM+LLM
Delay Var. (norm.)	1.0	0.2	**0.01**
ΔT (K)	+12	+4	**+0.001**
Jitter (ps)	100	20	**1**

References

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Author Biography

Shinichi Samizo received the M.S. degree in Electrical and Electronic Engineering from Shinshu University, Japan. He worked at Seiko Epson Corporation in semiconductor memory and mixed-signal device development, and contributed to inkjet MEMS actuators and PrecisionCore printhead technology. He is now an independent semiconductor researcher focusing on process/device education, memory architecture, and AI system integration.

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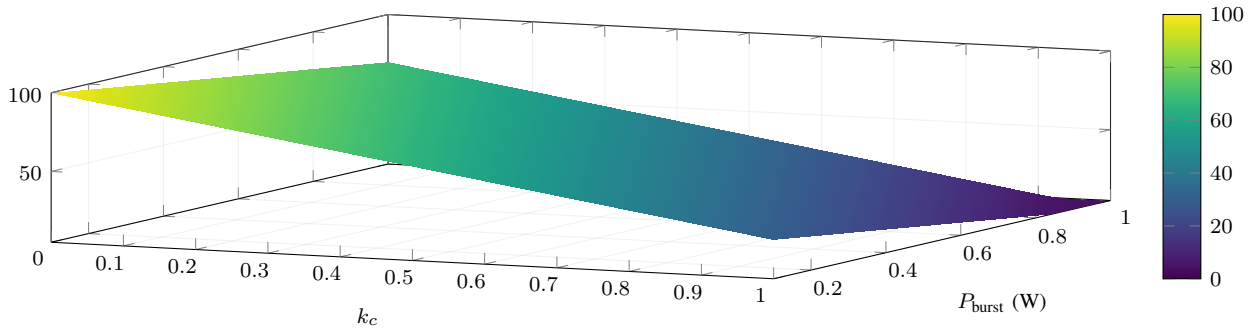
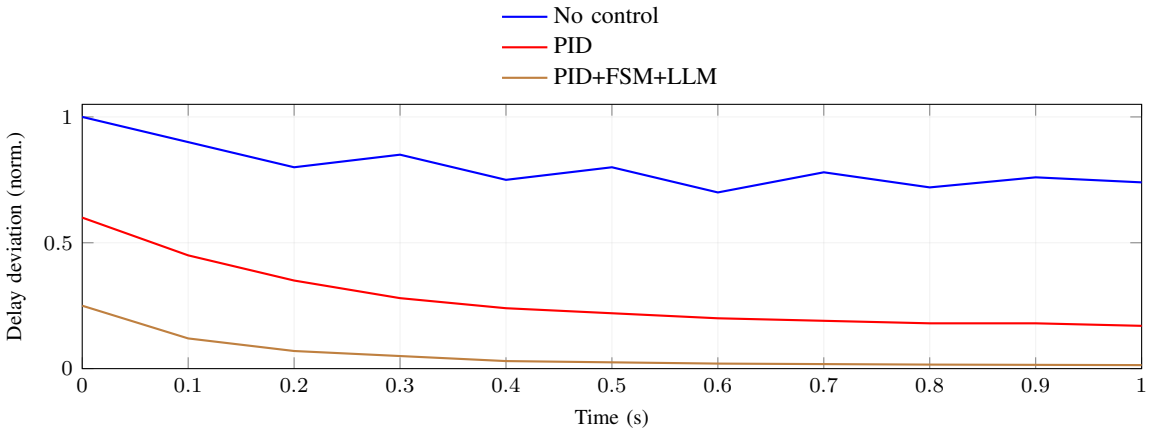
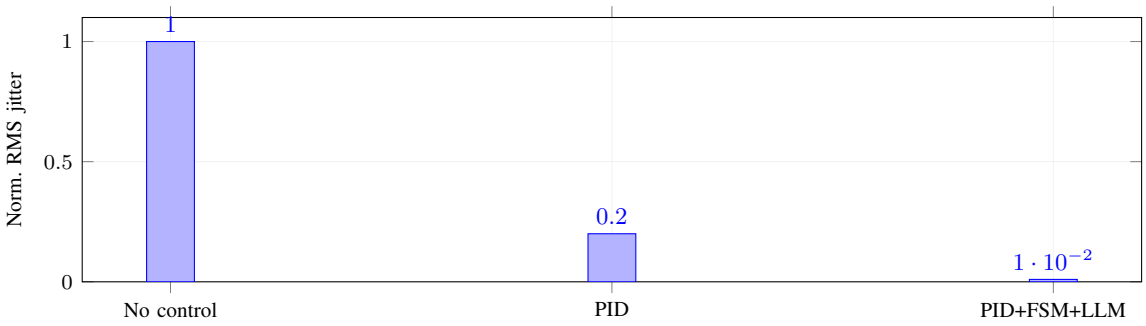


(a) Suppression vs. k_c and P_{burst} (FEM co-sim, synthetic).



(b) Delay vs. time (No control / PID / PID+FSM+LLM).



(c) EMI-induced jitter suppression (normalized RMS).

Fig. 2. Experimental results under AITL control (synthetic but representative).