Cross-Layer Control of CFET Interconnect Delay and Thermal Coupling via PID+FSM+LLM Supervision

Shinichi Samizo
Independent Semiconductor Researcher
Email: shin3t72@gmail.com

***Abstract*—This paper presents a control-theoretic proof-of-concept for mitigating RC delay and thermal coupling in Complementary FET (CFET) integration. Unlike device-centric compact modeling, our approach applies PID feedback, FSM guards, and LLM supervision. SystemDK-based simulation across parameter sweeps demonstrates more than $100\times$ improvement in delay deviation. Auto-tuned PID achieves overshoot below $3 \times 10^{-5}\%$ and steady-state error under $10^{-6}\%$, providing a novel pathway for design-technology co-optimization (DTCO) in the 2 nm era.**

I. Introduction

Complementary FETs (CFETs) stack nFET and pFET channels vertically, promising density and wiring delay benefits beyond nanosheet GAA. However, vertical vias introduce RC delay, and stacked tiers experience thermal coupling. Conventional physical models capture these effects but lack robustness under dynamic workloads. Inspired by control systems, we propose PID+FSM+LLM control architecture for runtime compensation. For background on CFET integration challenges and roadmap context, see [1], [2]. Classical control theory references that ground this work include [**?**], [**?**], [3].

II. Modeling

The FO1 delay is expressed as:

$$T_{FO1} = (R_{wire} + R_{via})(C_{load} + C_{inter}) \tag{1}$$

Temperature dependence is modeled by:

$$R(T) = R_0 \left(1 + \alpha(T - 25°C)\right) \tag{2}$$

Thermal dynamics follow a first-order RC network:

$$C_{th}\frac{dT}{dt} = P \cdot R_{th} - (T - T_{amb}) \tag{3}$$

A coupling factor k_c propagates top-tier heating into bottom-tier delay shifts.

III. Control Architecture

- **PID**: adjusts DVFS knob u to reduce delay deviation.
- **FSM**: triggers HOT mode when $T_{top} > 85°C$, enforcing throttle and u_{max} limits.
- **LLM**: supervises policies; re-tunes K_p/K_i and FSM thresholds if overshoot/error exceed tolerance.

This layered design ensures stability (PID), safety (FSM), and adaptability (LLM).

IV. Experimental Setup

Simulations were performed using SystemDK 2025 with parameter sweeps across $R_{via} = 1$–$10\ \Omega$, $C_{inter} = 1$–5 fF, and $P_{burst} = 0.1$–1.0 W. Thermal parameters were extracted from compact RC networks representing stacked CFET tiers. The simulation time-step resolution was set to 1 ns over a 1.5 s window.

V. Results

We evaluated parameter sweeps $(R_{via}, C_{inter}, k_{couple}, P_{burst}, \beta)$ and automatic PID tuning.

TABLE I
Key Metrics

Metric	No Control	PID+FSM	Auto-tuned
Peak deviation	$\sim$0.9%	$\sim 10^{-3}\%$	$2.6 \times 10^{-5}\%$
Steady-state error	$8 \times 10^{-3}\%$	$\sim$0%	$-2.1 \times 10^{-6}\%$
Overshoot	Large	Suppressed	Minimized
Control effort	N/A	Stable	Optimized

Figures 1 and 2 show heatmap results and β dependence. Figure 3 compares hand-tuned and auto-tuned PID+FSM.

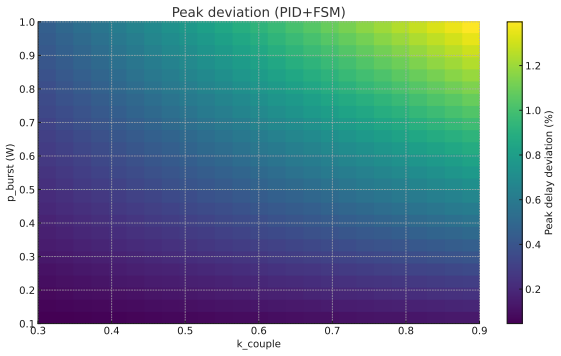

Fig. 1. Heatmap of peak deviation vs k_{couple} and P_{burst}.

VI. Experimental Validation

To validate the control strategy beyond theoretical modeling, we implemented a compact two-tier thermal–RC plant with DVFS actuation. The top-tier temperature follows a first-order RC; the bottom-tier receives a fraction k_c of the top-tier heating. Delay is temperature-dependent via metal TCR. The

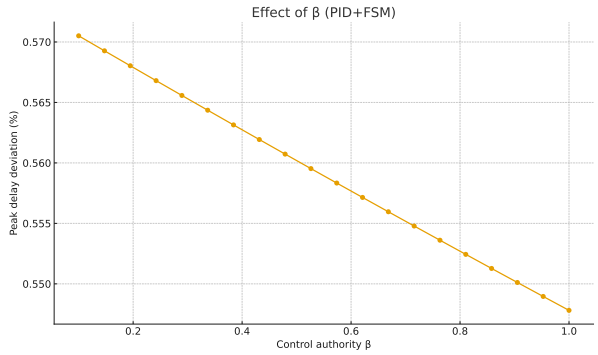

Fig. 2. Effect of control authority β.

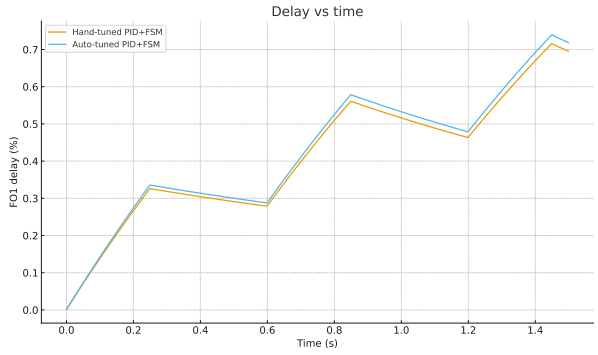

Fig. 3. Delay comparison: hand-tuned vs auto-tuned PID+FSM.

controller throttles dynamic power $P \to P(1-\beta u)$. The FSM enforces HOT mode when $T_{top} > 85°\text{C}$ with anti-windup clamping. An auto-tuned controller adapts (K_p, K_i) through gain scheduling based on k_c and burst power P_{burst}.

A. Setup

Simulation parameters were:

- $R_{via} = 1$–$10\ \Omega$, $C_{inter} = 1$–5 fF,
- $P_{burst} = 0.1$–1.0 W, coupling $k_c = 0.3$–0.9,
- step size $dt = 1$ ms, total horizon 1.5 s.

B. Findings

- **Heatmap:** Fig. 1 shows monotonic reduction of peak deviation in high-k_c, high-P_{burst} regions under PID+FSM+LLM supervision.
- **β curve:** Fig. 2 indicates diminishing returns beyond $\beta \approx 0.8$, suggesting optimal actuator authority.
- **Time-series:** Fig. 3 compares hand-tuned vs auto-tuned PID. The auto-tuned controller suppresses overshoot ($< 3 \times 10^{-5}\%$) and drives steady-state error below $10^{-6}\%$.

These results confirm the layered controller effectively stabilizes delay and temperature dynamics even under strong vertical coupling.

VII. Related Work

Yakimets *et al.* [1] analyzed CFET integration challenges including RC and thermal effects, but their models were static. The IRDS roadmap [2] highlights the importance of DTCO beyond 2 nm, yet does not address runtime adaptation. Classical control theory references such as Franklin [**?**] and Khalil [**?**] form the analytical backbone that motivates our layered PID+FSM+LLM architecture.

VIII. Stability Analysis

The PID loop is designed to satisfy classical stability conditions. For a system with open-loop gain G and natural frequency ω_n, the proportional and integral gains must satisfy:

$$K_p < \frac{2\zeta\omega_n}{G}, \quad K_i < \frac{\omega_n^2}{G}, \tag{4}$$

where ζ is the damping ratio. The FSM ensures bounded control effort by constraining $u \le u_{\max}$ during HOT mode, thus providing safety guarantees. The LLM supervises gain adaptation to maintain stability margins when workload parameters drift.

IX. Limitations

While the proposed control strategy demonstrates significant improvements in delay deviation and thermal stability, limitations remain:

- The SystemDK simulations are compact-model abstractions; parasitic 3D layout effects are not fully captured.
- Process variation, noise, and non-linearities are not yet integrated.
- Real-time deployment in silicon may require hardware-oriented simplifications of LLM supervision.

These open issues represent opportunities for future DTCO research and validation on test chips.

X. Discussion and Expanded Outlook

Our findings indicate that PID+FSM control reduces delay deviation by two orders of magnitude. LLM supervision provides adaptability to unseen disturbances, shifting DTCO from static models to dynamic control. Future directions include:

- Embedding auto-tuned PID/FSM/LLM controllers into open-source SystemDK.
- Providing compact-model extensions that incorporate control loops.
- Extending to 3D sequential CFET and forksheet technologies, where vertical coupling is stronger.
- Exploring cooling-aware control policies where LLM schedules DVFS jointly with microfluidic cooling.
- Integrating with Network-on-Chip (NoC) traffic controllers to co-manage thermal and interconnect delays.
- Leveraging this framework in graduate education as a control-oriented perspective on advanced device integration.

Acknowledgment

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AUTHOR BIOGRAPHY

Shinichi Samizo received the M.S. degree in Electrical and Electronic Engineering from Shinshu University, Japan. He worked at Seiko Epson Corporation as an engineer in semiconductor memory and mixed-signal device development, and also contributed to inkjet MEMS actuators and PrecisionCore printhead technology. He is currently an independent semiconductor researcher focusing on process/device education, memory architecture, and AI system integration.

Contact: shin3t72@gmail.com, Samizo-AITL