Historical Case Study on Ti Silicide ($TiSi_2$) Reliability Issues in Mixed-Voltage CMOS Driver ICs

Shinichi Samizo
Independent Semiconductor Researcher
Project Design Hub, Samizo-AITL
Email: shin3t72@gmail.com GitHub: Samizo-AITL

Abstract—This paper analyzes a historical failure case at the 0.25 µm CMOS node related to Ti silicide ($TiSi_2$) phase-transition instability. For active-matrix TFT (aTFT) LCD driver ICs that required mixed 3.3 V logic and ∼30 V high-voltage (HV) devices, manufacturers selected the 0.25 µm process because its LOCOS isolation safely supported HV co-integration. By contrast, the 0.18 µm STI-based node, although denser and yield-stable, posed edge-thinning risks for ∼30 V devices and required a new HV platform. Under this context, incomplete C49→C54 transformation with boron absorption created localized high-resistance spots, directly reducing 1 Mbit SRAM yield. The study highlights how process optimization and empirical feedback cycles were indispensable when isolation technology and device requirements constrained node selection.

I. Introduction

In the late 1990s, LCD driver ICs for passive monochrome panels were commonly fabricated in 0.35 µm processes supporting 3.3 V logic and 40 V HV devices. With the transition to active-matrix TFT (aTFT) LCD panels in the early 2000s, driver ICs required higher-performance logic, embedded large SRAM macros, and continued HV integration around 30 V.

Although the 0.18 µm CMOS process was already in mass production with small die size and stable yield, it relied on Shallow Trench Isolation (STI), where edge thinning introduced a reliability risk for ∼30 V devices. By contrast, the 0.25 µm process used Local Oxidation of Silicon (LOCOS), which had a proven track record for HV isolation. Therefore, manufacturers adopted the 0.25 µm LOCOS-based process for 3.3 V + 30 V LCD driver ICs, accepting area disadvantages to guarantee HV compatibility.

II. Technical Background

A. Isolation Choice for HV Devices

- 0.25 µm LOCOS: Mature, thick field oxide with well-established margins for ∼30 V HV device integration.
- 0.18 µm STI: Provided density and yield benefits, but corner thinning at the trench edge raised leakage and breakdown concerns for HV devices, necessitating a new HV device platform.

B. Ti Silicide Instability

$TiSi_2$ was widely adopted for its low resistivity. However, it undergoes a phase transformation from metastable C49 to stable C54 during rapid thermal annealing (RTA). If the transformation remains incomplete, residual C49 grains act as high-resistance spots. Boron absorption from halo implants into Ti further aggravated resistivity variation. While these effects were tolerable in smaller SRAM macros (e.g., 500 kbit), they became fatal when scaled to 1 Mbit capacity.

III. Failure Analysis

A. Observation: 1 Mbit SRAM

In mass production, random single-bit failures appeared in the 1 Mbit SRAM macro. Since redundancy was not implemented in the embedded macro, even a single defective bit caused rejection of the entire device.

B. Redundancy Limitation in Embedded Macros

In stand-alone memory products, redundancy circuits are standard practice and defective cells can be repaired during testing via laser trimming. In embedded memory macros, however, redundancy is generally excluded due to design complexity, timing, and area overhead. Additionally, LCD driver ICs were typically tested on mixed-signal/SoC testers, which lacked built-in support for redundancy repair. Therefore, redundancy was not adopted, and scaling to 1 Mbit carried critical reliability risk.

C. Root Cause

Failure localization confirmed that:

- Boron from halo regions diffused into Ti during silicidation.
- Local B uptake inhibited C54 transformation, leaving high-resistance C49 spots.
- These spots manifested as random SRAM bit failures.

D. Review Limitation

Earlier 500 kbit SRAM macro products had not shown this issue. Based on those precedents, engineers assumed that scaling to 1 Mbit would be safe. Consequently,

TABLE I
Comparison of 0.25 µm LOCOS and 0.18 µm STI nodes for LCD driver ICs

	0.25 µm (LOCOS)	0.18 µm (STI)
Isolation method	Thick field oxide (LOCOS); proven HV margin	Shallow trench isolation; edge thinning risk at HV corners
HV device support (at that time)	Existing ∼30 V HV design reusable	New HV platform required (re-qualification)
Die size / density	Larger die, lower density	Smaller die, higher density
Yield stability	Moderate; yield impacted by $TiSi_2$ instability	Generally stable baseline process
Embedded SRAM redundancy	Not implemented (design/area/timing overhead); no laser repair in mixed-signal testers	Same limitation; redundancy/laser repair infeasible in LCD driver IC test flow
Risk at 1 Mbit SRAM	High: localized resistive defects ⇒ chip rejection	Lower base risk, but HV co-integration not yet qualified
Adoption rationale	Safe HV compatibility outweighed cost/density	Density/yield advantage offset by HV risk; not adopted for HV driver products

the failure mode was not identified during the initial development review stage, demonstrating the limitation of relying on past yield experience without revalidation.

IV. Countermeasures

A. Provisional Measures

Etch profiles were tuned to slightly undercut sidewalls. This structural modification increased the physical separation between halo implant regions and the silicide formation area, reducing the probability of boron diffusion into Ti. As a result, localized inhibition of C54 transformation was temporarily suppressed, leading to short-term yield improvement. However, this countermeasure relied on process-window tuning and could not guarantee robustness across all wafer lots.

B. Permanent Measures

RTA conditions were optimized to promote complete transformation to the stable C54 phase. By carefully controlling temperature ramp rate and soak time, the process minimized residual C49 grains. This measure stabilized silicide resistivity, but at the cost of altering transistor series resistance and junction leakage, requiring re-characterization of device models and circuit timing libraries. Thus, the permanent solution involved a trade-off between silicide stability and overall device parameter shifts.

V. Yield Sensitivity Model

The yield impact of redundancy can be approximated by a Poisson model:

$$Y_k = e^{-\lambda} \sum_{i=0}^{k} \frac{\lambda^i}{i!},$$

where λ is the average defect count and k is the redundancy capacity.

VI. Educational Application

A. Teaching Tools

- Cause-effect diagrams: process → defect → yield
- Comparative analysis: 0.25 µm (LOCOS) vs 0.18 µm (STI) for HV devices (Table I)

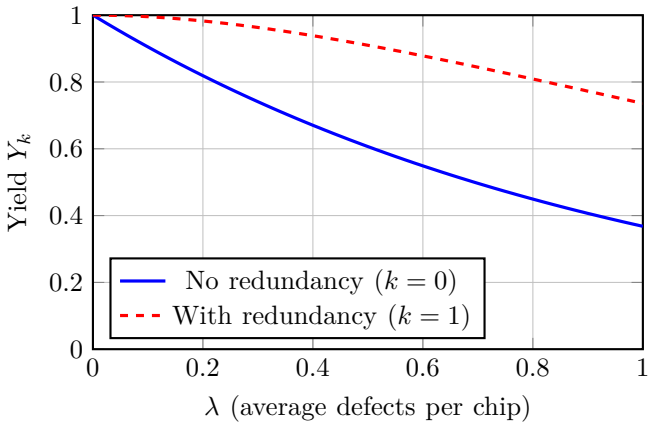

Fig. 1. Illustrative yield sensitivity (Poisson model) with and without redundancy.

- Exercises: prioritize process fix vs. redundancy adoption

B. Lessons

This case shows the risk of extrapolating from small macros (500 kbit) to larger ones (1 Mbit) without reassessing defect sensitivity. It also emphasizes that process-related instability, invisible at smaller scales, can dominate yield once redundancy is unavailable. For embedded SRAM, capacity scaling must always be coupled with explicit yield-risk validation.

VII. Conclusion

This case demonstrates how HV compatibility constraints dominated node selection. Despite the availability of a denser, yield-stable 0.18 µm STI process, the requirement for safe ∼30 V HV integration drove adoption of 0.25 µm LOCOS. Yield loss from incomplete $TiSi_2$ phase transformation (with boron absorption) became critical at the 1 Mbit SRAM scale. The educational value lies in showing how scaling, process technology, and reliability intersect, and why continuous empirical feedback is essential.

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Author Biography

Shinichi Samizo received the M.S. degree in Electrical and Electronic Engineering from Shinshu University, Japan. He worked at Seiko Epson Corporation on semiconductor memory and mixed-signal device development and contributed to inkjet MEMS actuators and PrecisionCore printhead technology. He is currently an independent semiconductor researcher focusing on process/device education, memory architecture, and AI system integration. Contact: shin3t72@gmail.com GitHub: Samizo-AITL.