Educational Perspectives on Complementary FETs (CFET): Evolution Beyond GAA and Open Challenges

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***Abstract*—This tutorial paper provides an educational overview of emerging *Complementary FET (CFET)* technology, which vertically stacks nFET and pFET devices beyond Gate-All-Around (GAA) nanosheets. CFET reframes the CMOS inverter as a *cross-sectional* integration, promising density and delay improvements. We consolidate structure, electrostatic motivations, layout and delay impacts, fabrication challenges, and modeling limitations, and articulate the pedagogical value of CFET as an open, unresolved technology for semiconductor curricula.**

***Index Terms*—CFET, GAA, FinFET, nanosheet FET, short-channel effects, scaling, education, tutorial, vertical stacking, PDK.**

I. Introduction

Scaling has progressed from planar CMOS to FinFET and most recently GAA nanosheet FETs. Beyond the 2 nm node, interconnect delay and cell footprint limit further gains despite excellent electrostatics. CFET stacks nFET and pFET in the vertical dimension so that the cross-section itself constitutes a CMOS inverter, potentially doubling effective standard-cell density while shortening n–p connections. This paper positions CFET as both a roadmap element and an educational vehicle for device–design co-optimization.

II. Device Evolution: From SCE Relief to Cross-Sectional CMOS

A. Planar CMOS and SCE Motivation

As gate lengths entered the deep sub-100 nm regime, planar MOSFETs suffered from short-channel effects (SCE): threshold-voltage roll-off, drain-induced barrier lowering, off-state leakage, and degraded subthreshold slope. Electrostatic control by a single top gate could no longer effectively pinch off the channel.

B. FinFET: Three-Sided Gate Control

FinFETs improved electrostatics by wrapping the gate around *three* sides of a vertical fin. The stronger gate-to-channel coupling sharpened subthreshold slope, reduced variability, and enabled higher drive per footprint by using multiple fins per device. However, the tall/narrow fin introduced process and variability trade-offs and left one side of the channel uncontrolled.

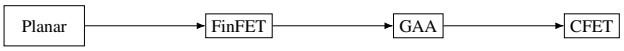

Fig. 1. Device evolution: Planar → FinFET (3-side) → GAA (4-side) → CFET (vertical stack).

C. GAA Nanosheet: Four-Sided Control

Gate-All-Around (GAA) nanosheet FETs extend control to *four* sides by surrounding suspended sheets (or wires) with the gate. This architecture further suppresses SCE and variability and allows continued gate-length scaling [1]. Yet, at advanced nodes the delay/energy bottleneck increasingly shifts from device electrostatics to *wiring*: local interconnect resistance/capacitance (RC) and the lateral footprint of standard cells.

D. CFET: Stacking Complementary Devices

CFET addresses wiring and density limits by placing nFET and pFET in the *same lateral footprint* and connecting them vertically. Educational takeaways are: (i) effective cell density can approach $\sim 2\times$ by sharing diffusion/gate footprint across polarities; and (ii) the critical n-to-p connection in inverters and logic stacks shortens, reducing local RC and stage delay. In short, CFET reframes CMOS as a *cross-sectional inverter* rather than a lateral pair [2].

III. CFET Structural Concepts

Two representative integration styles are considered.

(i) Sequential CFET: nFET is fabricated first, followed by pFET under a constrained thermal budget. Selective epitaxy/etch and dielectric isolation are crucial, as is vertical contact to the inverter output.

(ii) Forksheet CFET: n/p channels are placed orthogonally with a dielectric "fork" spacer to ease routing congestion and preserve electrostatics.

IV. Electrical and Layout Impacts

Key educational points include:

- **Area efficiency:** Near $\sim 2\times$ density for inverter cells; benefits extend to NAND/NOR by co-locating pull-up and pull-down networks.
- **Delay/energy:** Vertical n-to-p via shortens RC path; FO1 delay can improve even if device $I-V$ matches GAA.

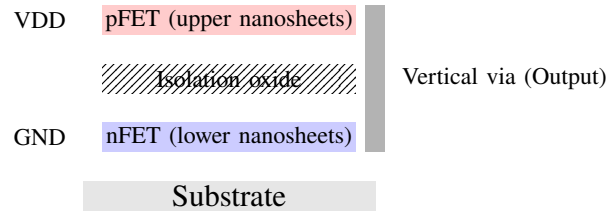

Fig. 2. Sequential CFET cross-section with stacked nFET/pFET and a vertical output via.

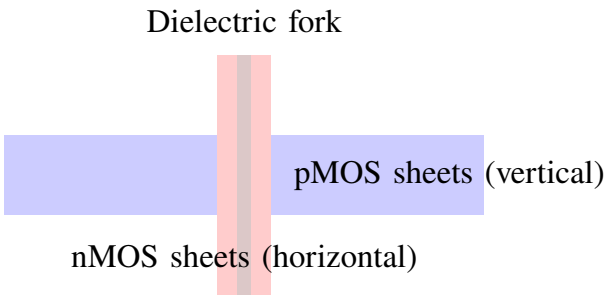

Fig. 3. Forksheet-CFET top view: orthogonal n/p nanosheets separated by a dielectric fork for routing relief.

- **Electrostatics:** Each tier can retain GAA-level control; inter-tier coupling introduces parasitics (capacitance, via resistance).
- **Variability/noise:** Thermal coupling and VDD/GND partitioning introduce asymmetries requiring placement and routing co-optimization.

V. Manufacturing Challenges

Realizing CFET integration introduces unprecedented fabrication hurdles. Independent n/p work-functions and junctions across stacked tiers demand highly selective epitaxy and etching steps, often at low thermal budgets ($< 500^{\circ}$C) to preserve the completed tier. Alignment tolerance for vertical vias is sub-5 nm, requiring EUV lithography overlay beyond current production standards. Dielectric isolation must simultaneously suppress dopant diffusion and maintain mechanical integrity across multiple layers. Recent demonstrations by IMEC indicate sequential CFET feasibility, while large-scale yield, variability control, and reliability remain open challenges [2].

VI. Modeling and EDA Limitations

Existing compact models such as BSIM-CMG can capture GAA device behavior, but extensions to CFET remain absent. Key missing aspects include (i) inter-tier electrostatics, (ii) vertical thermal coupling, and (iii) parasitic RC from stacked vias and tier-to-tier contacts. Prototype Verilog-A implementations exist but lack consensus and calibration. Furthermore, no open-source CFET-ready PDKs or standard-cell libraries are available, preventing standardized design flows. This gap not only limits immediate design enablement but also provides a fertile educational sandbox for research-oriented coursework [1].

VII. Educational Value

From a pedagogical perspective, CFET offers a unique opportunity to bridge device physics, fabrication, layout, and CAD. Graduate courses can integrate CFET Verilog-A models as design projects, explore sensitivity to inter-tier parasitics, and practice co-optimization with placement/routing. Roadmap discussions via IRDS provide context for technology forecasting and design-technology co-optimization (DTCO), bridging device-level abstraction to system-level design [3].

VIII. Conclusion and Outlook

CFET reframes CMOS as a stacked, cross-sectional inverter that simultaneously improves density and wiring delay. Looking forward, forksheet CFET layouts, 3D sequential stacks, thermal-aware power partitioning, co-optimized BEOL integration, and AI-driven design-space exploration are promising directions. Embedding CFET into curricula not only prepares engineers for the 2030s but also cultivates critical thinking about unresolved challenges at the frontier of scaling.

Acknowledgment

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Author Biography

Shinichi Samizo received the M.S. degree in Electrical and Electronic Engineering from Shinshu University, Japan. He worked at Seiko Epson Corporation as an engineer in semiconductor memory and mixed-signal device development, and also contributed to inkjet MEMS actuators and PrecisionCore printhead technology. He is currently an independent semiconductor researcher focusing on process/device education, memory architecture, and AI system integration.

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