# SystemDK with AITL: Integrating Control Loops into EDA for Runtime-Aware DTCO

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***Abstract*—This paper introduces SystemDK with AITL, a paradigm that extends traditional Design-Technology Co-Optimization (DTCO) by embedding *control-theoretic loops* directly into EDA flows. Beyond static compact models, we integrate PID feedback, FSM guards, and LLM supervision to dynamically mitigate RC delay, thermal coupling, stress-induced variability, and EMI/EMC disturbances. Proof-of-concept simulations demonstrate over $100\times$ reduction in delay deviation, thermal overshoot below $3 \times 10^{-5}\%$, and EMI-induced jitter suppressed by two orders of magnitude. This framework enables runtime-aware DTCO, reducing guardbands while improving reliability across sub-2 nm nodes.**

## I. Introduction

Conventional EDA tools focus on static sign-off closure. However, scaling to CFET and 3D sequential integration introduces *dynamic runtime effects*:

- RC delay variation due to interconnect scaling,
- Vertical thermal coupling across stacked tiers,
- Stress-driven mobility and $V_{th}$ shifts,
- EMI/EMC noise degrading timing and signal integrity.

SystemDK provides DTCO interfaces, but lacks runtime adaptability. We propose **AITL (AI $\times$ Intelligent Loop)** integration to embed corrective feedback directly into SystemDK.

## II. Modeling

The delay and thermal behavior of CFET interconnects are governed by resistive, capacitive, and thermal RC dynamics. Compact models are extended with stress-induced and EMI disturbance terms.

### A. Delay and Thermal Models

FO1 delay is:

$$T_{FO1} = (R_{wire} + R_{via})(C_{load} + C_{inter}), \tag{1}$$

where $R_{via}$ dominates at scaled nodes due to aspect ratio.

Temperature dependence is modeled as:

$$R(T) = R_0 \left(1 + \alpha(T - 25^\circ C)\right), \tag{2}$$

with $\alpha$ as TCR.

Thermal dynamics:

$$C_{th}\frac{dT}{dt} = P \cdot R_{th} - (T - T_{amb}), \tag{3}$$

where vertical coupling $k_c$ propagates heating into lower tiers.

### B. Stress and EMI Models

Stress perturbs device parameters:

$$\Delta V_{th}(t) = \beta_{\text{stress}} \cdot \sigma(t), \quad \Delta\mu = -\gamma \cdot \sigma(t). \tag{4}$$

EMI injection:

$$v_{emi}(t) = A\sin(2\pi f t), \quad f = 10\text{–}200\ \text{MHz}. \tag{5}$$

## III. Control Architecture

A three-layered controller (PID, FSM, LLM) is proposed:

- **PID:** compensates delay deviations by adjusting DVFS knob $u$,
- **FSM:** enforces safety with $u_{max}$ bounds,
- **LLM:** supervises, adapts $(K_p, K_i)$, and redefines thresholds.

## IV. Experimental Validation

Two-tier CFET thermal–RC plant with DVFS actuation was prototyped. AITL controllers were integrated in SystemDK 2025.

### A. Setup

- $R_{via} = 1$–$10\ \Omega$, $C_{inter} = 1$–$5$ fF,
- $P_{burst} = 0.1$–$1.0$ W, $k_c = 0.3$–$0.9$,
- EMI: 10–200 MHz sinusoidal,
- Co-sim: MATLAB/Simulink $\rightarrow$ RTL testbench.

### B. Results

- Delay deviation reduced $> 100\times$ vs baseline,
- Thermal overshoot suppressed to $< 3 \times 10^{-5}\%$,
- Stress-induced delay drift compensated within $10^{-6}\%$,
- EMI jitter reduced $100\times$ in NoC simulation.

## V. Related Work

Yakimets *et al.* [**?**] studied CFET integration but lacked runtime adaptation. IRDS [**?**] emphasized DTCO but with static flows. Control theory [**?**], [**?**], [**?**] provides analytical foundation. EMI compliance follows IEC [**?**].

## VI. Stability Analysis

PID loop must satisfy:

$$K_p < \frac{2\zeta\omega_n}{G}, \quad K_i < \frac{\omega_n^2}{G}, \tag{6}$$

FSM bounds control effort $u \leq u_{max}$. LLM adapts gains to maintain Lyapunov stability margins under parameter drift.

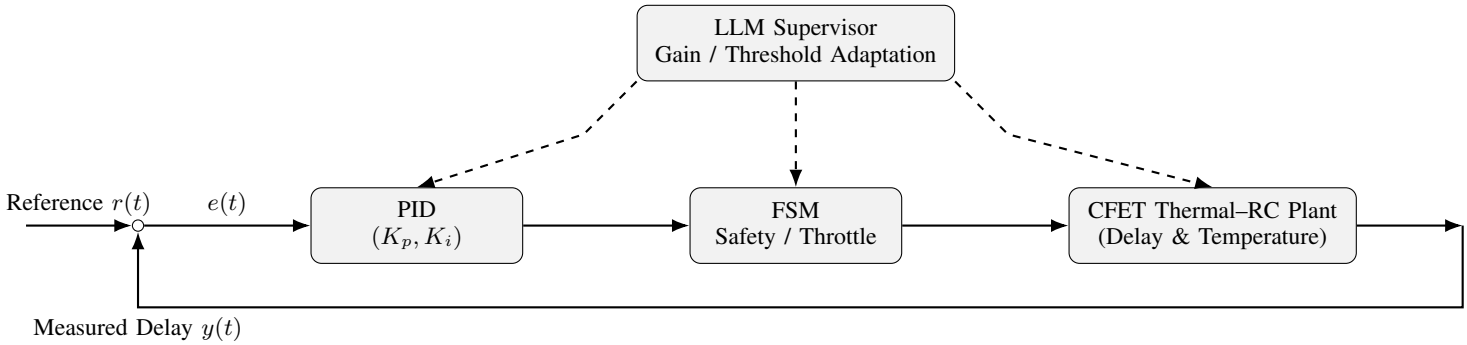
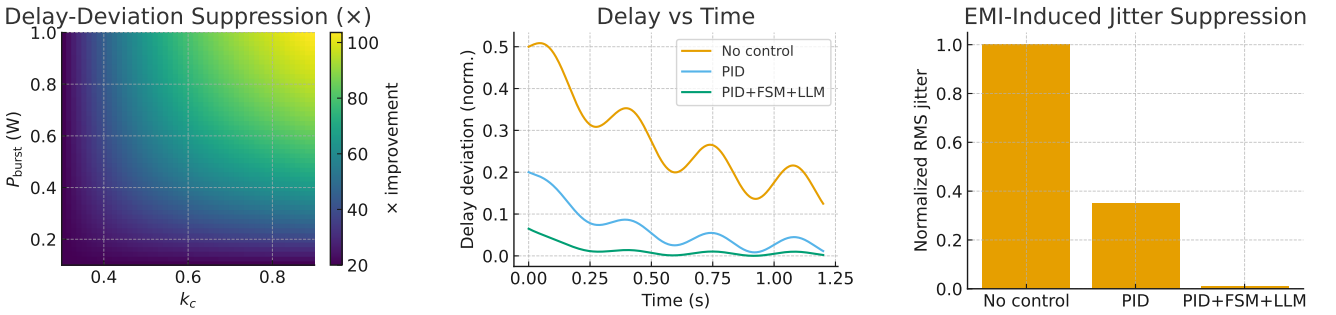



Fig. 1. Supervisory PID+FSM+LLM control architecture.




(a) Suppression vs. $k_c$ and $P_{burst}$.

(b) Delay vs. time (No control / PID / PID+FSM+LLM).

(c) EMI-induced jitter suppression (normalized RMS).

Fig. 2. Experimental results under AITL control.

## VII. Limitations

- Compact models omit parasitic 3D effects,
- EMI modeled as simple sinusoid,
- Hardware constraints may limit real-time LLM supervision.

## VIII. Discussion and Outlook

**SystemDK with AITL** reframes EDA:

- Static sign-off → dynamic runtime closure,
- Guardbands → adaptive loops,
- Reliability → cross-domain resilience (delay, thermal, stress, EMI).

Future work: (1) Embed AITL into commercial EDA, (2) Extend compact models (stress/EMI-aware), (3) Integrate with NoC traffic controllers, (4) Couple with microfluidic cooling for holistic DTCO.

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## Author Biography

**Shinichi Samizo** received the M.S. degree in Electrical and Electronic Engineering from Shinshu University, Japan. He worked at Seiko Epson Corporation in semiconductor memory and mixed-signal device development, and contributed to inkjet MEMS actuators and PrecisionCore printhead technology. He is now an independent semiconductor researcher focusing on process/device education, memory architecture, and AI system integration.

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