Low-Cost Integration of 1.8-V FeFET on 0.18-μm CMOS: +1 Mask and a Single ALD Tool, with Reliability Assessment

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***Abstract*—Ferroelectric FETs (FeFETs) are promising CMOS-compatible embedded NVMs. This paper demonstrates a 1.8 V FeFET module integrated on a legacy 0.18 μm CMOS process with only one additional mask and a single ALD tool. Fabricated devices show endurance exceeding 10^5 program/erase cycles and retention longer than 10 years at 85°C. Reliability was characterized on FeCAP/FeFET structures: time-zero dielectric breakdown (TZDB), time-dependent dielectric breakdown (TDDB), endurance, and retention. The approach provides a cost-effective path to extend mature-node lifetimes and to enable embedded NVM for automotive/industrial/IoT, while high-temperature retention remains the key limiter.**

I. Introduction

FeFETs based on HfO_2 have gained traction as CMOS-compatible NVMs. Most prior work targets advanced nodes; however, mature nodes (~0.18 μm) remain widely used in automotive/industrial markets where long supply lifetimes and low cost are critical. **This work contributes**: (i) a +1 mask low-cost module, (ii) only one ALD tool added to the line, (iii) a yield-friendly *SRAM+FeFET* system usage model, and (iv) comprehensive reliability evidence on FeCAP/FeFET.

II. Process Integration

Baseline is a 0.18 μm CMOS platform (1.8 V core, optional 3.3 V I/O). The FeFET module is inserted after poly definition and salicide/RTA, requiring minimal line modification.

A. Process Flow

B. Cross Section

III. Devices and Methods

Test structures include FeCAPs (flat/comb) and 100 μm × 100 μm FeFET cells. Programming used ±2.3–2.7 V, 1–50 μs pulses. Keysight B1500A and a manual probe were used.

Protocols: TZDB: DC ramp ≈ 0.1 V/s at RT–125°C. TDDB: constant-voltage stress at ±2.3/2.5/2.7 V, 85°C and 125°C; Weibull fitting. Endurance: ±2.5 V, 10 μs, 10 kHz up to 10^5 cycles. Retention: 25°C, 85°C, 125°C, with Arrhenius extrapolation.

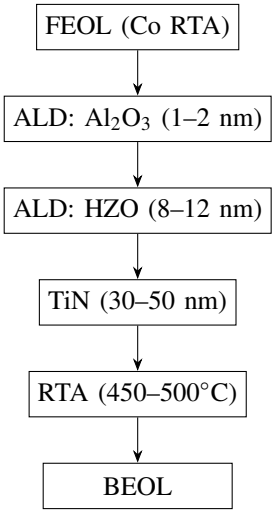


Fig. 1. Process flow of FeFET integration.

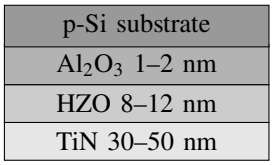


Fig. 2. Cross section of HZO/Al_2O_3/TiN stack.

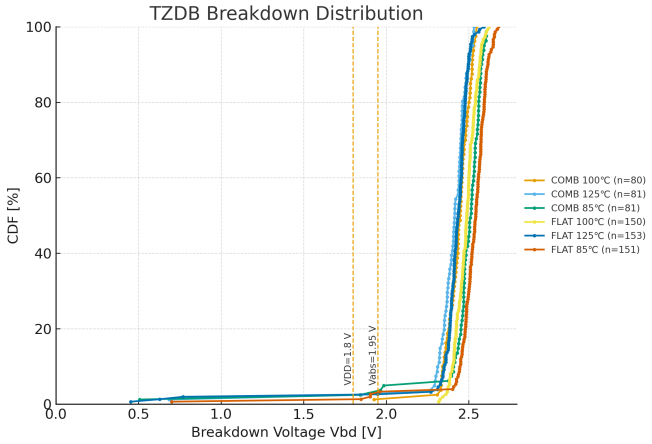
IV. Results

A. TZDB

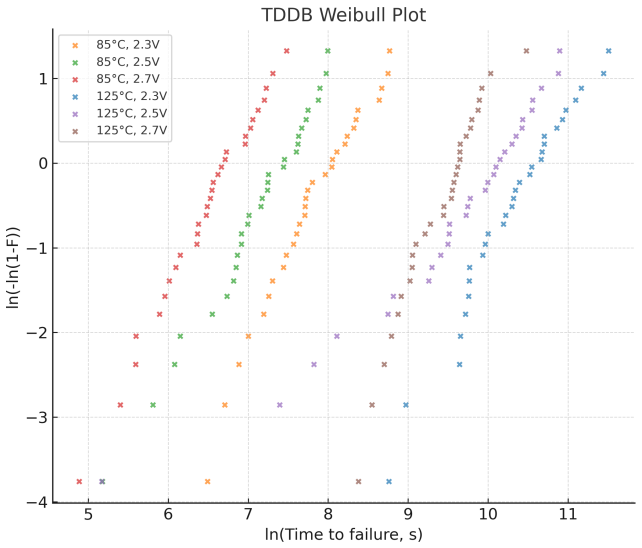
Breakdown statistics indicate early-failure tails due to defects.

B. TDDB (Weibull/Arrhenius)

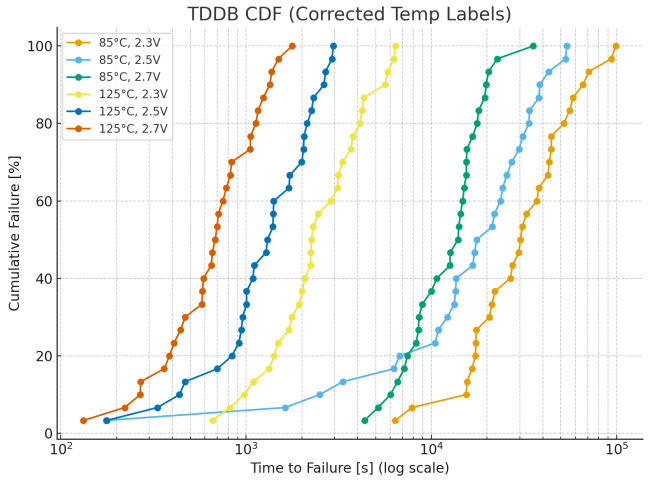
Weibull plots yield $\beta \approx 1.3$. Arrhenius analysis gives activation energies consistent with oxygen-vacancy diffusion: $E_a \approx 0.78$ eV @ 2.3 V, 0.84 eV @ 2.5 V, 0.88 eV @ 2.7 V.



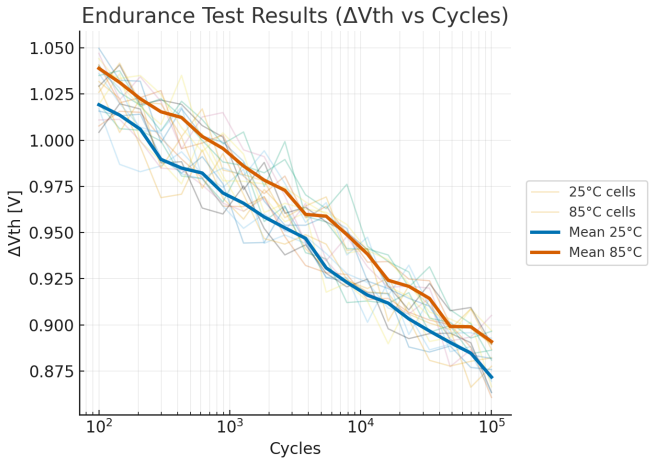
(a) TZDB distributions of FeCAPs.



(b) TDDB Weibull plots with fitted lines (β, η).



(c) TDDB CDF under all stress conditions.



(d) Endurance characteristics (ΔV_{th} vs. cycles).

Fig. 3. Reliability results summary.

C. Endurance

Up to 10^5 cycles verified; the window shrinks 20–30%. A compact fit is $\Delta V_{\text{th}}(N) = 1.12 - 0.05 \log_{10} N$.

D. Retention

Arrhenius extrapolation with $E_a \approx 1.1$ eV predicts: >100 years @ 25°C, >10 years @ 85°C, and only months @ 150°C.

V. System Architecture (SRAM + FeFET)

The SoC uses a single 1.8 V core domain for logic, SRAM, and FeFET access. Write/erase pulses (±2.3–2.7 V, 1–50 μs) are generated by an on-chip charge pump. A lightweight backup controller copies SRAM contents to the FeFET array on power-fail detection and restores them at power-up. An optional 3.3 V peripheral domain is kept for I/O and AMS (ADC/DAC, LDO).

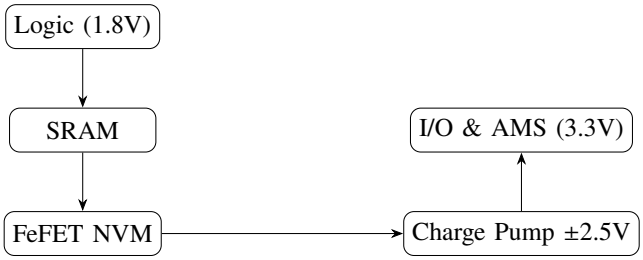


Fig. 4. System architecture with SRAM + FeFET backup.

Fig. 5. Backup/restore flow between SRAM and FeFET.

VI. Discussion

The HZO/Al_2O_3/TiN stack provides sufficient reliability for industrial/consumer embedded NVM. For high-temperature

automotive, improvements are required: IL optimization, crystallinity control, refresh/rewrite, and ECC.

VII. Conclusion

We realized an FeFET module on 0.18 μm CMOS with one extra mask and one ALD tool. Devices exhibit > 10^5 cycles and > 10 years retention at 85°C. The method extends mature-node lifetime and enables cost-effective embedded NVM for automotive/industrial/IoT.

Acknowledgment

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Biography

Shinichi Samizo has over 25 years of experience in semiconductor process integration and actuator development. After studying control theory and EM modeling in academia, he joined Seiko Epson in 1997 and worked on 0.35–0.18 μm CMOS logic/memory/HV integration, DRAM, and LCD drivers. Later he contributed to PZT actuator development and the PrecisionCore inkjet head. He is currently an independent researcher, publishing educational materials via the ‘‘Project Design Hub’’.