Low-Cost Integration of 1.8-V FeFET on 0.18-μm CMOS: +1 Mask and a Single ALD Tool, with Reliability Assessment

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***Abstract*—Ferroelectric FETs (FeFETs) are promising CMOS-compatible embedded nonvolatile memories. This paper demonstrates a 1.8 V FeFET module integrated on a legacy 0.18 μm CMOS process with only one additional mask and a single ALD tool. Fabricated devices show endurance exceeding 10^5 program/erase cycles and retention longer than 10 years at 85°C. Reliability was characterized on FeCAP/FeFET structures: time-zero dielectric breakdown (TZDB), time-dependent dielectric breakdown (TDDB), endurance, and retention. The approach provides a cost-effective path to extend mature-node lifetimes and to enable embedded NVM for automotive/industrial/IoT, while high-temperature retention remains the key limiter.**

I. Introduction

Ferroelectric HfO_2-based memories attract attention as CMOS-compatible NVMs [1]–[4]. While many works target advanced nodes, mature nodes (e.g., 0.18 μm) remain workhorses in automotive/industrial sectors for cost and longevity. **This work contributes**: (i) a +1 mask low-cost module, (ii) only one ALD tool added to the line, (iii) a yield-friendly *SRAM+FeFET* system usage model, and (iv) comprehensive reliability evidence (TZDB, TDDB, endurance, retention) on FeCAP/FeFET.

II. Process Integration

Baseline is a 0.18 μm CMOS platform (1.8 V core, optional 3.3 V I/O). The FeFET module is inserted after poly definition and salicide/RTA, requiring minimal line modification.

A. Process Flow

B. Cross Section

III. Devices and Methods

Test structures include FeCAPs (flat/comb) and 100 μm × 100 μm FeFET cells. Programming used ±2.3–2.7 V, 1–50 μs pulses. A Keysight B1500A with a manual probe station was used.

Protocols: TZDB: DC ramp ≈ 0.1 V/s at RT–125°C. TDDB: constant-voltage stress at ±2.3/2.5/2.7 V, 85°C and 125°C; Weibull fitting. Endurance: ±2.5 V, 10 μs, 10 kHz up to 10^5 cycles. Retention: 25°C, 85°C, 125°C with Arrhenius extrapolation.

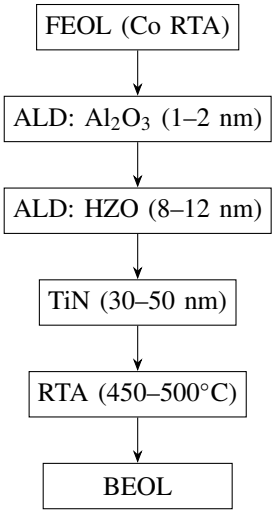

Fig. 1. Process flow of FeFET integration.

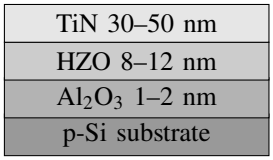

Fig. 2. Cross section of HZO/Al_2O_3/TiN stack.

TABLE I
Reliability test matrix (devices: FeCAP/FeFET).

Item	Conditions
TZDB	DC ramp ≈ 0.1 V/s, RT–125 °C
TDDB	±2.3/2.5/2.7 V, 85 °C, 125 °C
Endurance	±2.5 V, 10 µs, 10 kHz, up to 10^5
Retention	25 °C, 85 °C, 125 °C

IV. Results: Reliability

To keep readability high and figure sizes uniform, the reliability results are split across multiple figures (all with identical width).

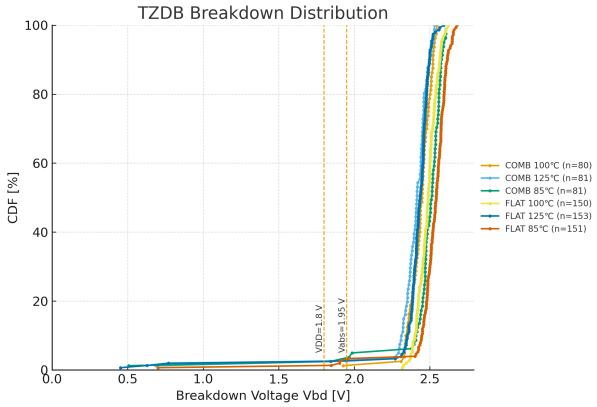

Fig. 3. TZDB distributions of FeCAPs. Early-failure tails imply defect-driven breakdown paths.

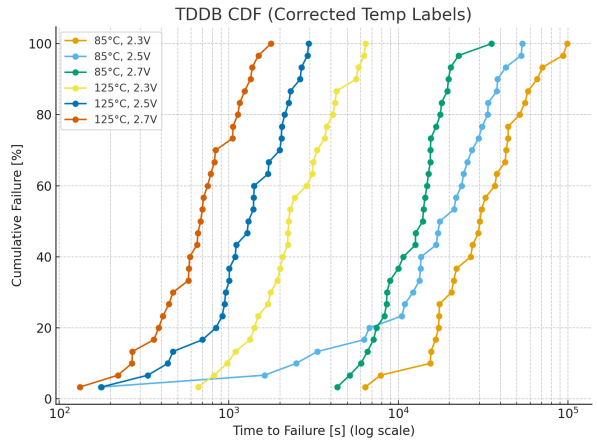

Fig. 4. TDDB cumulative failure probability (CDF) under multiple stress conditions (85°C / 125°C, ±2.3/2.5/2.7 V).

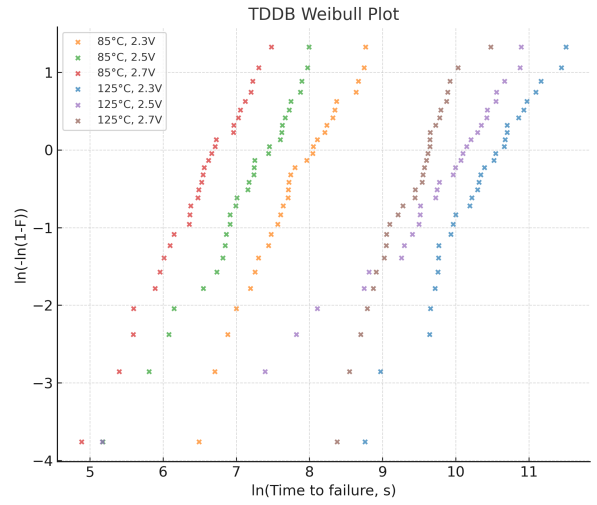

Fig. 5. TDDB Weibull plots with fitted slope $\beta \approx 1.3$ and scale η.

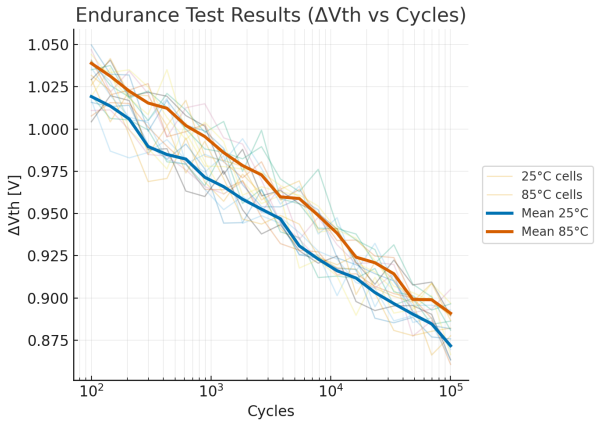

Fig. 6. Endurance characteristics (ΔV_{th} vs. cycles). Up to 10^5 cycles; window shrinks 20–30%.

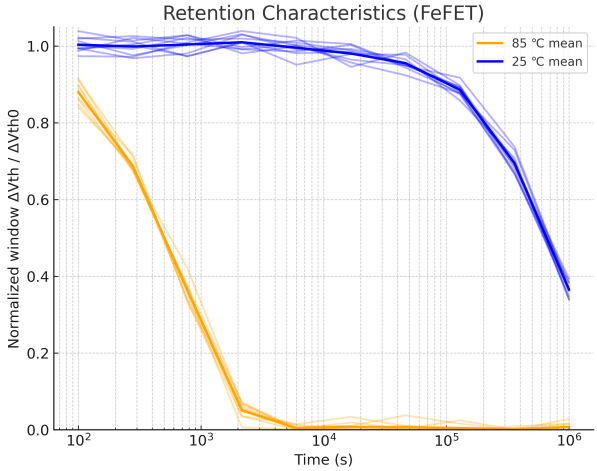

Fig. 7. Retention summary (CDF and/or Arrhenius extrapolation).

A. *Time-Zero Dielectric Breakdown (TZDB)*

B. *TDDB under Constant-Voltage Stress*

C. *Endurance*

D. *Retention*

E. *Model Fits*

Time-to-failure under constant-voltage stress follows a Weibull law

$$F(t) = 1 - \exp\left[-\left(\frac{t}{\eta}\right)^{\beta}\right], \tag{1}$$

with slope $\beta \approx 1.3$ and scale η extracted from Fig. 5. Temperature acceleration is described by an Arrhenius relation

$$\ln\left(\frac{t_2}{t_1}\right) = \frac{E_a}{k}\left(\frac{1}{T_2} - \frac{1}{T_1}\right), \tag{2}$$

yielding activation energies $E_a \approx 0.78$ eV (2.3 V), 0.84 eV (2.5 V), 0.88 eV (2.7 V). A compact endurance fit capturing memory-window shrink is

$$\Delta V_{\text{th}}(N) \approx 1.12 - 0.05 \log_{10} N. \tag{3}$$

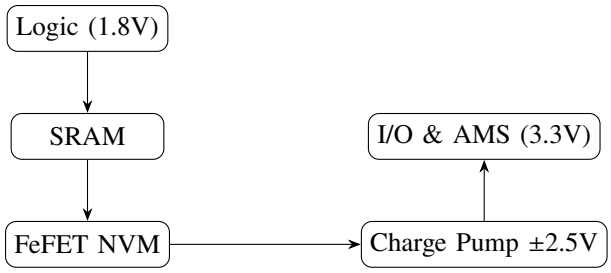

Fig. 8. System architecture with SRAM backup to FeFET (single-column).

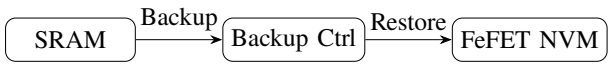

Fig. 9. Backup/restore flow between SRAM and FeFET (single-column).

V. System Architecture (SRAM + FeFET)

The SoC uses a single 1.8 V core domain for logic, SRAM, and FeFET access. Write/erase pulses (±2.3–2.7 V, 1–50 μs) are generated by an on-chip charge pump. A lightweight controller backs up SRAM contents to the FeFET array on power-fail detection and restores them at power-up. An optional 3.3 V peripheral domain is kept for I/O and AMS (ADC/DAC, LDO).

VI. Discussion

The HZO/Al_2O_3/TiN stack shows sufficient reliability for industrial/consumer embedded NVM. For high-temperature automotive, improvements are required:

- **Interlayer (IL) optimization**: Al_2O_3 thickness/composition tuning to mitigate wake-up/fatigue and reduce leakage.
- **Crystallinity control**: RTA window and TiN work-function engineering to stabilize ferroelectric phase and reduce variation.
- **Defect mitigation**: Precursor purity, ALD purge optimization, and post-deposition anneal to suppress oxygen-vacancy paths (helps TDDB/retention).
- **Circuit assists**: Verify-and-rewrite (background refresh at high-T), ECC, and adaptive write pulse shaping to slow window loss.
- **Array architecture**: Redundancy/repair and SRAM+FeFET hybrid usage to keep frequent writes on SRAM, reducing FeFET stress.

VII. Conclusion

We realized a +1 mask FeFET module on 0.18 μm CMOS with only one additional ALD tool. Devices exhibit $> 10^5$ cycles and $>$ 10 years retention at 85°C, verified by TZDB/TDDB/endurance/retention analyses. The method extends mature-node lifetime and enables cost-effective embedded NVM for automotive/industrial/IoT.

Acknowledgment

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References

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Biography

Shinichi Samizo has over 25 years of experience in semiconductor process integration and actuator development. After studying control theory and EM modeling in academia, he joined Seiko Epson in 1997 and worked on 0.35–0.18 μm CMOS logic/memory/HV integration, DRAM, and LCD drivers. Later he contributed to PZT actuator development and the PrecisionCore inkjet head. He is currently an independent researcher, publishing educational materials via the ‘‘Project Design Hub’’.