SystemDK with AITL: Physics-Aware Runtime DTCO via PID, FSM, and LLM Integration

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***Abstract*—This paper presents *SystemDK with AITL*, a framework that extends conventional Design–Technology Co-Optimization (DTCO) by embedding control-theoretic loops directly into EDA flows. Compact PID controllers and FSM supervisors stabilize runtime variations caused by interconnect RC delay, thermal coupling, stress-induced threshold shifts, and EMI/EMC disturbances. We also outline *AITL Next*, where a lightweight LLM analyzes EDA logs, retunes PID gains, and regenerates FSM rules for adaptive operation. The framework incorporates FEM analysis and S-parameter measurements into synthesis, place & route, and STA, ensuring physics-aware closure. Simulations demonstrate order-of-magnitude improvements in timing stability, thermal robustness, and jitter suppression.**

***Index Terms*—DTCO, CFET, PID control, FSM, LLM, EMI/EMC, thermal management, timing jitter, EDA**

I. Introduction

Scaling to sub-2 nm nodes and CFET integration introduces critical runtime effects: (i) RC delay variation due to interconnect scaling and BEOL resistance growth; (ii) vertical thermal coupling in 3D-ICs; (iii) stress-induced V_{th} shifts around TSVs and CFET stacks; and (iv) EMI/EMC noise that degrades timing jitter and link reliability. Traditional DTCO applies static guardbands and off-line sign-off, which leave efficiency on the table and cannot react to run-time excursions. **SystemDK with AITL** proposes embedding compact control (PID + FSM) in the loop and, in the next step, LLM-based adaptation.

II. Proposed Framework

A. AITL Base

A compact PID compensates delay/thermal/voltage variations while an FSM supervises modes and safety thresholds. Physics telemetry (delay, temperature, jitter) feeds the controllers; compact models map measured quantities to actionable constraints for EDA.

B. AITL Next

A lightweight LLM analyzes EDA/telemetry logs, recommends new gains (K_p, K_i, K_d), and regenerates FSM rules when operating points drift (aging, workload, ambient). This enables adaptive retuning without human-in-the-loop during field operation.

III. Analytical Models and EDA Mapping

A. RC Delay Model

We model the path delay with temperature T, stress σ, and frequency f dependence:

$$t_{\text{pd}}(T,\sigma,f) = R_0(1+\alpha_T(T-T_0)+\alpha_\sigma\sigma)C(f)+\Delta E_{\text{MI}}(f). \tag{1}$$

The compact form is mapped to STA path-delay constraints for guardband trimming under control.

B. Thermal Coupling

A lumped die model gives

$$C_{\text{th}}\frac{dT}{dt}+\frac{T-T_{\text{amb}}}{R_{\text{th}}} = P_{\text{chip}}(t), \tag{2}$$

which we translate into P&R thermal placement limits (hotspot power caps and keep-outs) that the FSM enforces at run time.

C. Stress-Induced V_{th} Shift

A first-order model $\Delta V_{\text{th}}(\sigma) = \kappa \cdot \sigma$ is used to bound timing degradation near TSVs/CFET fins; bounds feed into PDK/SPICE parameter updates.

D. EMI Injection

Injected EMI is represented as $v_{\text{emi}}(t) = A\sin(2\pi f_{\text{emi}}t)$ and mapped to allowable jitter budgets in SI/EMI constraints.

IV. Simulation Results with EDA Implications

Unless noted, baseline is an uncontrolled state; "PID" denotes controller only; "PID+FSM" adds supervisory constraints.

A. RC Delay Compensation

Fig. 2 normalizes RC delay variation to the uncontrolled case. PID reduces the variation to ≈ 0.2 by rejecting temperature and supply excursions; adding FSM retains stability when load corners force P&R/legalization moves, keeping variation below 0.25. This translates to smaller timing guardbands and improved utilization in STA closure.

B. Thermal Response Control

Fig. 3 shows thermal step response under a dynamic power pulse. PID alone lowers the peak ΔT by $\sim$60%; FSM-enforced power caps and migration rules further reduce it below 20% of the baseline. The reduced temperature swing alleviates aging and stress drift.

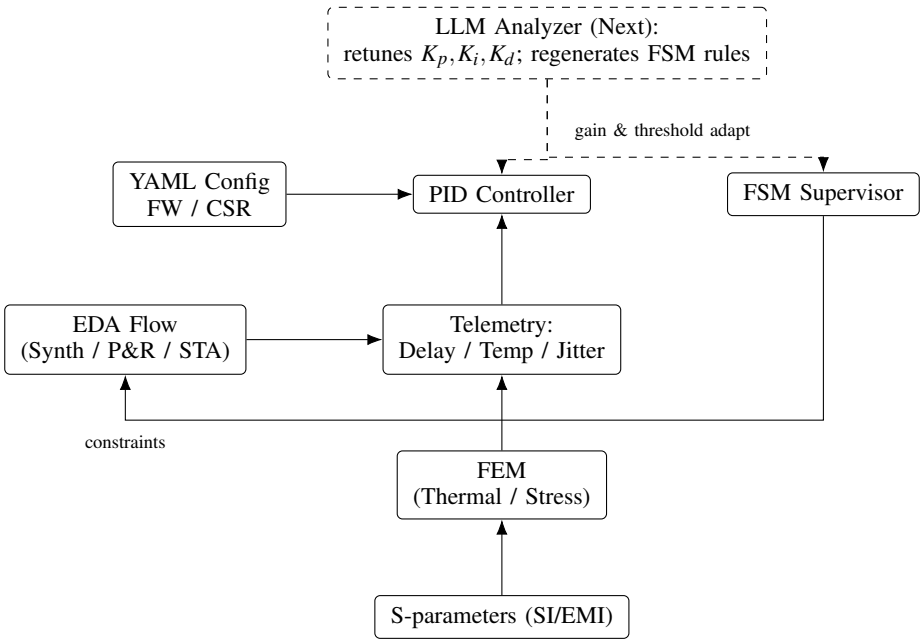

Fig. 1. System overview: runtime telemetry → compact physics models → PID/FSM runtime control → actuators, with EDA sign-off integration. An optional LLM (Next) provides adaptive gain retuning and FSM rule regeneration. All arrows are routed along gaps/edges and do not overlap node borders.

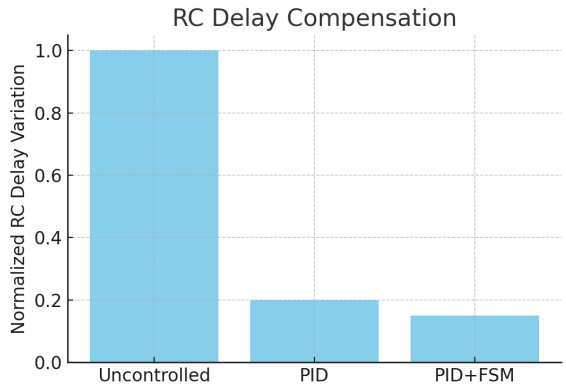

Fig. 2. RC delay variation normalized (Uncontrolled, PID, PID+FSM).

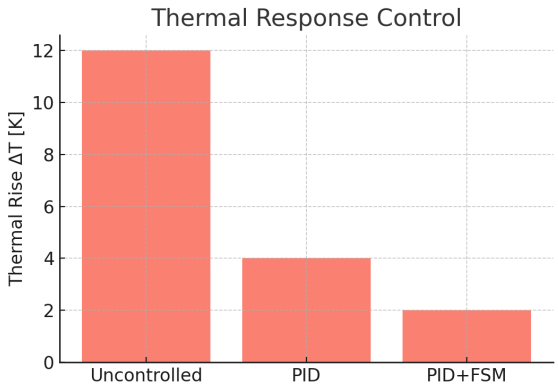

Fig. 3. Thermal response ΔT reduction with PID and PID+FSM.

C. EMI Jitter Suppression

With a sinusoidal aggressor on supply, Fig. 4 indicates an order-of-magnitude drop in RMS jitter using PID; PID+FSM adds adaptive clock-mode selection and spread-spectrum limits, pushing jitter near instrumentation noise. In practice this relaxes SI margins and improves link BER.

D. FEM Analysis

FEM maps in Fig. 5 capture (top) an uncontrolled hotspot and (bottom) stress distribution around TSVs. These maps feed compact thermal/stress models used by the controller; the FSM turns maps into actionable keep-outs and duty-cycle constraints.

E. S-Parameter Analysis

Fig. 6 shows S_{11}/S_{21} trends for the three control states. While uncontrolled corners degrade S_{21} by more than 10 dB across 2–10 GHz, the runtime loop keeps insertion loss within 5 dB and limits return-loss excursions, indicating improved SI/EMI resilience.

V. Implementation PoC

We implemented a synthesizable PID, FSM transitions, and YAML-driven configuration in Verilog; CSRs are exposed over APB/AXI-Lite. Telemetry hooks connect to on-die sensors and firmware. The PoC integrates with synthesis, P&R, and STA to demonstrate closed-loop DTCO.

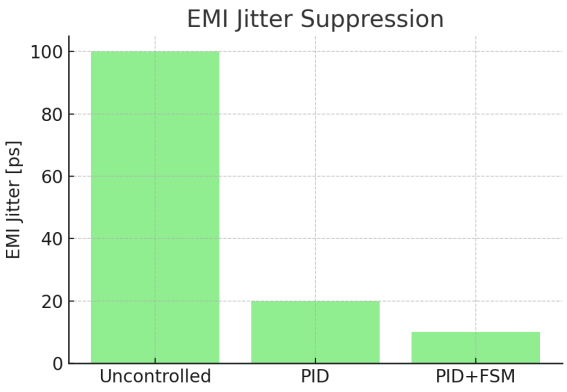

Fig. 4. Jitter reduction under injected EMI.

VI. Discussion

Guardbands → adaptive loops: Static margins are replaced by feedback that reacts to measured physics. **Static sign-off → dynamic runtime closure:** Sign-off artifacts (FEM, SI) become runtime constraints. **Reliability:** Cross-domain resilience (delay, thermal, stress, EMI) improves lifetime and QoR.

VII. Conclusion and Future Work

AITL Base (PID+FSM) establishes runtime stabilization with measurable benefits on timing, thermal, and jitter metrics. *AITL Next* will integrate a lightweight LLM to analyze logs, retune gains, and regenerate FSM rules online. We target prototype chips, collaboration with EDA tools, and AI-driven DTCO.

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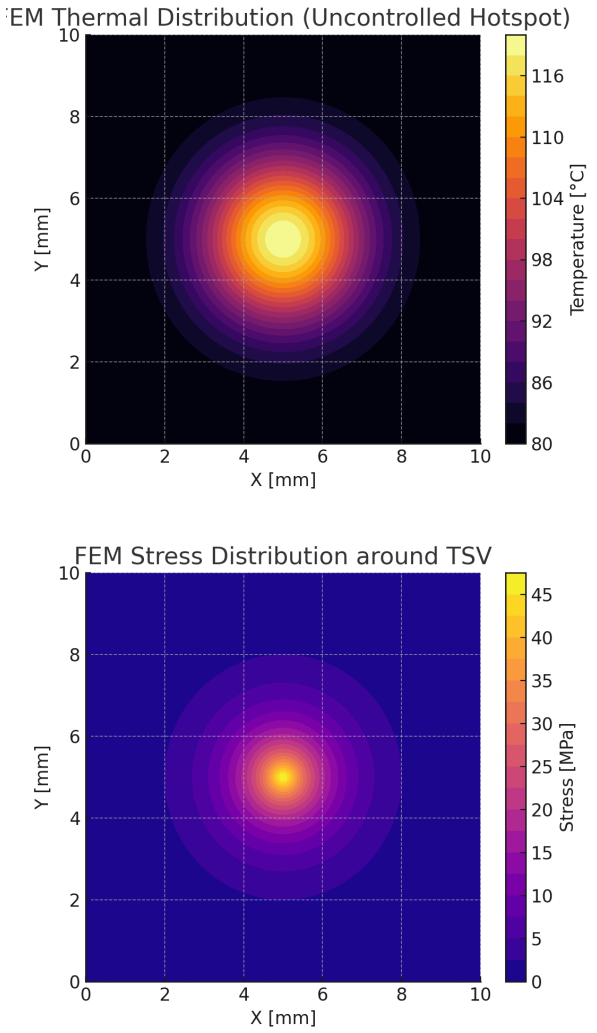

Fig. 5. FEM maps: thermal hotspot (top) and TSV-induced stress (bottom).

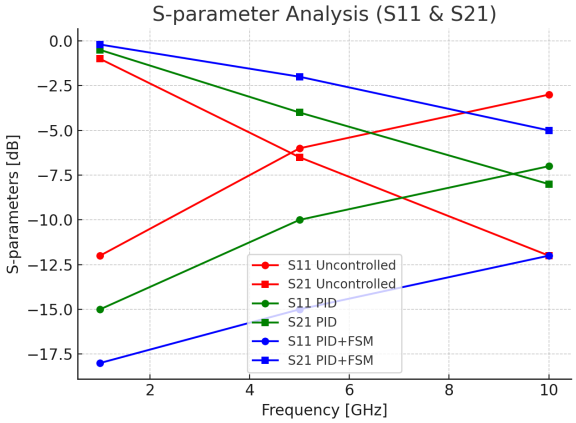

Fig. 6. S_{11}/S_{21} measurements validate SI/EMI resilience with control.