

# Historical Case Study: 0.25- $\mu\text{m}$ 64-Mbit DRAM Ramp-up and Pseudo-SRAM (VSRAM)

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**Abstract**—In 1998, a 3rd-generation 64-Mbit DRAM was transferred and ramped on a 0.25- $\mu\text{m}$  process using short-cycle feedback (SCF) and a parallel introduction of production and margin lots. The initial yield was  $\sim 65\%$ , dominated by retention-related failures under pause-refresh (Bin-5) and disturb-refresh (Bin-6) tests. Process tracing indicated cumulative plasma damage from resist ashing after WSA-ET and multiple LDD steps as a primary root cause. By shifting resist stripping to wet processes and strengthening body back-bias, the yield improved to  $\sim 80\%$  and passed long-term reliability. We position this as a practical ramp-up design framework and discuss its continuity to modern phenomena (e.g., row-disturb/row-hammer) and its educational value.

## I. INTRODUCTION

In the late 1990s, Japan’s semiconductor industry was in transition. At Epson’s Sakata 8-inch fab, DRAM was *not* pursued as an end business; rather, DRAM technology transfer was used as a **strategic vehicle** to absorb submicron process technologies at and beyond 0.35  $\mu\text{m}$  and redeploy them into Epson’s core devices (ASICs, logic ICs, display drivers, and inkjet driver ICs).

The technology transfer from Mitsubishi covered three nodes, each with a clear role: (1) 0.5  $\mu\text{m}$  16 Mbit DRAM — to establish mass-production capability and stabilize fab operation; (2) 0.35  $\mu\text{m}$  64 Mbit DRAM (2nd gen) — to introduce a scaled process while tackling yield window narrowing; (3) 0.25  $\mu\text{m}$  64 Mbit DRAM (3rd gen) — as the next-stage validation bed and the basis for in-house deployment.

This paper focuses on the 0.25  $\mu\text{m}$  (3rd gen) ramp-up in 1998: a process overview, the ramp-up method, and a failure-analysis-driven yield-improvement cycle. We also trace how these results enabled the 0.25  $\mu\text{m}$  mobile pseudo-SRAM (VSRAM) in 2001 and why trench-based 0.18  $\mu\text{m}$  VSRAM was abandoned.

## II. BACKGROUND

This work builds on the author’s 1997–1998 ramp activities at Epson’s Sakata fab under technology transfer from Mitsubishi; details are summarized in the Introduction and referenced archives.

## III. PROCESS OVERVIEW AND RAMP-UP METHOD

### A. Process Overview (0.25- $\mu\text{m}$ 64 Mbit DRAM, 3rd Gen)

- **Lithography:** First adoption of a KrF stepper for 0.25- $\mu\text{m}$  volume exposure.

- **Isolation:** Semi-recess LOCOS.
- **Wells:** Triple-well with Deep N-Well to improve cell noise immunity.
- **Word-Line Gate Electrode:** CVD tungsten silicide (WSi). A dielectric **barrier cap (BRAC)** sits atop the WL stack, providing etch robustness and insulation.
- **Bit Line:** *Self-aligned contact* — the bit-line contact and the bit line are formed simultaneously by WSi-CVD; the BRAC blocks contact-to-WL shorts.
- **Storage Node Capacitor:** Stacked capacitor; surface roughening yields  $\sim 1.5\text{--}1.8\times$  capacitance gain.
- **Metallization/Passivation:** AlCu/TiN interconnect; SOG planarization; SiN or PI passivation.

### B. Ramp-up Method

The node transfer followed a factory-wide, fast-turn scheme:

a) *Base flow:* SCF  $\rightarrow$  shape lots  $\rightarrow$  production lots:

- 1) **Short Cycle Feedback (SCF):** Each unit process (diffusion, CVD/PVD, etch, etc.) runs short-cycle wafers per its ramp-up spec to quickly evaluate and lock conditions.
- 2) **Shape lots ( $\sim 10$  lots):** Provide *real product wafers* to unit teams for items only assessable on full stacks and, in parallel, (i) verify photo CDs, (ii) photo $\rightarrow$ etch CD transfer, and (iii) cross-sections after interlayer films. Recipes are updated for following lots.
- 3) **Production (reliability) lots:** Multiple lots for wafer test and long-term reliability (incl. burn-in) to judge mass-production readiness.

b) *Practical flow (author’s role):* Process conditions (two floppy disks) were received from the mother fab and deployed to unit teams; each team executed SCF and fed back updates. The author consolidated the latest settings into the *electronic traveler*, launched  $\sim 10$  shape lots, fixed target CDs/films, and then ran 5 reliability lots for E-test and reliability signoff.

c) *Operations to compress schedule:* Normal lots use stocker  $\leftrightarrow$  rail transfer and queue at tools. For critical first-pass lots, we used **hand-carry flow**: engineers delivered cassettes to tools with operators standing by, eliminating transfer/queue loss. Even so, a full pass took about two months; the entire ramp spanned  $\sim 5$  months. Daily morning meetings posted a laminated traveler on a whiteboard to visualize lot progress, schedule slip (in days), and unit-team status. Technical staff also operated in a two-shift scheme (day/night) to sustain 24/7 feedback.

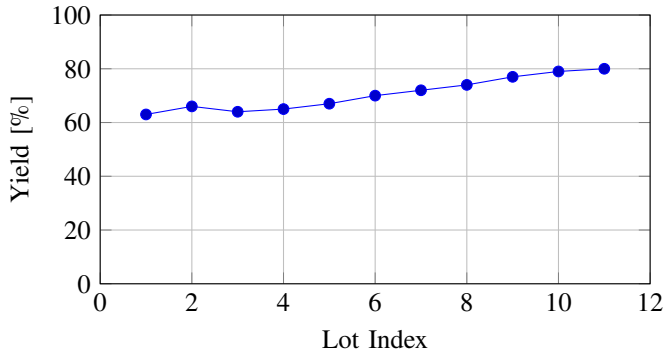


Fig. 1. Yield evolution during the 0.25-μm ramp.

#### IV. FAILURE ANALYSIS AND YIELD IMPROVEMENT

##### A. Initial Observation

The first production lots showed ~65% yield. Wafer test was dominated by **Pause Refresh Fail (Bin5)**. Defects appeared as uniformly scattered single-bit errors across the wafer (weak clustering, no edge/line signature). Storage-node capacitance met spec; SEM cross-sections at failed cells revealed no structural anomaly. Other CDs/films/electricals were within spec.

##### B. Hypothesis (Failure Model)

Directly measurable leakages were normal, suggesting a subtle leakage path. We hypothesized increased leakage at the **storage-node contact  $n^+/p^-$  junction**. After gate etch, a remnant gate oxide on S/D active is repeatedly exposed to resist-stripping *ashing* during multiple LDD steps. Cumulative plasma damage makes the oxide locally porous and can extend damage into the diffusion, creating minute leakage paths. This explains random single-bit distribution without visible structural defects.

##### C. Countermeasures

- **Process:** Replace resist stripping in LDD steps from plasma ashing to **wet stripping (sulfuric-based)** to eliminate plasma damage.
- **Integration hygiene:** Confirm downstream photo cleanliness and avoid residue risks with the wet strip.

##### D. Effectiveness

Yield improved from ~65% to ~80%. Uniformly scattered single-bit fails decreased markedly. Burn-in and retention/reliability passed; the final recipe was fixed for volume production.

#### V. FROM DRAM RAMP TO MOBILE VSRAM (2001)

Around 2000, market focus shifted from PC DRAM to mobile devices. Sharp's camera-phone project demanded **high-density, low-power memory**. Leveraging the 0.25-μm DRAM process, Epson mass-produced a **pseudo-SRAM (VSRAM)** by adding internal refresh control and extending the operating guarantee from 80 °C to 90 °C for mobile use. Initial yield

was only ~30%, yet production started as a *rational business decision* to secure market entry, and yield was improved in-flight.

##### A. Integrated Challenges and Solutions

a) *Pause Refresh under 90 °C and extended refresh interval:* To reduce standby current, the internal refresh interval was lengthened; coupled with 90 °C spec, junction leakage limits surfaced. *Process*—building on the DRAM fix—wet stripping replaced ashing; additionally, **minimized HF cleans** preserved gate-oxide residual thickness, mitigating diffusion damage and storage-node contact leakage. *Device bias*—body bias was deepened from -1 V to -3 V to suppress temperature-sensitive leakage while maintaining switching capability.

b) *Disturb Refresh at short channel:* At 0.25 μm, repeated neighboring WL activations aggravated channel disturbance. We tightened **gate CD centering** and optimized **cell-channel doping** to raise  $V_{th}$  moderately while keeping access speed; the deeper body bias also helped disturb immunity.

c) *Outcome:* With these combined actions, yield improved from ~30% at launch to **80–90%** while production continued, and high-temperature reliability was satisfied.

#### VI. CONCLUSION

The 0.25-μm DRAM ramp at Epson's Sakata fab demonstrated how DRAM can function as a **strategic vehicle** to internalize advanced process technologies and redeploy them to core products. A data-driven cycle—observation, hypothesis, countermeasure, and verification—eliminated a subtle plasma-damage-induced junction leakage and stabilized yield (~65% → ~80%).

Built on that foundation, the 0.25-μm VSRAM was mass-produced in 2001 and enabled the first camera phone, even though it initially shipped at ~30% yield before improving to 80–90%. At 0.18 μm, a trench-capacitor VSRAM was abandoned due to larger junction area and insufficient 90 °C retention, marking practical limits of 1T-1C-based pseudo-SRAM for mobile.

Strategically, stepping off commodity memory competition while retaining the acquired process/design/reliability know-how strengthened Epson's display driver, ASIC, and logic businesses. This case offers a concrete template for technology-transfer ramp-ups that prioritize *capability acquisition and reuse* over direct DRAM commercialization.

#### REFERENCES

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#### AUTHOR BIOGRAPHY

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