A Comparative Review of DRAM and FeRAM: The Boundary between Volatile and Non-Volatile Memory and Future Perspectives

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***Abstract*—Dynamic Random-Access Memory (DRAM) is the workhorse of volatile memory, while ferroelectric memories (FeRAM and FeFET) offer CMOS-compatible non-volatility. This paper reviews DRAM and FeRAM from technology scaling and reliability to system-level use. We summarize key metrics (speed, retention, endurance, and energy/bit) and discuss hybrid hierarchies that combine DRAM performance with FeRAM persistence.**

***Index Terms*—DRAM, FeRAM, FeFET, HfO2, retention, endurance, scaling, memory hierarchy.**

I. Introduction

Memory hierarchies are central to computing systems. DRAM remains the dominant volatile memory due to speed, density, and scalability [1], [2]. However, DRAM scaling faces limits as capacitors shrink; 3D DRAM concepts are explored to extend scaling [3].

In parallel, doped HfO_2 ferroelectrics enabled FeRAM and FeFET with CMOS-friendly integration [4], [5]. These offer non-volatility with fast switching but face polarization variability, endurance, and TDDB concerns.

This review contrasts DRAM and FeRAM at device and system levels and outlines hybrid use-cases. As an overview, Figs. 1 and 2 conceptually illustrate the trade-offs in access speed, retention, and write energy, which will be detailed in Sec. IV.

II. DRAM Technology and Scaling

DRAM scaling progressed via high-k dielectrics and either deep-trench or stacked capacitors. Maintaining sufficient cell capacitance while suppressing leakage below deep sub-20 nm nodes is challenging [1]. To extend scaling, 3D stacking and array layering are explored, though integration complexity and refresh overhead remain open concerns [3].

From a metrics viewpoint, DRAM provides sub-10 ns access, very low energy/bit for reads and writes, and effectively unlimited endurance (refresh-limited). Retention is short and necessitates periodic refresh [2].

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TABLE I
Representative metrics (order-of-magnitude, literature indications).

Tech.	Speed (ns)	Retention (s)	Endurance	Energy/bit
DRAM	≤ 10	$\sim 10^{-2}$ to 10^{-1}	$\geq 10^{16}$	10–100 fJ
FeRAM	≤ 50	$\geq 10^{5}$	10^{12}–10^{13}	10^{2}–10^{3} fJ

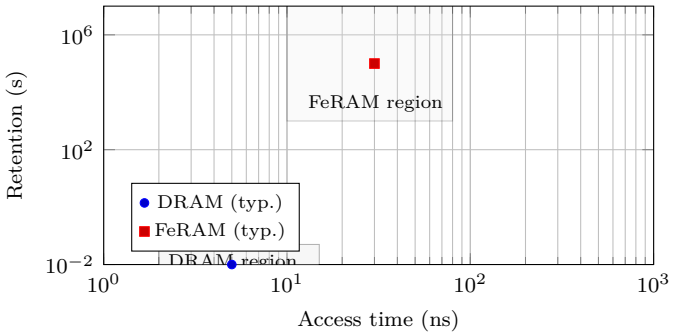

Fig. 1. Speed vs. retention trade-off. DRAM is faster but requires refresh, whereas FeRAM provides long retention at modest access times.

III. FeRAM Technology and Advances

The discovery of robust ferroelectricity in doped HfO_2 films enabled FeRAM and FeFET with CMOS-friendly back-end integration [4], [5]. Device-level challenges include polarization variability, endurance dispersion, and high-field reliability concerns (e.g., TDDB). System-wise, FeRAM/FeFET provide non-volatility with fast writes and low-voltage operation, making them attractive complements to DRAM [6], [7].

IV. Comparative Analysis: DRAM vs FeRAM

Table I summarizes representative literature values for DRAM and FeRAM. DRAM provides high speed and very low energy/bit but requires periodic refresh due to short intrinsic retention [1]–[3]. FeRAM offers non-volatility with retention beyond 10^5 s and endurance reported in the 10^{12}–10^{13} range for optimized HfO_2 stacks, typically at higher write energy per bit [4]–[7].

V. Hybrid Perspectives and Future Memory Hierarchies

Hybrid memory hierarchies aim to combine DRAM performance with FeRAM persistence. By placing FeRAM

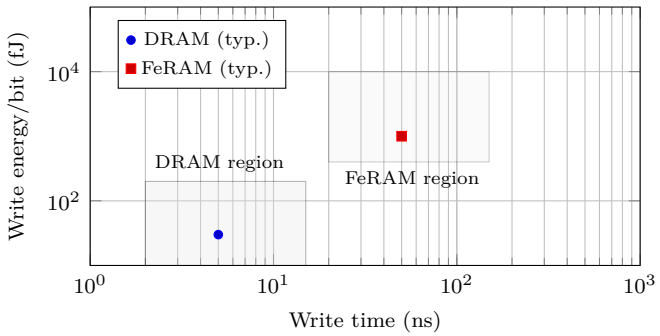

Fig. 2. Conceptual write energy versus write time. DRAM typically achieves lower energy at short write times; FeRAM writes cost more energy but persist without refresh.

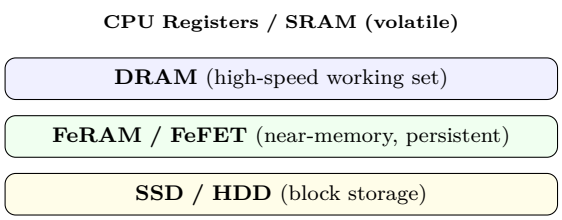

Fig. 3. Hybrid memory hierarchy where FeRAM near DRAM provides persistence and reduces refresh pressure.

near the controller or adjacent to DRAM, systems can reduce refresh energy, enable instant-on features, and accelerate checkpointing and recovery for critical state.

Benefits

- Reduced refresh overhead: cold pages and metadata can reside in FeRAM, cutting DRAM refresh traffic and standby power.
- Fast persistence: OS/app state can be checkpointed to FeRAM with μs–ms latency.
- Data resilience: FeRAM provides crash consistency for critical metadata and write-back buffers.

Constraints and trade-offs

- Endurance/variability: FeRAM endurance (10^{12}–10^{13} cycles) is high but below effective DRAM activity.
- Write energy/latency: typically higher than DRAM; bias read-mostly or cold data to FeRAM.
- Integration cost: ferroelectric layer/FeFET adds process and reliability risks (e.g., high-field stress).

System directions

- Intensity/retention-aware placement and migration.
- Refresh co-optimization for DRAM regions shadowed/backed by FeRAM.
- Controller/OS support for wear tracking, retention-aware placement, and error telemetry.

VI. Conclusion and Outlook

DRAM will continue to dominate volatile working memory due to speed, density, and ecosystem maturity. HfO2-based FeRAM/FeFET offers a CMOS-compatible non-volatile complement with fast access, though variability, endurance dispersion, and integration limits remain active topics [6], [7]. Hybrid hierarchies that pair DRAM for hot data with FeRAM for persistence can reduce refresh energy while enabling fast recovery paths.

Looking ahead, co-design across devices, controllers, and operating systems will be central: retention-aware placement, telemetry-driven reliability management, and low-latency persistence paths are promising directions to broaden deployment from embedded and edge to selected data-centric systems.

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