

④ MOSFET Scaling :- Over the past decades, the MOSFET has continually been scaled down in size; typical MOSFET channel lengths were once several micrometers, but modern ICs are incorporating MOSFET's with channel lengths of tens of nanometers. The reduction of the dimension of MOSFET is commonly referred as scaling. Intel began production of a process featuring a 32 nm feature size (with the channel being even shorter) in late 2009.

The difficulties with decreasing the size of the MOSFET has been associated with the semiconductor device fabrication process, the need to use very low voltages with poorer electrical performance (small MOSFET

exhibit higher leakage current & lower O/P resistance.

Reasons of MOSFET Scaling :-

- i) Make transistors smaller, which helps to pack more and more devices in a given chip area. The cost per integrated circuit. Smaller IC allows more chips per wafer, reducing the price per chip.
- ii) This result in a chip with the same functionality in a smaller area, or chips with more functionality in the same area, which is associated with Moore's Law.

There are two basic types of size reduction strategies —

- i) Full Scaling / Constant field scaling.
- ii) Constant voltage scaling.

To describe device scaling, we introduce a constant scaling factor ($S > 1$). All horizontal & vertical dimensions of the large size transistor are then divided by the scaling factor to obtain scaled device. It is seen that a new generation of manufacturing technology replaces the previous one about every two or three years & scaled factor is about (1.2 to 1.5).

It is easy to recognize that the scaling of all dimension by a factor of $S > 1$, leads to the reduction of the area occupied by the transistor by a factor of S^2 .

1) Constant field Scaling or In this scaling technique, it preserve the magnitude of internal electric field in the MOSFET, while the dimensions are scaled down by a factor of S .

Now, we can describe different parameters of MOSFET which is affected due to scaling

Quantity	Before Scaling	After Scaling
i) Channel Length	i) L	i) $L' = L/S$
ii) Channel Width	ii) W	ii) $W' = W/S$
iii) Gate oxide thickness	iii) t_{ox}	iii) $t_{ox}' = t_{ox}/S$
iv) Junction Depth	iv) N_j	iv) $N_j' = N_j/S$
v) power supply voltage	v) V_{DD}	v) V_{DD}/S
vi) Threshold voltage	vi) V_T	vi) $V_T' = V_T/S$
vii) Doping densities	vii) $\{ N_A, N_D \}$	vii) $\{ N_A' = S \cdot N_A, N_D' = S \cdot N_D \}$

Now,

$$1. C_{ox}' = \frac{\epsilon_{ox}}{t_{ox}'} = \frac{\epsilon_{ox}}{t_{ox}/S} = S \cdot \frac{\epsilon_{ox}}{t_{ox}} = S \cdot C_{ox}$$

$$C_{ox}' = S \cdot C_{ox}$$

$$2. \text{ Linear mode Drain Current } (I_D') = \frac{K_n}{2} \left[(V_{GS}' - V_T') \cdot V_{DS}' - \frac{V_{DS}^2}{2} \right]$$

$$= S \cdot K_n \cdot \frac{1}{S^2} \left[(V_{GS} - V_T) \cdot V_{DS} - \frac{V_{DS}^2}{2} \right]$$

$$= \frac{I_D(\text{lin})}{S} \quad \therefore I'_D(\text{linear}) = \frac{I_D(\text{lin})}{S}$$

Similarly, the saturation mode drain current is also reduced by the same scaling factor.

$$I'_D(\text{sat}) = \frac{K_n'}{2} (V_{GS} - V_T')^2 = \frac{S \cdot K_n}{2} \cdot \frac{1}{S^2} (V_{GS} - V_T)^2$$

$$= \frac{I_D(\text{sat})}{S}$$

$$I'_D(\text{sat}) = \frac{I_D(\text{sat})}{S}$$

Now, Consider the power dissipation of the MOSFET. The instantaneous power dissipated by the device (before scaling) is found as,

$$P = I_D \cdot V_{DS}$$

$$\text{Now, } P' = I'_D \cdot V'_{DS} = \frac{1}{S^2} \cdot I_D \cdot V_{DS} = \frac{P}{S^2}$$

$$P' = P/S^2$$

$$\text{Gate oxide Capacitance } (C_g) = W \cdot L \cdot C_{ox}$$

$$\text{Now, } C'_g = W' \cdot L' \cdot C_{ox}' = \frac{W}{S} \cdot \frac{L}{S} \cdot S \cdot C_{ox}$$

$$= \frac{W \cdot L \cdot C_{ox}}{S} = \frac{C_g}{S}$$

So, C_g is scaled down by a factor of S .

Constant Voltage Scaling \rightarrow In Constant field

Scaling strategies, power supply voltages & all terminal voltages be scaled down proportionally with the device dimensions. But the peripherals & interface circuitry may require certain voltage levels; for this reason Constant voltage scaling is usually preferred over full scaling.

So, in Constant voltage scaling, all dimensions of MOSFET are reduced by a factor of 's' but the power supply voltage & terminal voltages remain unchanged.

Here, doping densities must be increased by a factor of s^2 .

Quantity	Before Scaling	After Scaling
i) Dimensions	i) w, L, t_{ox}, α_j	i) Reduced by factor s .
ii) Voltages	ii) V_{DD}, V_T	ii) Remain Unchanged.
iii) Doping Densities.	iii) N_A, N_D	iii) Increased by s^2
iv) Oxide Capacitance	iv) C_{ox}	iv) $C_{ox}' = s \cdot C_{ox}$
v) Drain Current	v) I_D	v) $I_D' = s \cdot I_D$
vi) Power Dissipation	vi) P	vi) $P' = s \cdot P$
vii) Power Density	vii) P/Area	vii) $P'/\text{Area}' = s^3 \cdot P/\text{Area}$

$$\text{So, } I_D'(\text{lin}) = K_n' \left[(V_{GS}' - V_T') \cdot V_{DS} - \frac{V_{DS}^2}{2} \right]$$

$$= S \cdot K_n \left[(V_{GS} - V_T) \cdot V_{DS} - \frac{V_{DS}^2}{2} \right]$$

$$I_D'(\text{lin}) = S \cdot I_D(\text{lin})$$

NOW,

$$I_D'(\text{sat}) = \frac{K_n'}{2} (V_{GS}' - V_T')^2 = \frac{S \cdot K_n}{2} (V_{GS} - V_T)^2$$

$$I_D'(\text{sat}) = S \cdot I_D(\text{sat})$$

power dissipation of MOSFET

$$P' = I_D' \cdot V_{DS} = (S \cdot I_D) \cdot V_{DS} = S \cdot P$$

$$P' = S \cdot P$$

Finally the power density (power dissipation per unit area) is found to increase by a factor of S^3 ; after constant voltage scaling.