

1.1) Evolution of VLSI Technology

Michael Faraday was the first person to observe a semiconductor effect in 1833. Faraday observed that the electrical resistance of silver sulphide (Ag_2S) decreases with temperature.

⟨ Silver Sulphide is a dense black solid that is insoluble in all solvents. It features a covalent bond between silver and sulfur. ⟩

During the first half of the twentieth century, electronic circuits used large, expensive, power-hungry and unreliable vacuum tubes.

On 1947, John Bardeen, Walter Brattain built the first point contact transistor at Bell Lab under the supervision of William Shockley.

BJT were more reliable, less noisy and more power efficient, smaller, cheaper to manufacture.

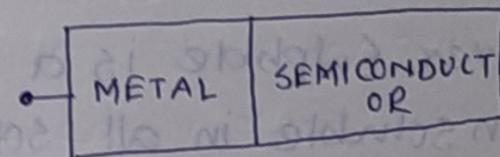
⟨ The invention of the transistor earned the Nobel prize in physics in 1956. ⟩

Semiconductor devices have been studied for over 125 years. To date, we have about 60 major devices, with over 100 device variations related to them.

However, all these devices can be constructed from a small no of device building blocks.

figure (a) shows, the metal Semiconductor interface.

This building block was the first semiconductor device

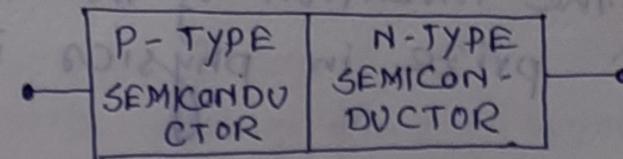


(a)

ever studied (1874). This interface can be used as a rectifying contact. { Rectifying Contact allow flow of current in one direction, while ohmic contact allow current in both direction with a negligible small voltage drop. }

for example → using a rectifying contact at the gate & two ohmic contact at the source and drain, can form a MESFET (an important microwave device).

The p-n junction is the key building block for most semiconductor devices.

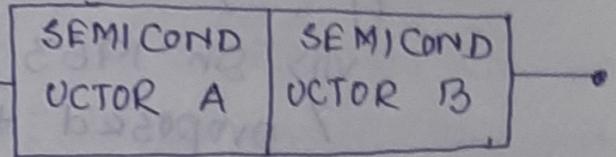


(b)

Simply it acts as a switch.

By combining two p-n junction form p-n-p or n-p-n bipolar transistor. If you combine three p-n junction, it forms p-n-p-n structure; it is a switching device called Thyristor. (mainly used in high current flow and controlled current flow applications.) [developed by Ebers in 1952]

The third building block is the heterojunction interface. For example

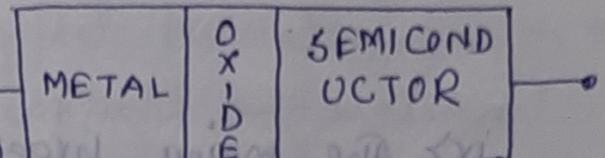


→ Gallium Arsenide (GaAs)

and Aluminium Arsenide (AlAs) to form a hetero-junction. Heterojunctions are the key components for high speed and photonic devices.

It's a Metal Oxide Semiconductor (MOS) structure.

MOSFET is the most important device for advanced integrated



*> After the invention of Transistor (in 1947)



i) Thyristor invented by 'Ebers' in 1952.

ii) Solar cell developed by 'Chapin' in 1954.

iii) 'Kroemer' proposed heterojunction BJT to improve transistor performance in 1957.

iv) 'Tsaki' developed Tunnel diode in 1958. < associated with tunneling

phenomenon are important for ohmic contact and carrier transport within through thin layers>

v) MOSFET reported by Kahng and Atalla in 1960. < with gate length 20 nm>

vi) At the beginning of 1960, Jack Kilby of Texas Instrument, created first

prototype of IC.

vii) In 1963, Kroemer, Alferov and Kazaninov proposed the heterostructure LASER.

viii) { In the next three years, three important microwave devices were invented.
a) first Transferred Electron Device (Gunn diode) invented by Gunn in 1963.
b) In 1965, IMPATT diode by Johnston.
c) MESFET invented by 'Mead' in 1966.

{ A key device of monolithic microwave IC (MMIC) }

ix) The major breakthrough came in 1963, with the invention of CMOS by 'Wannam & Sot'.

{ It's a combination of PMOS & nMOS Connected in Series. }

x) An important Semiconductor memory device was invented by 'Kahng & Sze' in 1967.

{ It was the non-volatile Semiconductor memory, which can retain its stored information even the power supply is switched-off }

{ → It is quite similar to MOSFET, the major difference is the addition of the floating gate. }

{ during that period, it became the dominant memory element for cellular phone, notebook Computer etc. }

xii) The charged couple device (CCD) < movement of electric charges within the device. It can be treated as CCD sensor, which is mainly used in the digital & video cameras → for taking images and recording videos through photoelectric effect. It is used for converting the captured light into digital data. >

Was invented by 'Boyle & Smith' in 1970.

xiii) In 1980 'Minura' developed MODFET

(Modulation doped field effect transistor), with the proper selection of the heterojunction material, the MODFET expected to be the fastest FET.

* Historical perspective :-

The Bipolar transistor technology was developed early on and applied to the first mainframe computers in 1960's; CKT speed was important so it does. However a large power dissipation limit their integration level to about 10^4 CKT per chip. This integration level is quite low compare to the today's VLSI tech. standard.

First MOSFET was fabricated in 1960 by Kahng & Atalla. During 1960 to 1970 both n-channel & p-channel MOSFET widely used along with bipolar transistor.

The major advantage of MOSFET device is that it had higher layout density & relatively simple to fabricate, but it suffers

from large standby power dissipation & hence limits the level of integration on a chip.

The major breakthrough came in 1963, with the invention of CMOS by 'Nawans & Sah'. CMOS typically consists of n-channel & p-channel MOSFET connected in series. There is negligible standby power dissipation. Significant power is dissipated during switching of the circuit.

Now, engineer's able to integrate millions of transistors in a single chip & it is readily air coolable.

Another advantage of CMOS ORT is full rail to rail logic swing, which improves the noise margin & makes a CMOS chip easier to design.

Since, CMOS tech available, then it became popular technology for digital circuits and bipolar tech used in RF and analog circuits only.

Another technology that has emerged very recently, the BiCMOS technology makes use of Bipolar and CMOS devices on the same chip. Usually most of the logic in BiCMOS device is CMOS, while the Bipolar devices are used for on-chip and off-chip drivers. These bipolar drivers are capable of driving much higher loads without the cost of speed.

BiCMOS is faster as compared to CMOS but fabrication cost increases.

In IC fabrication processes either Silicon or gallium Arsenide technologies.

GaAs technology is slowly advancing and has found suitable market in military and aerospace areas.

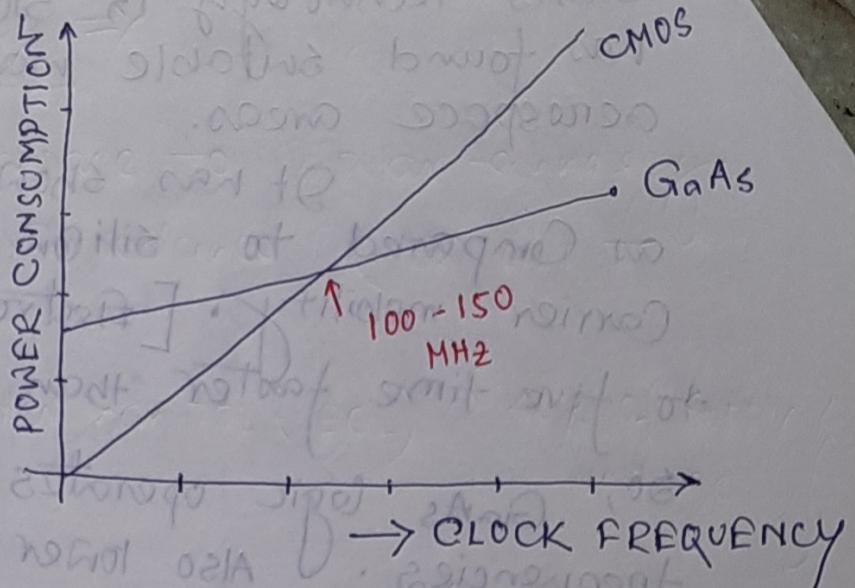
It has shown better performance as compared to silicon due to its higher carrier mobility. [electrons in GaAs travel four to five times faster than in silicon]

so, GaAs logic operates at much higher clock frequencies; also lower electric field is necessary to achieve maximum mobility when compared to CMOS. But in GaAs tech, there is no native oxide to act as an insulator (just like SiO_2 in silicon tech) to produce simple MOS style logic elements. Furthermore holes in GaAs move comparatively slower speed than silicon which makes complementary style Ckt operation inefficient.

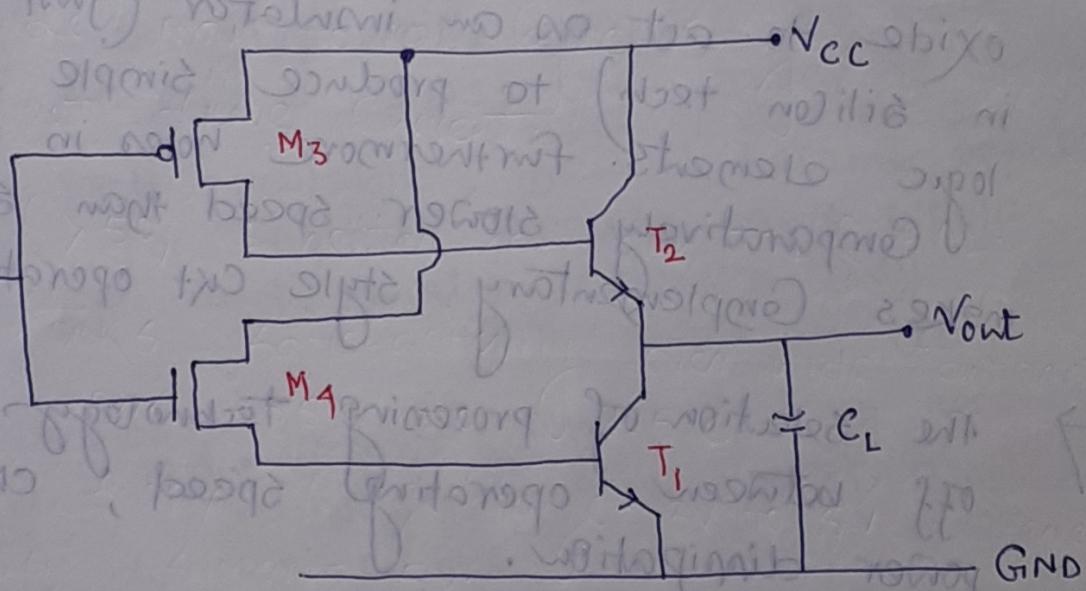
\Rightarrow The selection of processing technology is a trade off between operating speed, chip area & power dissipation.

CMOS has major advantage of high density and lower power dissipation. Compared to the other processing technologies, speed is the limiting factor. In GaAs tech though the speed is high but power dissipation largely increased

CMOS technology has the advantage below 100-150 MHz clock frequency range. But it is observed that GaAs has a clear advantage in terms of speed power product for low voltage applications.



The BiCMOS Inverter :-



An BiCMOS inverter consists of two BJT T_1 & T_2 with one nMOS (M_1) & pMOS (M_3) which are in enhancement mode. operations \rightarrow

if when $V_{in} = 0V$; M_1 is off & T_1 is non-conducting but M_3 is in ON condition & T_2 Conducting & act as a current source to charge load capacitor to get $V_{out} = V_{cc}$.

ii) When $V_{in} = V_{CC} = 5V$; M_2 is ON Condition & T_1 is Conducting but M_3 is OFF & T_2 is not Conducting

As T_1 is Conducting, the load capacitance discharge through T_1 to make V_{out} to become OV.

This ckt has following advantages,

i) High i/p impedance & low o/p impedance.

ii) High Current operation capabilities.

Main disadvantages is, \rightarrow Low noise margin.

max o/p voltage is approximately $(V_{CC} - 0.7V)$ & min logic o/p voltage is 0.7V. (because $V_{BE} = 0.7V$)

This low o/p voltage (0.7V) is very close to the threshold voltage of n-channel MOSFET. So if there are cascode connection, create problem.

< Home task \rightarrow Design Bi CMOS NAND gate >

- Advantages of CMOS technology \Rightarrow
- i) Low power dissipation Compare to Bipolar technology.
 - ii) CMOS offer high input Impedance & low output Impedance.
 - iii) High noise margin (better than TTL & ECL) { 40% of Supply voltage }
 - iv) High packing density
 - v) Threshold voltage of CMOS is highly Scalable
 - vi) Bidirectional Capability (Drain & Source are interchangeable)
 - vii) It provides rail to rail logic swing
 - viii) Low output drive current.
 - ix) Fanout (> 50) is better than both TTL & ECL.
 - x) CMOS works satisfactorily over wide temperature range from -155°C to 125°C .
 - xii) Nominal supply voltage range 3V to 5V ; whereas TTL only supports 5V.

Disadvantages

- i) Average propagation delay time (1 to 200 ns) is worst Compare to TTL & ECL logic families.