(A)

Threshold Voltage

The threshold voltage (V_{th}) is the voltage at which there are sufficient electrons in the inversion layer to make a low resistance conducting path between the source & drain of the MOSFET.

If the gate voltage is below the threshold voltage, the transistor is turned off & ideally there is no current from the drain to source. But practically there is a very small amount of current (even for gate biases below threshold) will flow, called sub-threshold leakage.

Body Effect ⇒ The body effect describe the changes in the threshold voltage by the change in 'V_{SB}' (source to bulk voltage).

For an n-channel enhancement type MOSFET, the threshold voltage is computed according to the 'Shichman – Hodges' model.

$$\boxed{V_{TN} = V_{TO} + \gamma\left(\sqrt{|V_{SB} + 2\phi_F|} - \sqrt{2\phi_F}\right)}$$

here, V_{TN} = Threshold voltage, when substrate bias is present.

V_{SB} = Source to body/substrate biasing voltage.

φ_F = Surface potential.

V_{TO} = Threshold voltage for zero substrate bias.

$$\gamma = \left(t_{ox}/\epsilon_{ox}\right) \cdot \sqrt{2q \cdot \epsilon_{si} \cdot N_A} \quad \Big\{ \text{Body effect parameter.}$$

So, using the formulae, V_{TN} is directly proportional to γ and t_{ox}.

Thus, for thinner oxide thickness, lower the threshold voltage. It seems to be the improvement, but for the thinner oxide thickness, higher the subthreshold leakage current.

So, consequently for 90 nm gate oxide thickness was set at 1nm to control the leakage current.

This kind of tunneling is called 'Fowler-Nordheim' tunneling.

$$\boxed{I_{fn} = C_1 \cdot W \cdot L \cdot (E_{ox})^2 \cdot e^{-E_0/E_{ox}}}$$

here,

C_1, E_0 are constant.

E_{ox} = electric field constant across the gate oxide.

As we have seen that, oxide thickness affect the threshold voltage, Temparature has also an effect on the threshold voltage.

We know that,

$$\phi_F = \left(\frac{KT}{q}\right) \ln\left(\frac{N_A}{n_i}\right)$$

K = Boltzman Constant

T = temparature.

So, surface potential has a direct relationship with the temparature.

for a change of 30°C, this result in significant variation from the 500mV design parameter. (used in 90nm tech)