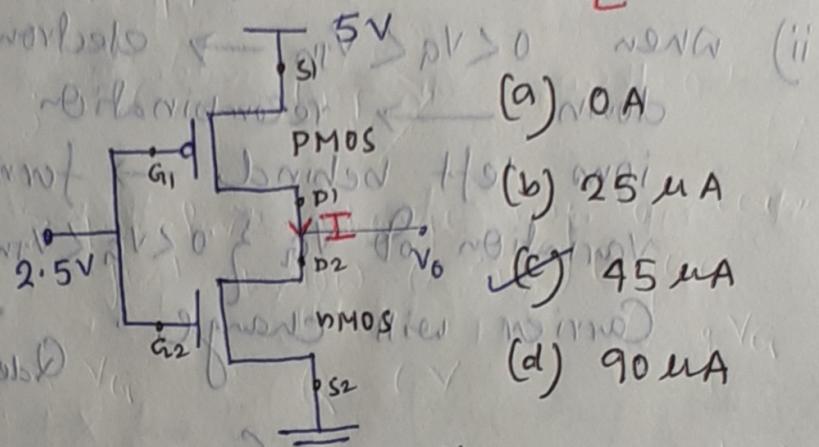


2) In the CMOS inverter, $K_n = K_p = \mu_n C_{ox} \cdot \frac{W_p}{L_p} = 10 \mu A/V^2$
 and, $|V_{Th,n}| = |V_{Th,p}| = 1 V$ find current I.

[Gate 2007]



(a) 0 A

(b) 25 μA

(c) 45 μA

(d) 90 μA

⇒ ASV, both the transistor
 is in saturation

→ Current will be Constant.

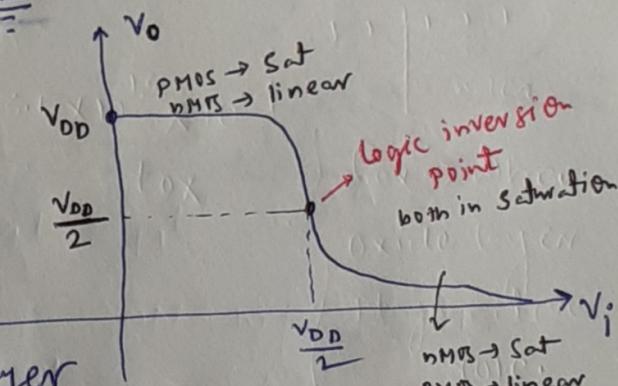
$$I_{D1} = I_{S1} \quad (I_{G1} = 0 A)$$

because of Si_3O_2 layer

= Saturation Current of PMOS & NMOS respectively.

$$I_{D1} = \frac{1}{2} \mu_p \cdot C_{ox} \cdot \frac{W_p}{L_p} (V_{GS} - V_{Th,p})^2$$

$$= \frac{40 \mu A/V^2}{2} \times (V_{G1} - V_S - V_{Th,p})^2 = \frac{1}{2} \times 40 \times 10^{-6} (2.5 - 1)^2 = 45 \mu A$$



84.7 A MOSFET in saturation has a drain current of 1mA for $V_{DS} = 0.5V$. The channel length modulation Co-efficient is $0.05 V^{-1}$. The output resistance (r_o) of the MOSFET is, [Gate 2015]

$$\Rightarrow \gamma = 0.05 V^{-1} \quad (mV - \text{opV}) \approx \frac{1}{C} = (mV)^{-1} \text{ ID}$$

$$(mV - 0.5V - I_D) = \frac{1}{2} \times \mu_n \cdot C_o \cdot \frac{W}{L} (V_{GS} - V_{Th})^2 (1 + 2V_{DS})$$

When CLM Considered, then only I_D depends upon V_{DS} . < when MOSFET in saturation >

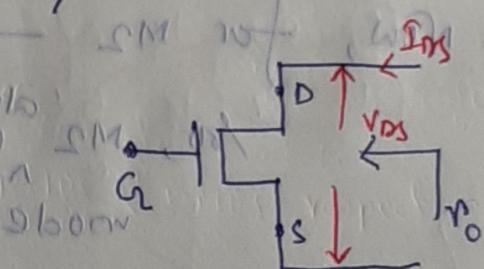
$$\Rightarrow I_D = \frac{1}{2} K_n (V_{GS} - V_{Th})^2 (1 + 2V_{DS})$$

$$= K_n' (V_{GS} - V_{Th})^2 (1 + 2V_{DS})$$

Here, $r_o = \frac{\partial V_{DS}}{\partial I_D} = \frac{1}{K_n' (V_{GS} - V_{Th})^2 (1 + 2V_{DS})} = \frac{1}{I_D \times 2} = 50 \Omega$

When CLM not considered $= I_D$

$$(mV - 0.5V - 0) = \frac{1}{10^{-3} \times 0.05} = 20 \text{ k}\Omega = 20 \times 10^3 \Omega$$

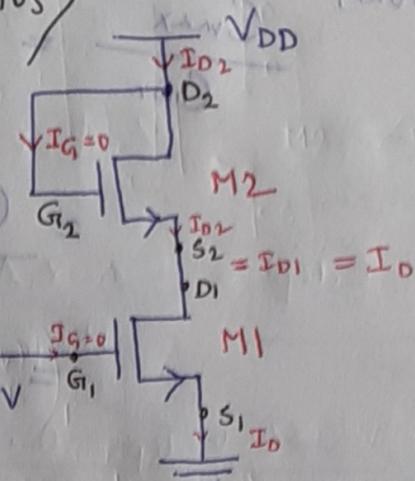


Q5) $K_n = \mu n C_{ox} \left(\frac{W}{L} \right) = 1 \text{ mA/V}^2$; $V_{Th} = 1 \text{ V}$. Assume that $\gamma = 0$ & body is shorted to source. The min supply voltage (V_{DD}) needed to ensure that M_1 operates in saturation mode \rightarrow [Gate 2015]

~~< Both M_1 & M_2 enhancement type MOS>~~

\Rightarrow

In Case of nMOS
always, $V_{DD} > V_S$.



Here, $\gamma = 0$ so,

$$I_D = \frac{1}{2} K_n (V_{GS} - V_{Th})^2 (1 + \gamma V_{DS})$$

$$\Rightarrow I_D = \frac{1}{2} K_n (V_{GS} - V_{Th})^2 \quad \left\{ I_D \rightarrow \text{is independent of } V_{DS} \right\}$$

and, $V_{SB} = 0$; (body effect not considered)

then, $V_{Th} = \text{Constant} = 1 \text{ V}$. And

Let, M_1 in saturation, then \rightarrow

$$I_{D1} (\text{for } M_1) = \frac{1}{2} K_n (V_{GS} - V_{Th})^2$$

$$(20 \text{ VR} + 1) \left(2 \text{ V} - 1 \text{ V} \right)^2 = \frac{1}{2} \times 1 \left(V_{G1} - V_{S1} - V_{Th} \right)^2$$

$$= \frac{1}{2} \times 1 \left(2 - 0 - 1 \right)^2 = \frac{1}{2} \text{ mA}$$

As, $I_{D1} = I_{D2} = \frac{1}{2} \text{ mA}$

Now, for $M_2 \rightarrow$ there $V_{DS} = V_{GS}$ $\left\{ \begin{array}{l} V_{DS} > V_{GS} - V_{Th} \\ \text{to operate in} \\ \text{saturation} \end{array} \right.$
so, M_2 always operates in saturation mode.

$$I_{D2} = \frac{1}{2} K_n (V_{GS2} - V_{Th})^2 = \frac{1}{2} K_n (V_{GS2} - V_{Th})^2$$

$$\Rightarrow \frac{1}{2} = \frac{1}{2} \times 1 \text{ mA/V}^2 \times \left(V_{GS2} - V_{Th} \right)^2 \quad \left\{ \begin{array}{l} \text{as } V_{Th} \text{ positive} \\ \text{and } V_{GS2} \text{ positive} \end{array} \right.$$

$V_{GS2} > V_{DS} - V_{Th}$
 \rightarrow always true

here, $V_{S2} = V_{D1}(\text{min}) = V_{GS1} - V_{Th} = 2 - 1 = 1 \text{ volt}$

$$\frac{1}{2} \text{ mA} = \frac{1}{2} \times 1 \left(\frac{V_{DD} - 1}{2} - 1 \right)^2$$

$$\Rightarrow (V_{DD} - 2)^2 = 1 \Rightarrow V_{DD} = 1 + 2 = 3 \text{ volt (Ans)}$$

Q6) In the CMOS inverter circuit, both T_1 & T_2 are enhancement type MOS having $V_{Th} = 2 \text{ V}$. [Gate 2002]

Statement 1: T_1 Conducts when $V_i \geq 2 \text{ V}$

Statement 2: T_1 always in saturation, when $V_o = 0 \text{ V}$.

(a) only statement 1 is true (b) only statement 2 is true.

(c) Both are true (d) Both are false

Here,

$$V_{TN} = 2 \text{ V}$$

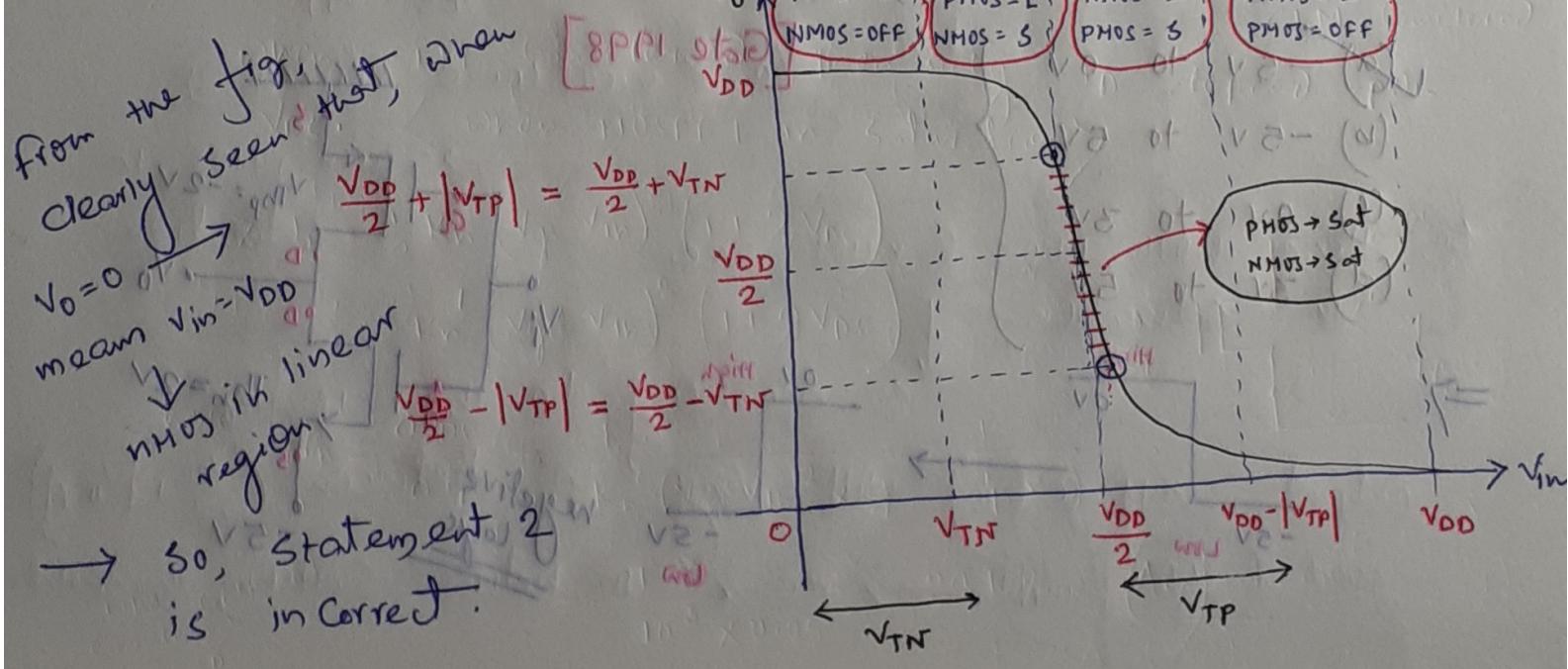
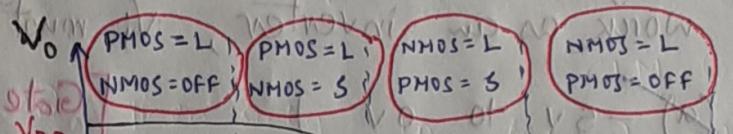
$$\text{if } V_{TP} = -2 \text{ V} \quad |V_{TP}| = 2 \text{ V}$$

In Case of nMOS,

$$V_{GS} > V_{TN} \rightarrow \text{nMOS}$$

Conduct

So, T_1 Conducts, when $V_i \geq 2 \text{ V}$ Statement 1 Correct.



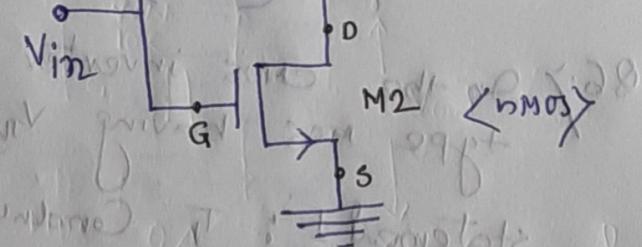
Q7) Here M_1 & M_2 are equally sized. The device M_1 is in the linear region if,

Here, $V_{Thn} = |V_{Thp}| = 1V$
and, $I_{Ln} = I_{Up}$

[Gate 2012]

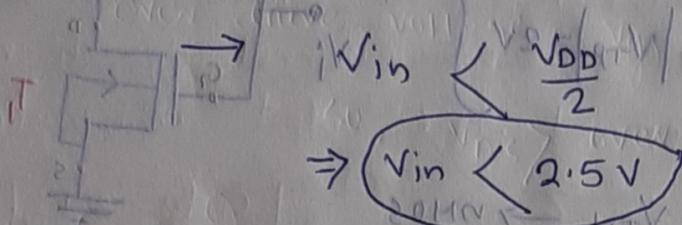
$$5V = V_{DD}$$

- (a) $V_{in} < 1.875V$
- (b) $1.875 < V_{in} < 3.125V$
- (c) $V_{in} > 3.125V$
- (d) $0 < V_{in} < 5V$



\Rightarrow Equal size, so, $\left(\frac{W}{L}\right)_n = \left(\frac{W}{L}\right)_p$

According to the question $\rightarrow M_1$ transistor means PMOS should be in linear region $\rightarrow i_D$ (i_{in}) should be in between 0 to $\frac{V_{DD}}{2}$ \rightarrow according to the fig in the previous page.

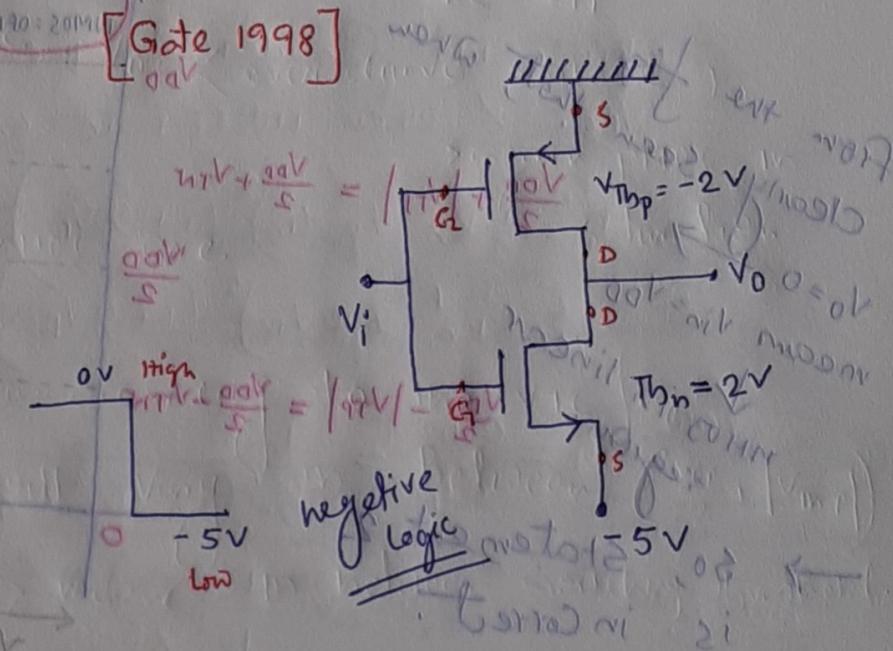


According to option (a) is Correct.

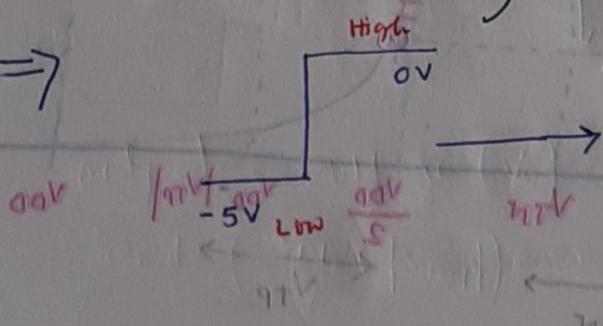
Q8) V_{Th} for each transistor in the fig is $2V$. For this circuit to work as an inverter, V_i must take the values, \rightarrow

- (a) $-5V$ to $0V$
- (b) $-5V$ to $5V$
- (c) $0V$ to $3V$
- (d) $3V$ to $5V$

[Gate 1998]



\Rightarrow



negative logic

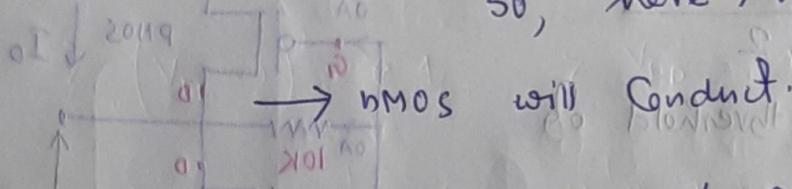
Case 1

[0 to 5V step]

$V_{in} = 0V$ (high)

$$0V \text{ NMOS: } V_{gs} = V_g - V_s = V_{in} + 5 = 0 + 5 = 5V$$

$$\text{so, here } V_{gs} > V_{Th,n} \quad \left\{ V_{Th,n} = 2V \right\}$$



$$0V \text{ PMOS: } V_{gs} = V_g - V_s = V_{in} - 0 = 0V$$

$$\text{so, here } V_{gs} < V_{Th,p} \rightarrow \text{Cut-off}$$

$$\text{so, } A_O = 1011 \text{ (1011)} \Rightarrow I_D = 0A$$

so, → In this Case

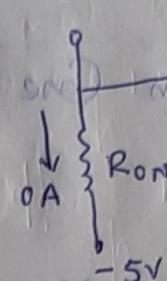
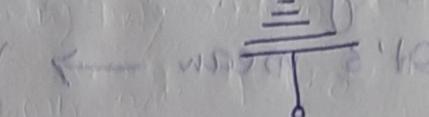
$$V_{in} = 0V$$

$$V_D = -5V$$

$$0V = 0V$$

act as inverter

$$20V = 20V$$



Case 2

$V_{in} = +5V$ (low)

$$\text{NMOS: } V_{gs} = V_g - V_s = V_{in} + 5 = -5 + 5 = 0V$$

$$0V - 20V = -20V \quad \text{here } V_{gs} < V_{Th,n}$$

→ NMOS in cut-off region (OFF)

$$0V - 20V =$$

$$I_D = 0mA$$

$$\text{Operation: PMOS: } V_{gs} = V_g - V_s = V_{in} - 0 = -5V$$

$$\text{so, here } V_{gs} > V_{Th,p}$$

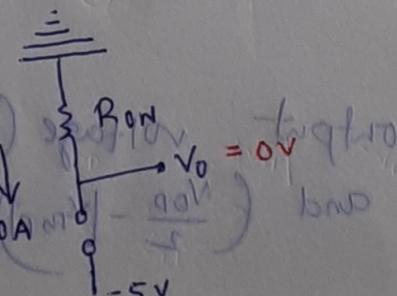
either Linear or Saturation

so, → In this Case

$$0V + 20V = 20V \quad \text{act as inverter}$$

$$0V = 0V$$

$$-5V = -5V$$



89. Find out the value of V_{out} of the following circuit.

- \Rightarrow
- (a) $0V$
(b) $\frac{|V_{Thn}| + |V_{TpP}|}{2}$

[Gate 2016]

(c) switching threshold of inverter.

- (d) V_{DD}

\Rightarrow As, Gate Current of both MOS = OA \rightarrow so current through $10\text{ k}\Omega$ resistance will be OA.

It's mean $\rightarrow V_{GD}(\text{PMOS}) = V_{GD}(\text{nMOS}) = 0 \text{ volt}$.

In Case of nMOS \rightarrow

$$V_{DS} = V_{GS}$$

$$\text{Over drive voltage} = V_{GS} - V_{Thn}$$

so, $V_{DS} > \text{over drive voltage}$

In Case of PMOS \rightarrow

$$\text{over drive voltage} = V_{GS} - V_{Tp}$$

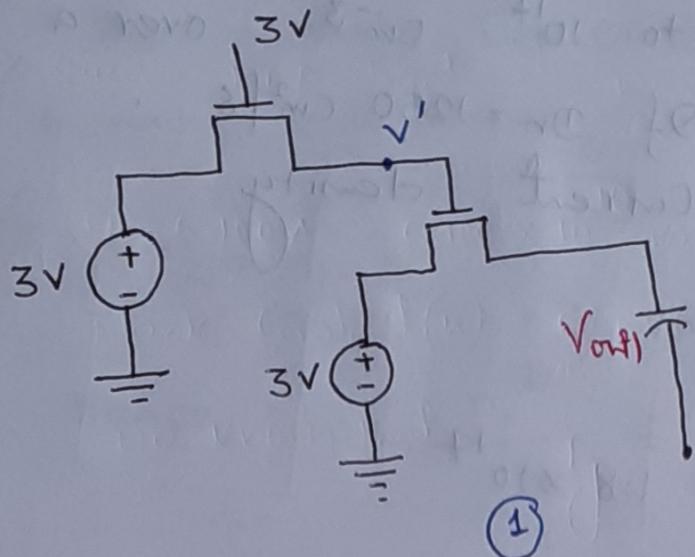
$$= V_{DS} - V_{Tp}$$

Here $V_{DS} < \text{over drive voltage}$

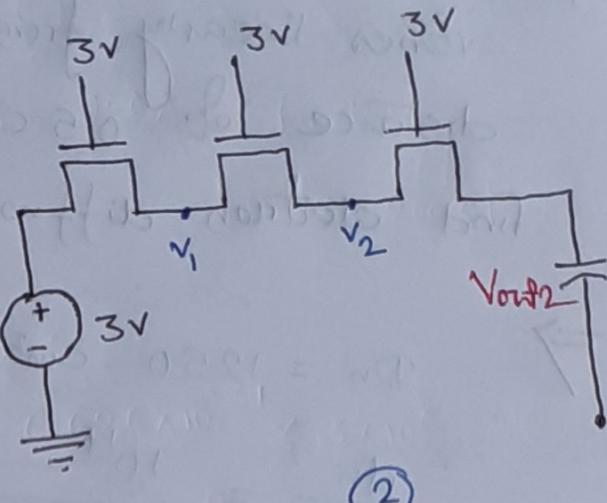
so, Here both PMOS & nMOS are in saturation \rightarrow again PMOS in saturation

so, according to the NTC fig
 V_{DS} between $(\frac{V_{DD}}{2} + |V_{Thn,p}|)$
and $(\frac{V_{DD}}{2} - |V_{Thn,p}|)$ \rightarrow means in between switching threshold.

Q1.7 $V_{TH} = 0.6V$; find V_{out1} & V_{out2} .



(1)



(2)

$$\Rightarrow V_{TH} = 0.6V \quad ; \quad V_{SB} = 0V \quad \text{and} \quad I = 0$$

from fig 1 $\rightarrow V' = V_G - V_{TH} = 3 - 0.6 = 2.4V$

$$\begin{aligned} \text{&} V_{out1} = V_G - V_{TH} &= V' - V_{TH} \\ &= 2.4 - 0.6 \\ &= 1.8 \text{ volt (Am)} \end{aligned}$$

from fig 2 \rightarrow

$$V_1 = V_2 = V_G - V_{TH} = 3 - 0.6 = 2.4 \text{ volt}$$

$$V_{out2} = 2.4 \text{ volt (Am)}$$

$$Q4) V_{TN} = 1.2V ; K_n = 0.5 \text{ mA/V}^2 ; \gamma = 0$$

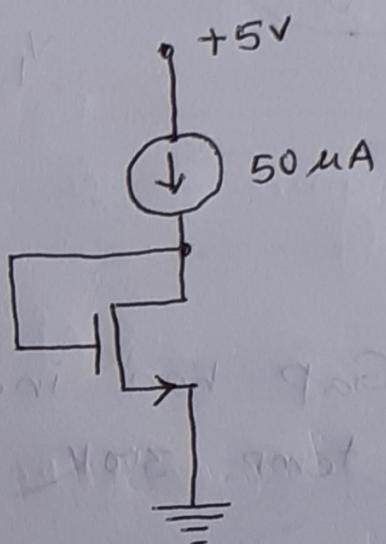
Find V_{DS}

\Rightarrow

$$I_D = K_n [V_{GS} - V_{TN}]^2 [1 + 2V_{DS}]$$

$$\Rightarrow 50 \times 10^{-6} = 0.5 \times 10^{-3} [V_{GS} - 1.2]^2 [1 + 2V_{DS}]$$

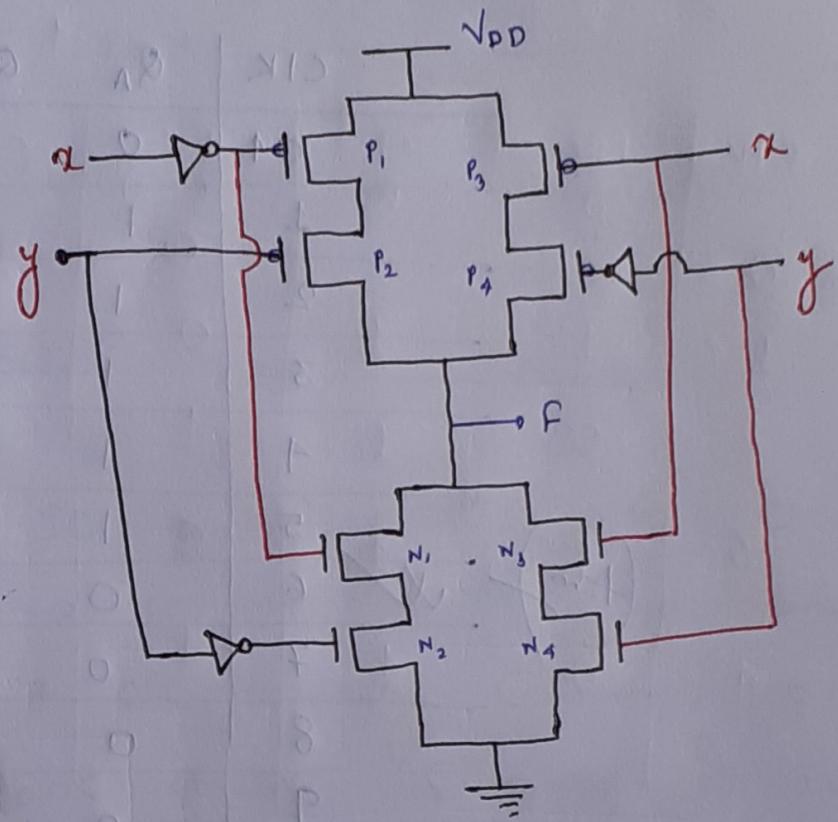
$$\Rightarrow V_{GS} = 1.52 \text{ volt.}$$



According to the figure, $V_{GS} = V_{DS}$

$$\therefore V_{DS} = 1.52 \text{ volt } (\text{Ans})$$

Q20) find logic implemented by the given ckt.



X	Y	P ₁	P ₂	P ₃	P ₄	N ₁	N ₂	N ₃	N ₄	F
0	0	OFF	ON	ON	OFF	ON	ON	OFF	OFF	0
0	1	OFF	OFF	ON	ON	ON	OFF	OFF	ON	1
1	0	ON	ON	OFF	OFF	OFF	ON	ON	OFF	1
1	1	ON	OFF	OFF	ON	OFF	OFF	ON	ON	0

→ 'F' denote X-OR function.

Q11) $V_T = 1V$ given $\mu_n C_{ox} = 120 \mu A/V^2$ & $I_D = 0$ for $V_{GS} = 0$

find $\frac{W_2}{W_1}$.

Assuming, $L_1 = L_2 = 1 \mu m$.

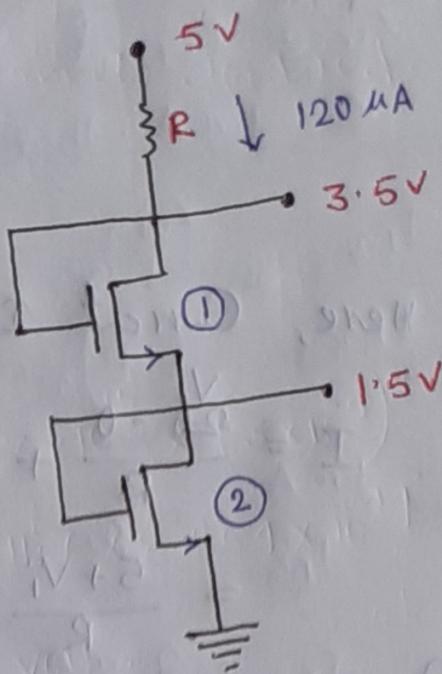
\Rightarrow Both are in saturation,

$$\therefore \mu_n C_{ox} \cdot \frac{W_1}{2L_1} (V_{GS1} - V_T)^2$$

$$= \mu_n C_{ox} \cdot \frac{W_2}{2L_2} (V_{GS2} - V_T)^2$$

$$\Rightarrow \frac{W_2}{W_1} = \frac{(V_{GS1} - V_T)^2}{(V_{GS2} - V_T)^2} \stackrel{(no)}{=} \frac{(2-1)^2}{(1.5-1)^2} = \frac{1}{0.5^2} = 4$$

$$\Rightarrow \frac{W_2}{W_1} = 4 \text{ (Ans)}$$



Q7.) $V_{TH} = 2V$; $I_D = 4mA$ when $R_D = 1K$. So

$R_D = 4K \rightarrow$ find I_D .

$$\Rightarrow I_D = K (V_{GS} - V_{TH})^2$$

$$\therefore 4mA = K (V_{GS} - 2)^2$$

Now,
 $V_{GS} = 10 - 4 \times 1 = 6V$

$$\therefore 4mA = K (6-2)^2 \quad ; \quad K = \frac{1}{4}$$

when, $R_D = 4K \rightarrow V_{GS} = 10 - 4I_D$

$$I_D = \frac{1}{4} (10 - 4I_D - 2)^2$$

$$\Rightarrow I_D = 2.8mA, 1.4mA$$

$$\therefore I_D = 1.4mA \quad (\underline{\text{Ans}})$$

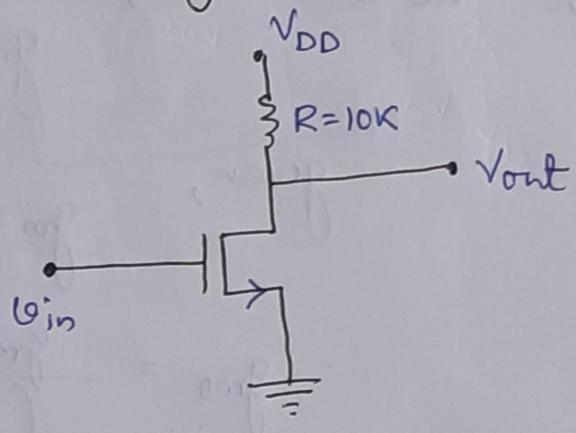
$\left. \begin{array}{l} I_D \text{ can't be } 2.8mA \\ \text{then, } V_{GS} \text{ become negative.} \end{array} \right\}$

Q97 Assume $\frac{W}{L} = 2$; $V_{DD} = 2.0$ volt .

$$m_n C_x = 100 \mu A/V^2 \text{ and } V_{Th} = 0.5 \text{ volt}$$

The transistor M₁ switches from saturation region to linear region , when V_{in} is greater than , →

- (a) 1.5
- (b) 1.6
- (c) 1.7
- (d) 1.8



for saturation ,

$$\begin{aligned} I_D &= m_n C_x \cdot \frac{W}{2L} (V_{GS} - V_{Th})^2 && \left. \begin{array}{l} \text{at the} \\ \text{edge of} \\ \text{saturation} \end{array} \right\} \\ &= \frac{1}{2} \times 100 \times 10^{-6} \times 2 \times (V_{out})^2 \\ &= 100 \times 10^{-6} \times (V_{out})^2 \quad \text{--- (i)} \end{aligned}$$

Now, KVL in outer loop we get , →

$$V_{DD} = I_D \times 10k\Omega + V_0 \quad \text{--- (ii)}$$

From eqn. (i) and (ii) we get ,

$$2 = 100 \times 10^{-6} \times (V_{out})^2 \times 10 \times 10^3 + V_{out}$$

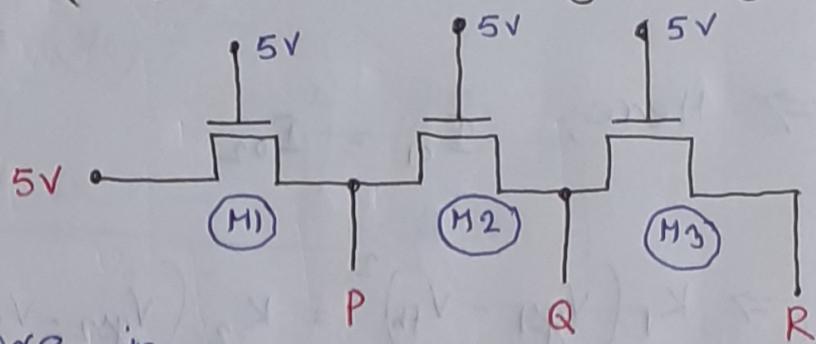
$$\Rightarrow \sqrt{V_{out}^2} + V_{out} - 2 = 0 ; \quad V_{out} = 1 \text{ volt}$$

$$V_{DS} = V_{GS} - V_{Th} ; \quad V_{outf} = V_{in} - V_{Th}$$

$$\Rightarrow V_{in} = V_{out} + V_{Th} = 1 + 0.5$$

$$= 1.5 \text{ volt} \quad (\text{Ans})$$

Q5) In the pass transistor logic, nMOS transistors are identical & $V_{TN} = 1V$. Ignoring body effect, find P, Q & R.



\Rightarrow Assuming all nMOS are in saturation.

$$V_{DS} \geq V_{GS} - V_{TH}$$

for M1,

$$5 - V_P \geq 5 - V_P - 1$$

$$\Rightarrow 5 - V_P \geq 4 - V_P \quad \xrightarrow{\text{Saturation}} \text{Saturation (valid)}$$

$$I_{D1} = K (V_{GS} - V_{TH})^2 = K (4 - V_P)^2 \quad \dots \dots \textcircled{i}$$

for M2

$$I_{D2} = K (5 - V_Q - 1)^2 = K (4 - V_Q)^2 \quad \dots \dots \textcircled{ii}$$

$$\text{As, } I_{D1} = I_{D2} \quad \xrightarrow{\text{K}(4 - V_P)^2 = K(4 - V_Q)^2}$$

$$\Rightarrow V_P = V_Q = 4 \text{ volt}$$

Similarly,

$$I_{D2} = I_{D3} \quad \xrightarrow{V_Q = V_R = 4 \text{ volt}}$$

$$\therefore V_P = V_Q = V_R = 4 \text{ volt} \quad (\text{Ans})$$

Q6.) Both T_1 and T_2 having threshold voltage = 1 V
 $K_1 = 36 \text{ MA/V}^2$; $K_2 = 9 \text{ MA/V}^2$; find V_o .

\Rightarrow Here, $I_{o1} = I_{o2}$

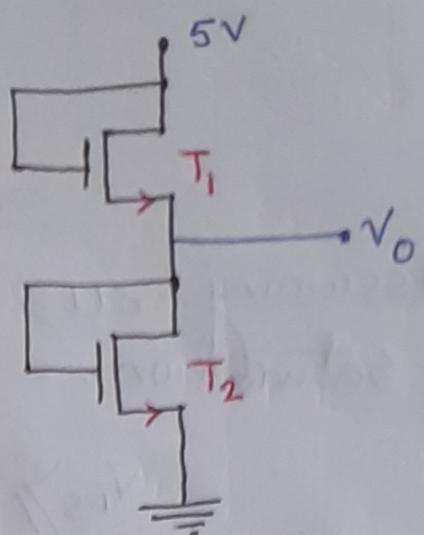
$$\Rightarrow K_1 (V_{gs1} - V_{th})^2 = K_2 (V_{gs2} - V_{th})^2$$

$$\Rightarrow 36 [(5 - V_o) - 1]^2 = 9 [(V_o - 0) - 1]^2$$

$$\Rightarrow 36 (4 - V_o)^2 = 9 (V_o - 1)^2$$

$$\Rightarrow \frac{4 - V_o}{V_o - 1} = \frac{3}{6} = \frac{1}{2}$$

$$\Rightarrow V_o - 1 = 8 - 2V_o ; 3V_o = 9 ; V_o = 3 \text{ volt } (\text{Ans})$$



Q10) For n-channel JFET, $V_p = -5V$; shows transconductance (g_m) = 1 mA/V .
 When $V_{gs} = -3V$; find max transconductance.

\Rightarrow We know that,

$$g_m = g_{m0} \left(1 - \frac{V_{gs}}{V_p}\right)$$

given,

$$g_m = 1 \text{ mA/V}$$

$$\therefore g_{m0} = \frac{g_m}{\left(1 - \frac{V_{gs}}{V_p}\right)} = \frac{1}{1 - \frac{3}{5}} = 2.5 \text{ mA/V}$$

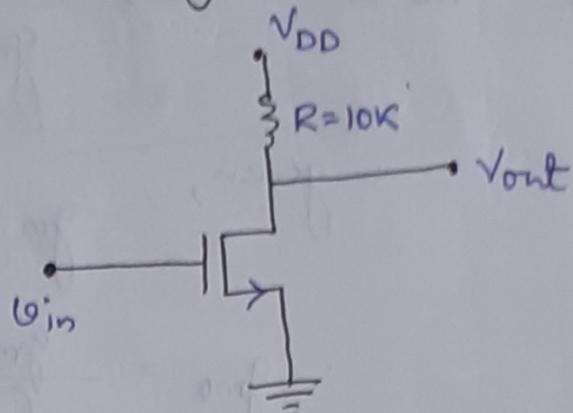
(A_m)

89) Assume $\frac{W}{L} = 2$; $V_{DD} = 2.0$ volt.

$\mu_n C_{ox} = 100 \text{ mA/V}^2$ and $V_{Th} = 0.5$ volt

The transistor M₁ switches from saturation region to linear region, when V_{in} is greater than, →

- (a) 1.5
- (b) 1.6
- (c) 1.7
- (d) 1.8



⇒

for saturation,

$$\begin{aligned} I_D &= \mu_n \cdot C_{ox} \cdot \frac{W}{2L} (V_{gs} - V_{Th})^2 && \left\{ \text{at the edge of Saturation} \right. \\ &= \frac{1}{2} \times 100 \times 10^{-6} \times 2 \times (V_{out})^2 \\ &= 100 \times 10^{-6} \times (V_{out})^2 \end{aligned} \quad \dots \textcircled{i}$$

Now, KVL in outer loop we get, →

$$V_{DD} = I_D \times 10k + V_0 \quad \dots \textcircled{ii}$$

From eqn. (i) and (ii) we get, →

$$2 = 100 \times 10^{-6} \times (V_{out})^2 \times 10 \times 10^3 + V_{out}$$

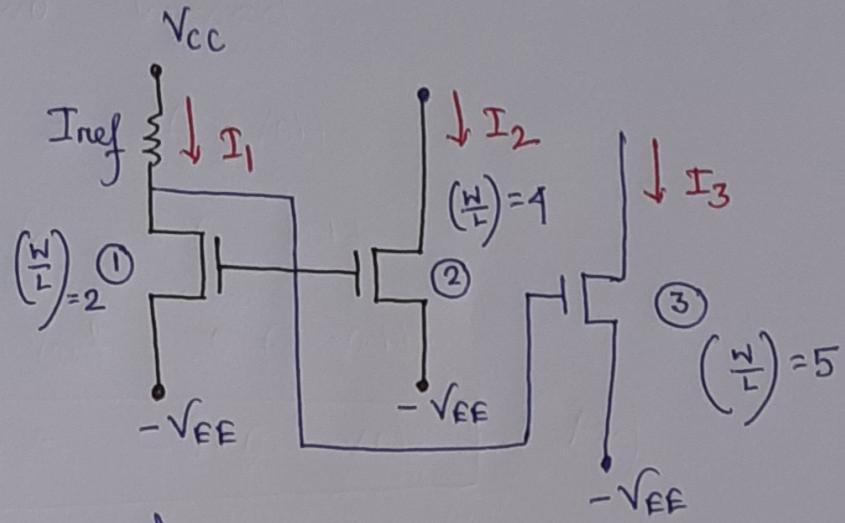
$$\Rightarrow V_{out}^2 + V_{out} - 2 = 0 \quad ; \quad V_{out} = 1 \text{ volt}$$

$$V_{DS} = V_{gs} - V_{Th} \quad ; \quad V_{out} = V_{in} - V_{Th}$$

$$\Rightarrow V_{in} = V_{out} + V_{Th} = 1 + 0.5 = 1.5 \text{ volt (Ans)}$$

Q4) find I_3 .

$$I_{ref} = 10 \text{ mA}$$



\Rightarrow It is clearly seen that, given circuit is a current mirror circuit.

$$I_2 = I_{ref} \frac{\left(\frac{W}{L}\right)_2}{\left(\frac{W}{L}\right)_1}$$

$$I_3 = I_{ref} \frac{\left(\frac{W}{L}\right)_3}{\left(\frac{W}{L}\right)_1} = 10 \text{ mA} \times \frac{5}{2}$$

Q5) find V_{D2} .

$$\left(\frac{W}{L}\right)_1 = 1.5 \left(\frac{W}{L}\right)_2 ; \mu_n C_{ox} = 100 \text{ mA/V}^2$$

$V_f = 1 \text{ V}$ < both Q_1 & Q_2 in saturation>.

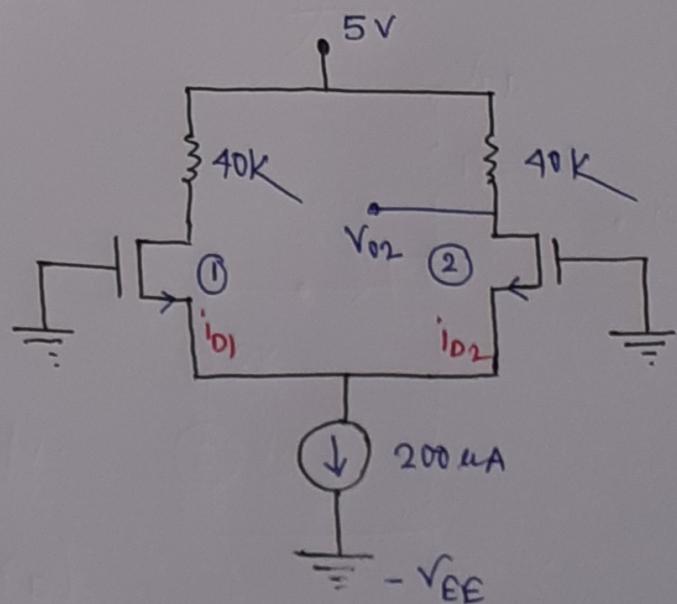
\Rightarrow Here,

$$\frac{i_{D1}}{i_{D2}} = 1.5 \quad \dots \text{(i)}$$

$$i_{D1} + i_{D2} = 200 \mu\text{A} \quad \dots \text{(ii)}$$

$$\therefore i_{D1} = 120 \mu\text{A} ; i_{D2} = 80 \mu\text{A}$$

$$\begin{aligned} \therefore V_{D2} &= 5 - 40 \times 10^3 \times 80 \times 10^{-6} \\ &= 1.8 \text{ volt} \quad (\text{Ans}) \end{aligned}$$



$$82) I_D = 10 \text{ mA}, V_P = -5 \text{ V}, I_{DSS} = 1 \text{ mA}$$

$r_d = 4.7 \text{ k}\Omega$ find voltage gain (A_v)

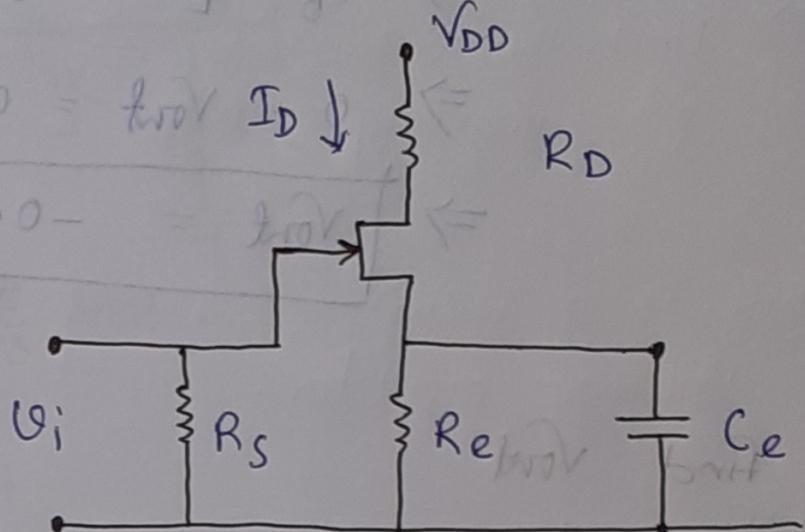
\Rightarrow

$$g_m = \left| \frac{2I_{DSS}}{V_P} \right| \left(1 - \frac{V_{GS}}{V_P} \right)$$

$$= \left| \frac{2I_{DSS}}{V_P} \right| \sqrt{\frac{I_D}{I_{DSS}}}$$

$$= \left| \frac{2 \text{ mA}}{-5} \right| \sqrt{\frac{10}{1}}$$

$$= 1.265 \times 10^{-3} \text{ A/V}$$



$$\text{Now, voltage gain } (A_v) = -g_m r_d = -1.265 \times 10^{-3} \times 4.7$$

$$0 = V_o + 10V \approx -10 \text{ V} (\text{Ans})$$

Q1) Find voltage gain (A_v).

$$\text{Given, } \mu = 50 ; r_d = 10K$$

\Rightarrow We know that,

$$g_m = \frac{\mu}{r_d}$$

$$\Rightarrow g_m = \frac{\mu}{r_d} = \frac{50}{10K} = 5 \text{ mA/V}$$

$$\text{Voltage gain } (A_v) = -g_m (r_d || R_D)$$

$$A_v = -5 \times (10 || 10) = -25 \text{ (Am)}$$

