

* Short channel Devices:-

A MOSFET device is considered to be short when the channel length is the same order of magnitude as the depletion layer width (α_{ad} , α_{ds}) of the source & drain junction.

- i) As the channel length (L) is reduced, it increases both the operation speed and the no of components per chip.

Short channel Effects :-

Short channel effects are attributed to two physical phenomena —

1. The limitation imposed on electron drift characteristics in the channel.
2. The modification of threshold voltage due to the shortening channel length.

In particular five different short-channel effects can be distinguished, —

- i) DIBL & punch through.
- ii) Surface scattering.
- iii) Velocity saturation.
- iv) Impact ionization.
- v) Hot electrons effect.

* Drain Induced Barrier Lowering (DIBL):

- i) It refers to reduction of threshold voltage of the transistor at higher drain voltages.
- In a classical planar FET with long channel, threshold was independent with drain voltage. In short channel devices it is no longer true; As the drain is close enough to the gate, so a high drain voltage can open the bottleneck and turn on the transistor prematurely.
- ii) From 'you' charge sharing model \rightarrow The combined charge in the depletion region of the device and that in the channel of the device is balanced by three electrode charges (Gate, Source & Drain).
As drain voltage is increased, the depletion region of the p-n junction (drain & bulk) increases in size and extended under the gate. As a result, the charge present on the gate retains charge balanced by attracting more carriers into the channel which is the effect equivalent to lowering the threshold voltage of the device.

In effect, the channel becomes more attractive for electrons. In other words, the potential energy barriers for electrons in the channel is lowered — Called Barrier lowering.

iii) Barrier Lowering increases as channel length is reduced (even at zero applied drain bias). At extremely short length, the gate entirely fails to turn the device off.

In practice, DIBL can be calculated as,

$$DIBL = - \frac{V_{Th}^{DD} - V_{Th}^{low}}{V_{DD} - V_D^{low}}$$

Minus sign ensure positive DIBL value.

V_{Th}^{DD} → Threshold voltage measured at high Drain voltage.

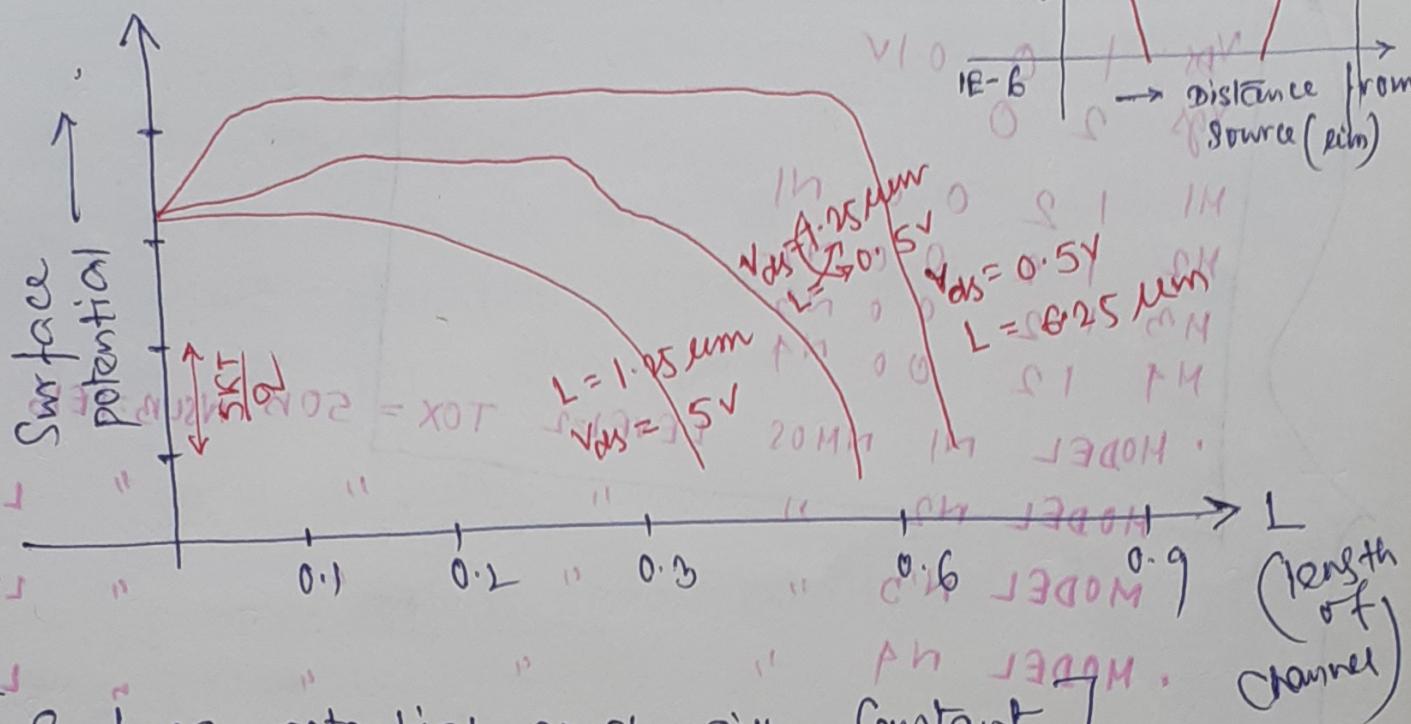
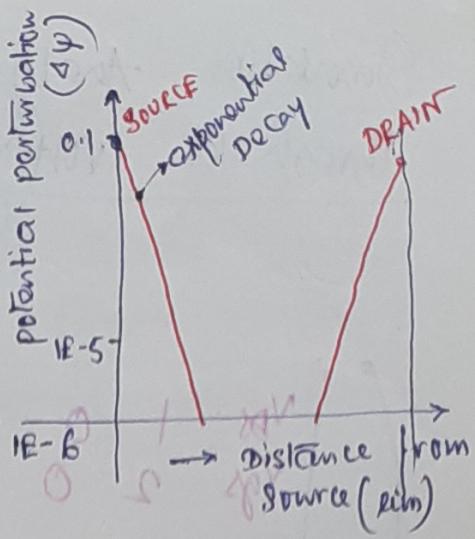
V_{Th}^{low} → Threshold voltage measured at low Drain voltage. (typically 0.05V).

V_{DD} → Supply voltage

V_D^{low} → Low Drain voltage.

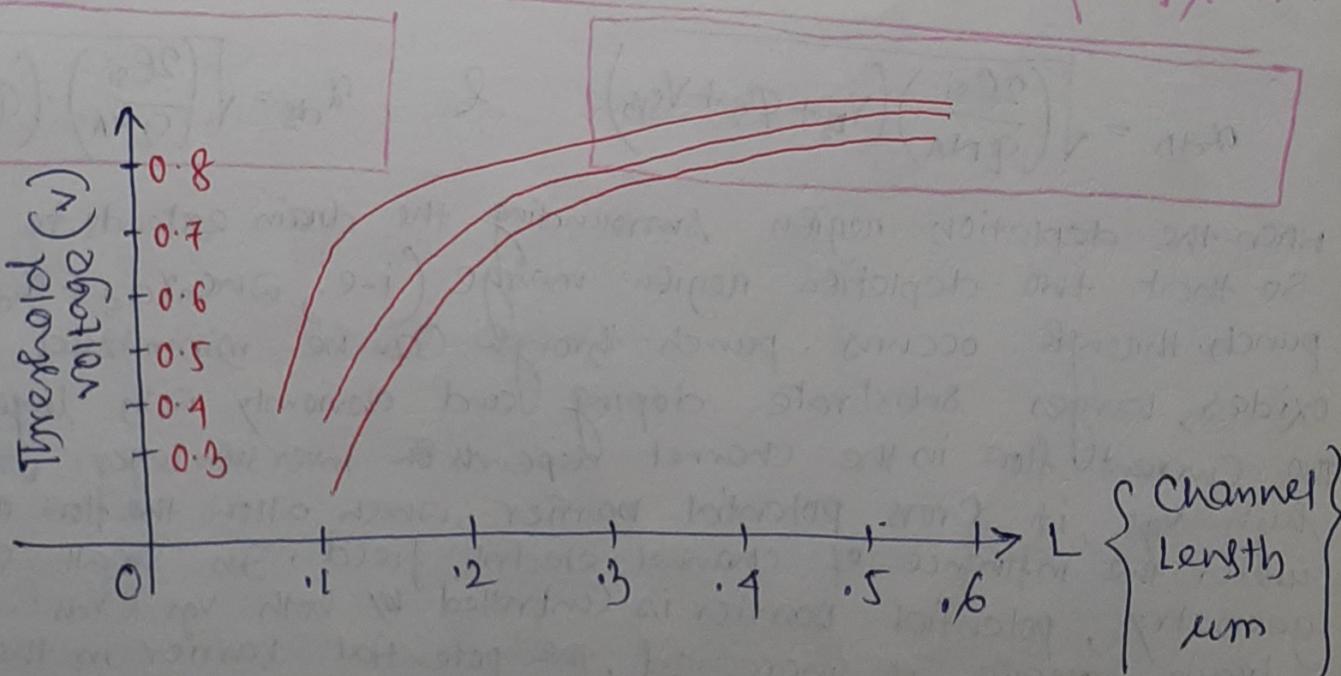
iv) DIBL can reduce the Device operating frequency as well.

$$\frac{\Delta f}{f} = - \frac{2 * DIBL}{V_{DD} - V_{Th}}$$



[Surface potential graph with Constant gate voltages and V_{L0} are varied]

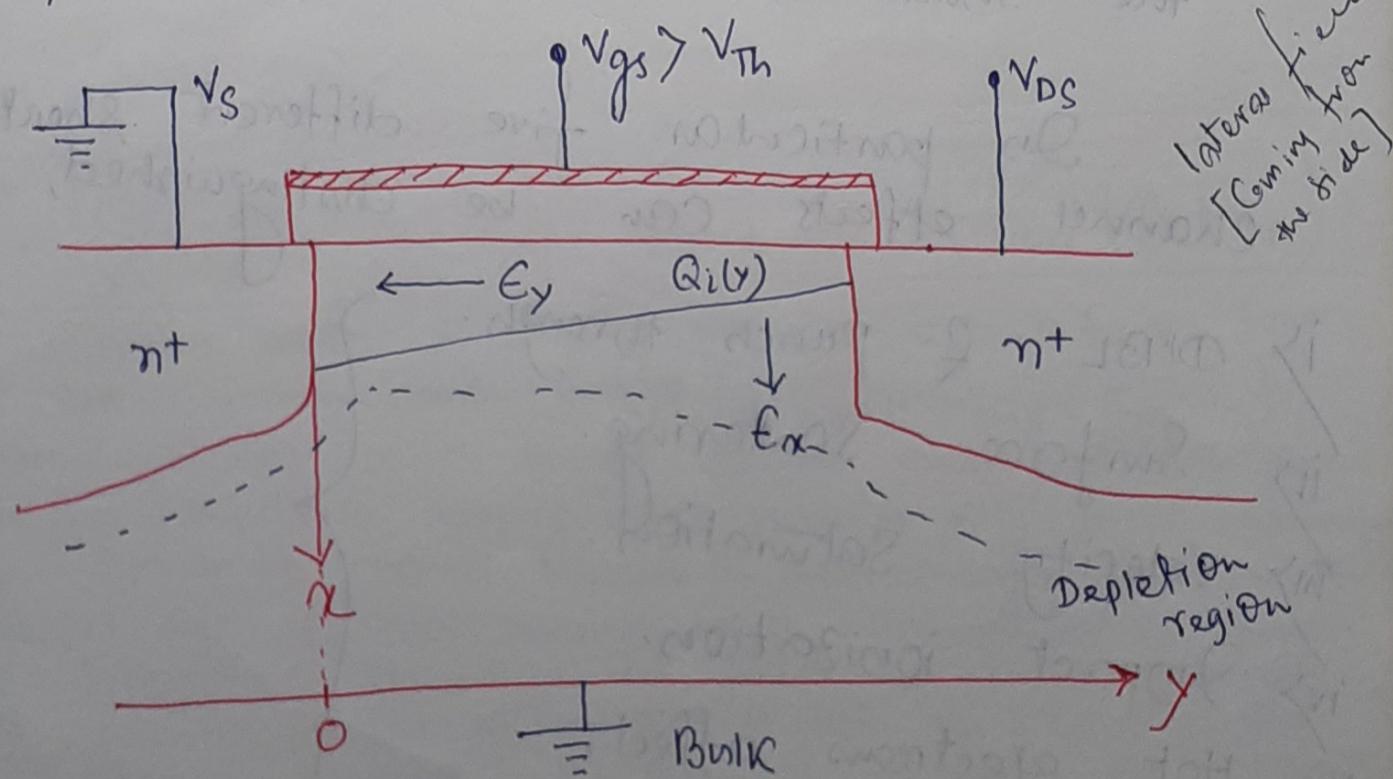
N.B. \Rightarrow The channel current that flows under this condition ($V_{GS} < V_{Th}$) is called sub-threshold current.



* Surface Scattering: As the channel length becomes smaller due to the lateral extension of the depletion layer into the channel region, the longitudinal electric field component (E_y) increases and the surface mobility becomes field dependent.

i) Since the carrier transport phenomena in a MOSFET is confined within the narrow inversion layer and the surface scattering (that is the collision suffered by the electrons that are accelerated towards the interface by E_x) causes reduction of the mobility.

The electrons move with great difficulty parallel to the interface, so that the average surface mobility, even for small values of E_y , is about half as much as that of the bulk mobility.



N.B → In a long channel device, lateral field is negligible over most of the channel & almost all the depletion charge is controlled by the gate field.

In a short channel device, lateral field become appreciable. Lateral field is highest at the source & drain junction, decreasing exponentially toward the middle of the channel.

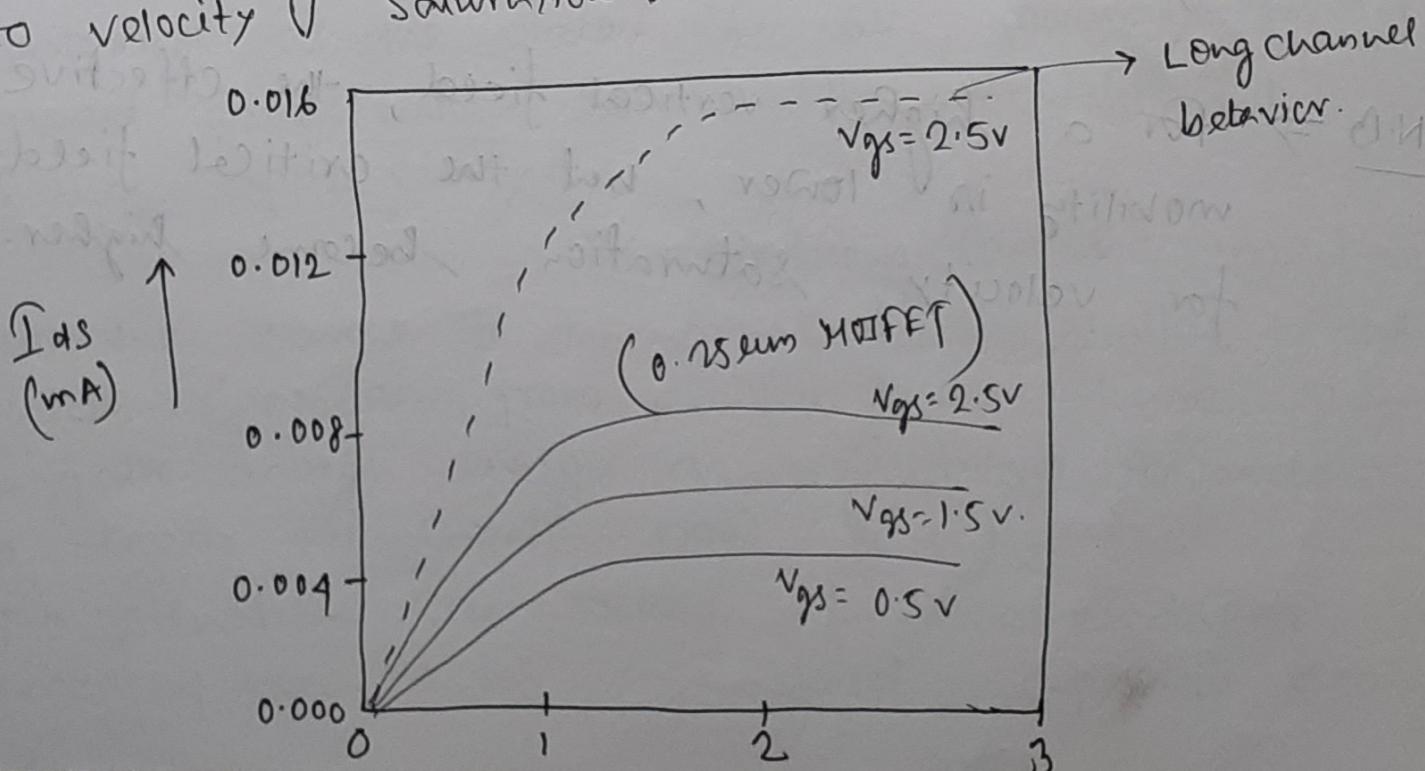
$$\frac{V}{\sqrt{(3/3) + 1}} = 2$$

① Velocity Saturation & High field transport:-

When the drain voltage increases in a long channel MOSFET, the drain current first increases, then become saturated at a voltage equal to

$$V_{dsat} = (V_{gs} - V_t) / m ; \quad m = 1 + \frac{3 \cdot t_{ox}}{W \cdot d_m}$$

In a short channel devices, the saturation of drain current may occurs at a much lower voltage due to velocity saturation.



Due to velocity saturation, the drain current saturates at a drain voltage much lower than $(V_{GS} - V_t)/m$.

Velocity field Relationship \Rightarrow velocity-field

Relationship for electrons & holes takes the empirical forms

$$v = \frac{M_{eff} \cdot \epsilon}{[1 + (\epsilon/\epsilon_c)^n]^{1/n}}$$

Where,

$n=2$, for electrons } 'n' is a measure of
 $n=1$ " holes. } how rapidly the carriers approaches the saturation.

The parameter ϵ_c \rightarrow called critical field.

At low field

$$v = M_{eff} \cdot \epsilon$$

$$\text{As, } \epsilon \rightarrow \infty, v = v_{sat} = M_{eff} \cdot \epsilon_c$$

N.B \Rightarrow for a higher vertical field, the effective mobility is lower, but the critical field for velocity saturation become higher.

* Impact Ionization :-

Another undesirable SCE, specially in NMOS occurs due to the high velocity of electrons in presence of high longitudinal field (E_y) that can generate electron-hole pairs by impact ionization (that is by impacting on Silicon atoms and ionizing them).

It happens as follows:- Normally most of the electrons are attracted by the drain while the holes enter the substrate to form part of the parasitic substrate current.

Moreover, the region between the source and the drain can act the base of an NPN transistor, with the source playing the role of emitter and drain that of the collector.

If the aforementioned holes are collected by the source and the corresponding hole current creates a voltage drop in the substrate material of the order of $1.6V$, normally reverse-biased substrate-source pn junction will conduct appreciably.

Then electrons can be injected from the source to the substrate, similar to the injection of electrons from emitter to the base. They can gain enough energy as they travel towards the drain to create new (e-h) pairs.

The situation can worsen if some electrons generated due to the high field escape the drain

field to travel into the Substrate, therefore affecting other devices on a chip.

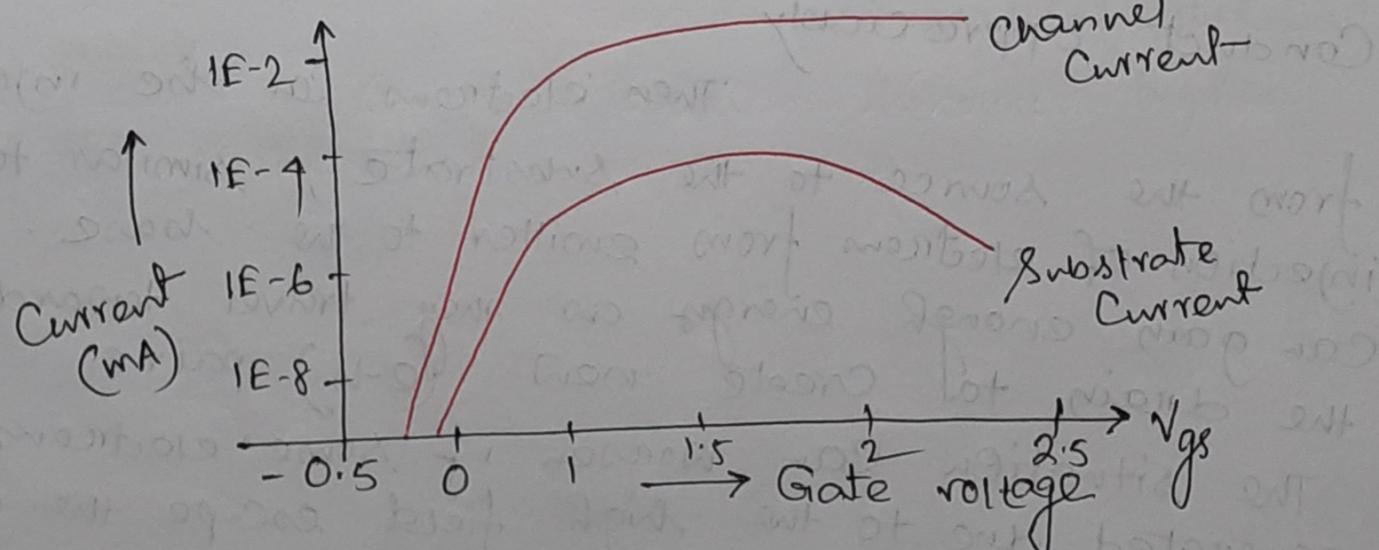
* * Hot Carrier /electrons effects :-

Consider an n-channel MOSFET, with $V_{gs} > V_t$ applied to the gate and V_{ds} applied to the drain. A high field space-charge region is established in the Silicon near the drain.

As the electrons drift towards the drain, they gain energy from the electric field in the space charge region and become hot.

These hot electrons can cause impact ionization near the drain or they can be injected into the gate insulator.

The secondary holes from impact ionization contribute to a substrate current which is less than channel current at same V_{ds} .



When the surface inversion channel is pinch-off

$$\left\{ V_{ds} > V_{dsat} = (V_{gs} - V_t) / m ; m = 1 + \frac{3t_{ox}}{Wd_m} \right\}$$

There is a voltage drop V_{dsat} (drain saturation voltage) along the inversion channel between the source and the pinch-off point and the voltage drop $(V_{ds} - V_{dsat})$ in the space-charge region between the pinch-off point and the drain.

That is the maximum electric field in the Silicon Space charge region is determined by $(V_{ds} - V_{dsat})$.

* for a given V_{ds} , as N_{gs} increases, so does V_{dsat} , which means the voltage drop $(V_{ds} - V_{dsat})$ decreases hence the maximum electric field in the silicon decreases.

The rate of the impact ionization decreases rapidly with decrease in electric field.

The 'hot electrons' injected into the gate insulator near the drain region contribute gate current.

Some of the injected electrons can become trapped in the gate insulator near the drain. These trapped electrons cause the surface potential near the drain to shift.

So, due to the accumulation of hot electrons in the oxide layer (trapped electrons) giving rise to oxide charging with time help to degrade the device performance by increasing V_T .

Thin device degradation is referred as channel hot electrons effect (CHE).

In case of p-channel MOSFET, it is referred as hot hole effect.

N.B \Rightarrow Minority electrons from substrate can gain energy named hot electrons can be injected into the gate insulator, the associated device degradation referred as substrate hot electron effect (SHE).

Since we know that SHE effect increases with temperature.

To reduce/minimize these kind of effects designer often employs lightly doped drain (LDD) design to suppress the same; which introduces additional series resistance and reduces the peak field in a MOSFET.

N.B \Rightarrow If the peak electric field exceed 10^5 V/cm impact ionization takes place at the drain leading abrupt increase of drain current cause Breakdown. (nMOSFET has lower breakdown voltage compared to pMOSFET).