

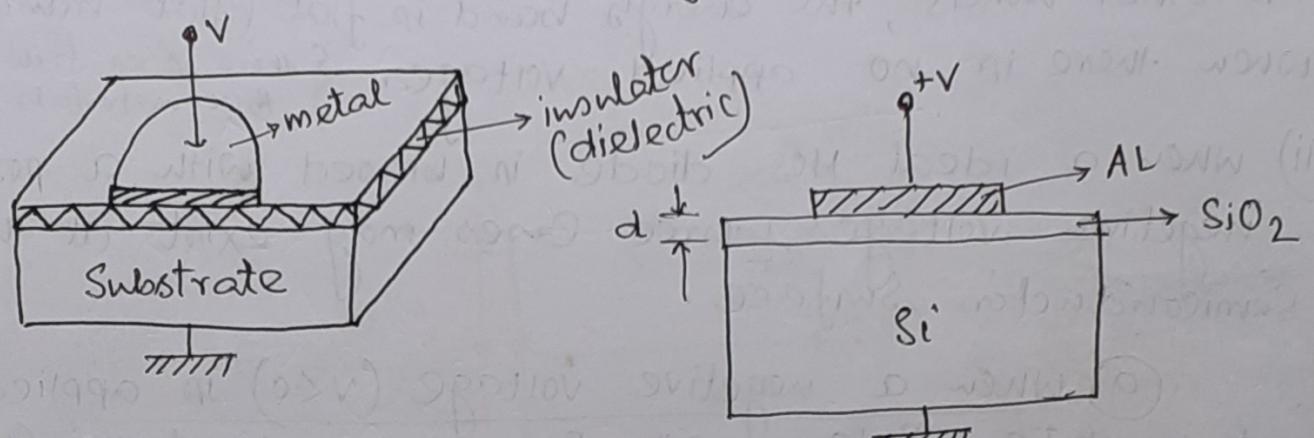
THE MOS DIODE

(5)

(1)

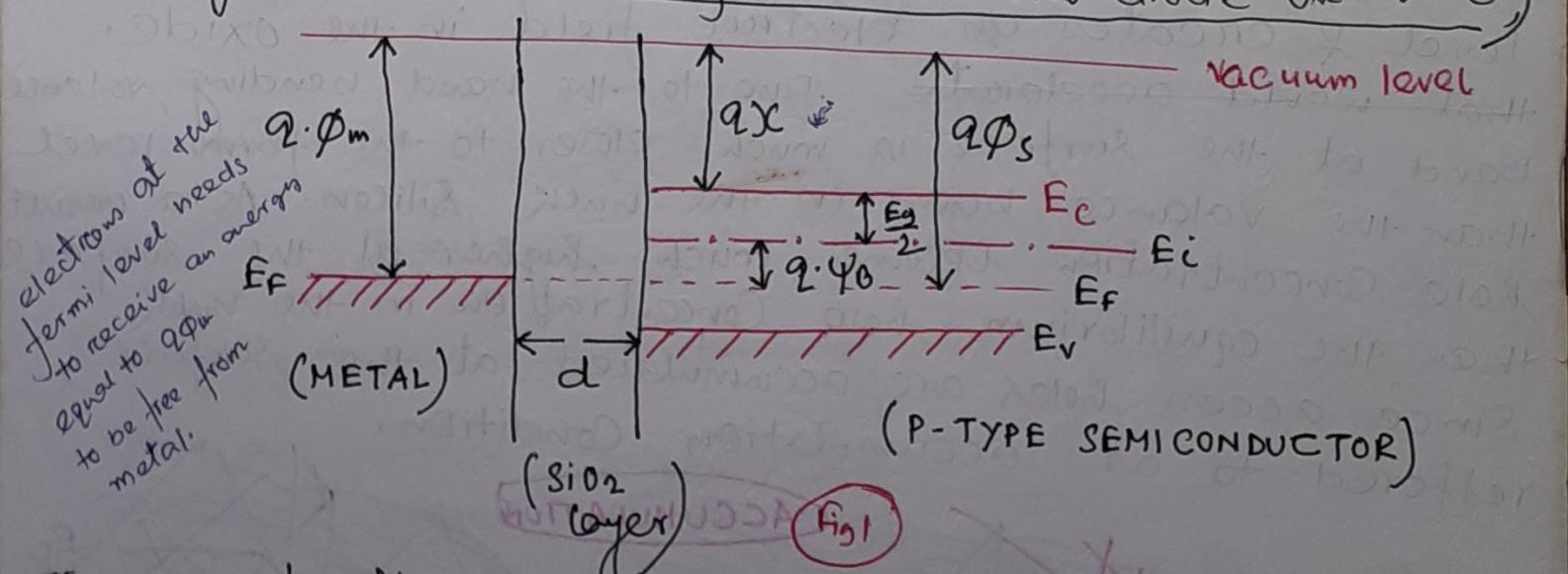
The MOS diode is a very important Semiconductor device, because the device is extremely useful in the study of Semiconductor surfaces.

The MOS diode is the heart of MOSFET & it can be used as a storage capacitor in integrated circuit & it form the building blocks of charge coupled devices (CCD).



Conventionally applied voltage 'V' is positive when the metal plate (polysilicon) is positively biased with respect to ohmic contact.

(The energy band diagram of an ideal MOS diode at V=0)



The work function is the energy difference between the Fermi level and the vacuum level ($q\Phi_m$ for the metal & $q\Phi_s$ for the Semiconductor).

N.B. \Rightarrow when two different materials are brought into contact, the free electron levels in continuous from one material to the next.

Also shown the electron affinity (χ), which is the energy difference between conduction band edge and the vacuum level in the semiconductor. φ_B is the energy difference between fermi level (E_F) & intrinsic fermi level (E_i).

i) when applied bias is zero, $|(\varphi_m - \varphi_s)| = 0$; or the work function difference $\varphi_{ms} = 0$

$$* \text{For this example, the metal work function is less than the silicon work function, the flat-band condition is reached by applying a negative gate voltage.}$$

$$-(\varphi_s - \varphi_m) = \varphi_m; \varphi_{ms} = (\varphi_m - \varphi_s) = \left[\varphi_m - \left(\chi + \frac{E_g}{2} + \varphi_B \right) \right] = 0$$

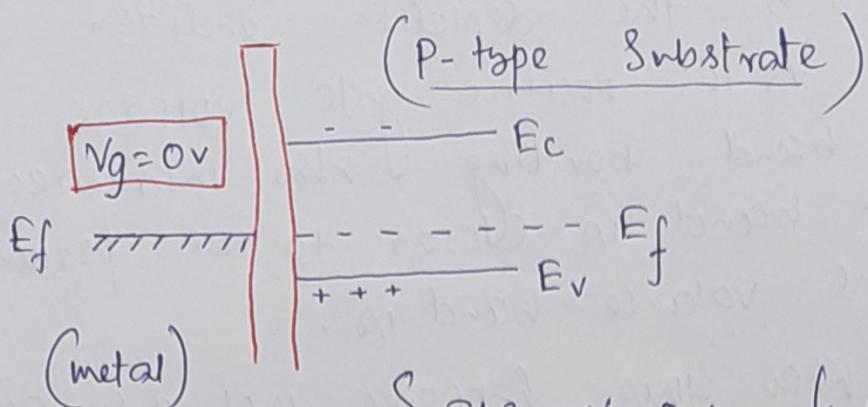
(flat band voltage)

in other words, the energy band is flat (flat-band condition) when there is no applied voltage. {there is no field in all three materials.}

ii) when an ideal MOS diode is biased with a positive or negative voltages, three cases may exist at the semiconductor surface.

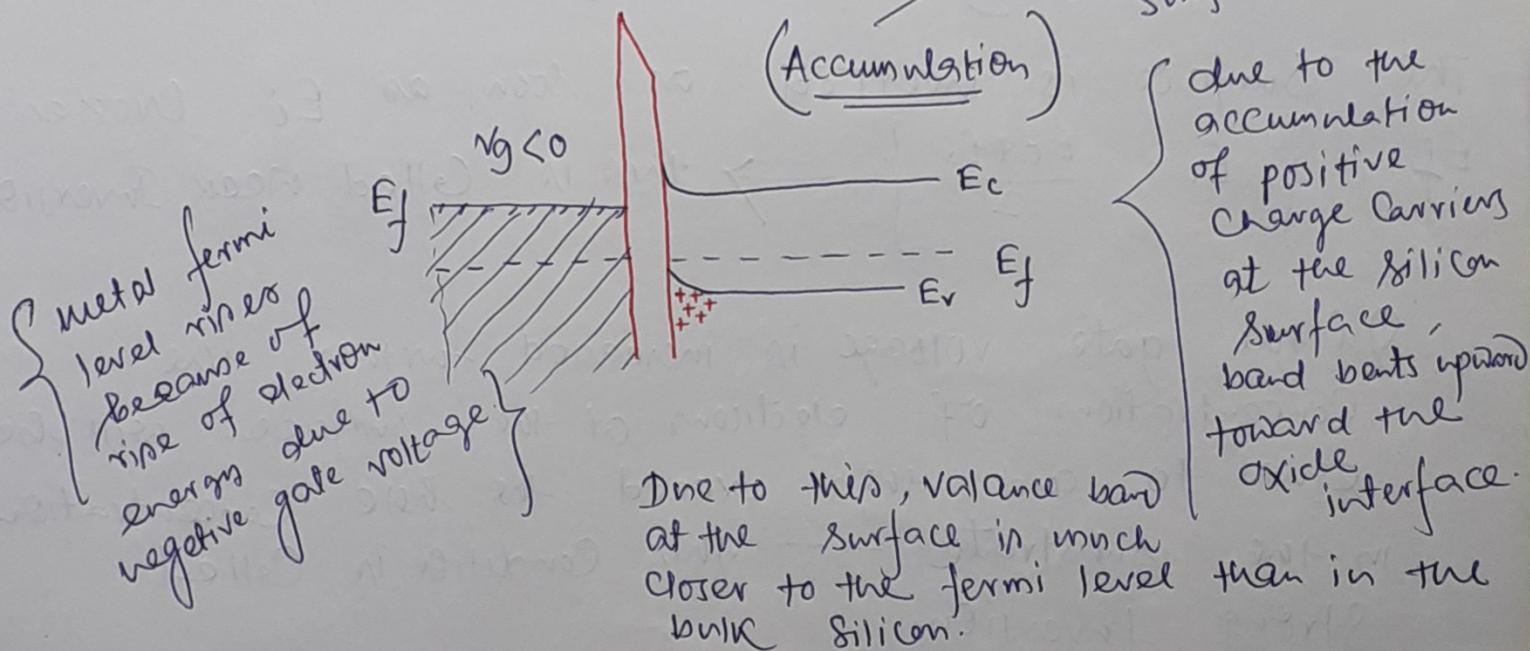
a) When a negative voltage ($V < 0$) is applied to the metal plate, holes will be induced at the $(SiO_2 - Si)$ interface. In this case, bands near the semiconductor surface are bent upward. This raises the metal fermi level (i.e., electron energy) with respect to silicon fermi level & creates an electric field in the oxide.

~~that would accelerate~~ Due to the band bending, valence band at the surface is much closer to the fermi level than the valence band in the bulk silicon. As a result hole concentration becomes much higher at the surface than the equilibrium hole concentration in the bulk. Since excess holes are accumulated at the surface, referred to as accumulation condition.



} when $V_g = 0V$, flat band Condition }

① When $V_g < 0$;

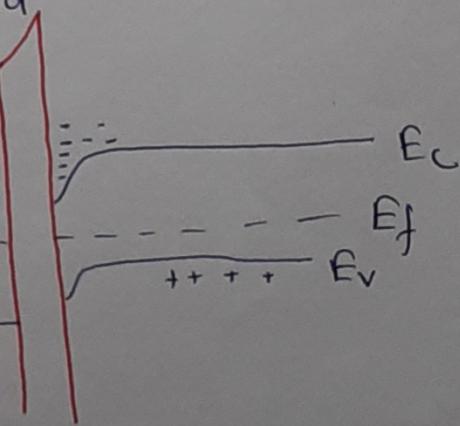


Due to this, valence band at the surface is much closer to the Fermi level than in the bulk silicon.

② When $V_g > 0$;

i) Metal Fermi level moves downward.

ii) Due to positive gate voltage negative charge will be induced at the Si-Substrate Surface; so then holes concentration at the surface become lower than the concentration in the bulk.



this is referred as the depletion Condition.

As the positive gate voltage increases, the band bending also increases. The conduction band is closer to the fermi level than the valance band is.

When this happens not only are the holes depleted from the surface, but the surface potential is such that helps electrons to populate the conduction band. { Surface behaves like n-type material } — this condition is called Inversion.

The surface is inverted as soon as E_i crosses E_f . { $E_i = \frac{E_c + E_v}{2}$ } → this is called weak inversion.

If the gate voltage is increased further, the concentrations of electrons at the surface will be equal to and then exceed the hole concentration in the substrate — this condition is called strong inversion.



The upward bending of the energy band at the Semiconductor Surface causes an increase in the energy ($E_C - E_F$) there, which gives to rise to an enhancement concentration, an accumulation of holes near the oxide Semiconductor Surface. (2)

(b) If a positive voltage applied to the gate of a p-type MOS, the metal fermi level moves downward, which creates an oxide field in the direction of accelerating negative charge towards the metal electrode. A similar field is induced in the silicon which cause the band to bend downward toward the surface. Since the valence band at the surface is now further away from the fermi level (than in the) valence band in the bulk, so, hole concentration at the surface is lower than the concentration in the bulk. This is referred to as depletion condition.

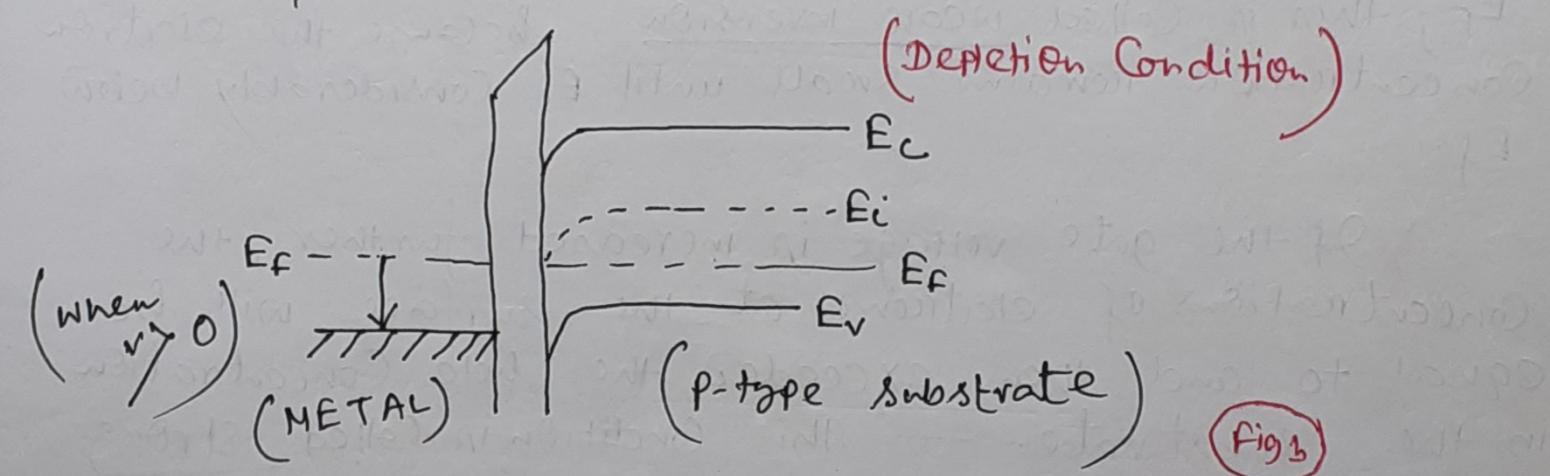


Fig 3

[N.B. → One can think the holes as being repelled away from the surface by the positive gate voltage.]

As the positive gate voltage increases, the band bending also increases. It goes on until the band bent downwards & the conduction band is closer to the fermi level than the valence band.

When this happens, not only the holes

depleted from the surface, but the surface potential is much that energetically favors the electrons to populate the conduction band. In other words, the surface behave like n-type material. This condition is called INVERSION.

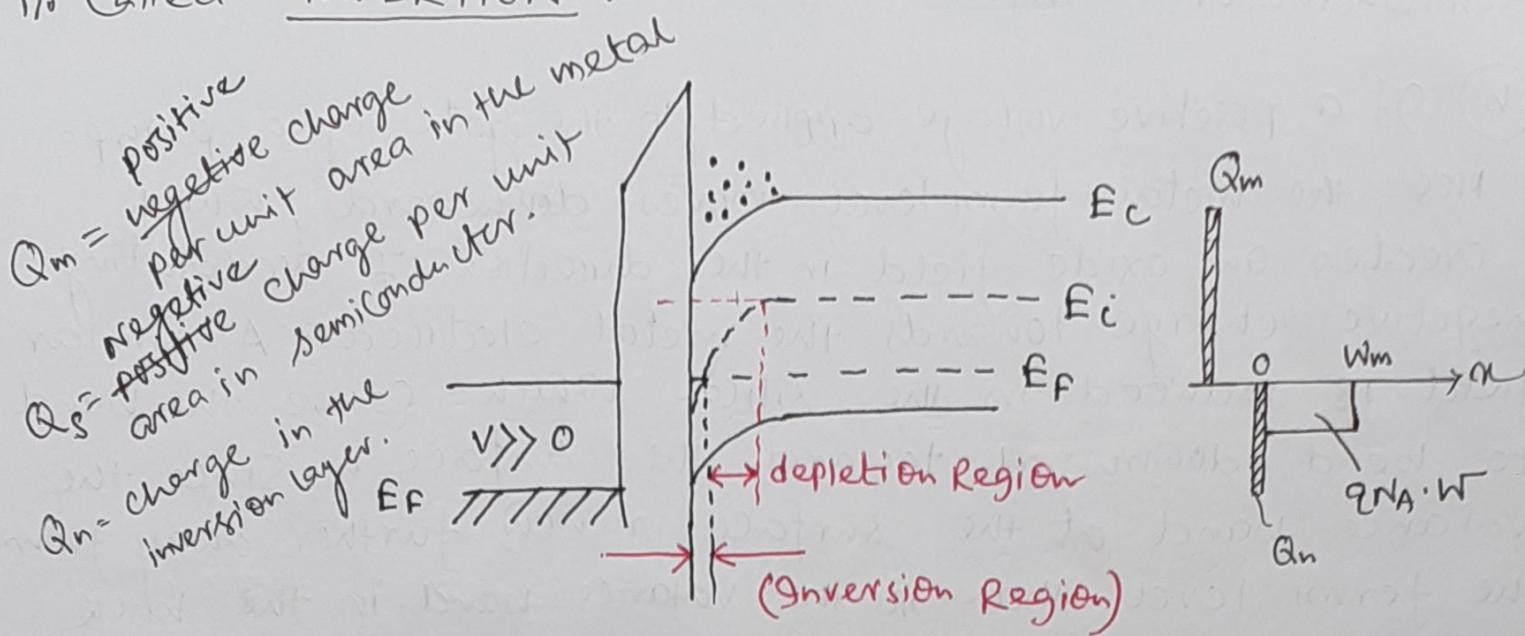


Fig 1
The surface is inverted as soon as $E_i = \frac{(E_C + E_V)}{2}$ crosses E_F ; this is called weak inversion, because the electron concentration remains small until E_i considerably below E_F .

If the gate voltage is increased further, the concentrations of electrons at the surface will be equal to and then exceed the hole concentration in the substrate. — This condition is called strong inversion.

