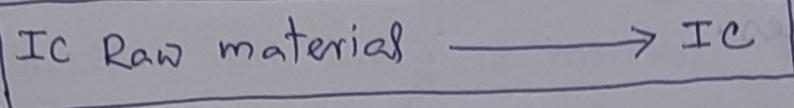


* Introduction to IC Technology →

It's practical topic → On theoretical basis →

Inside IC → CMOS Building blocks → { we can easily fabricate }

any circ. Component using CMOS technology }

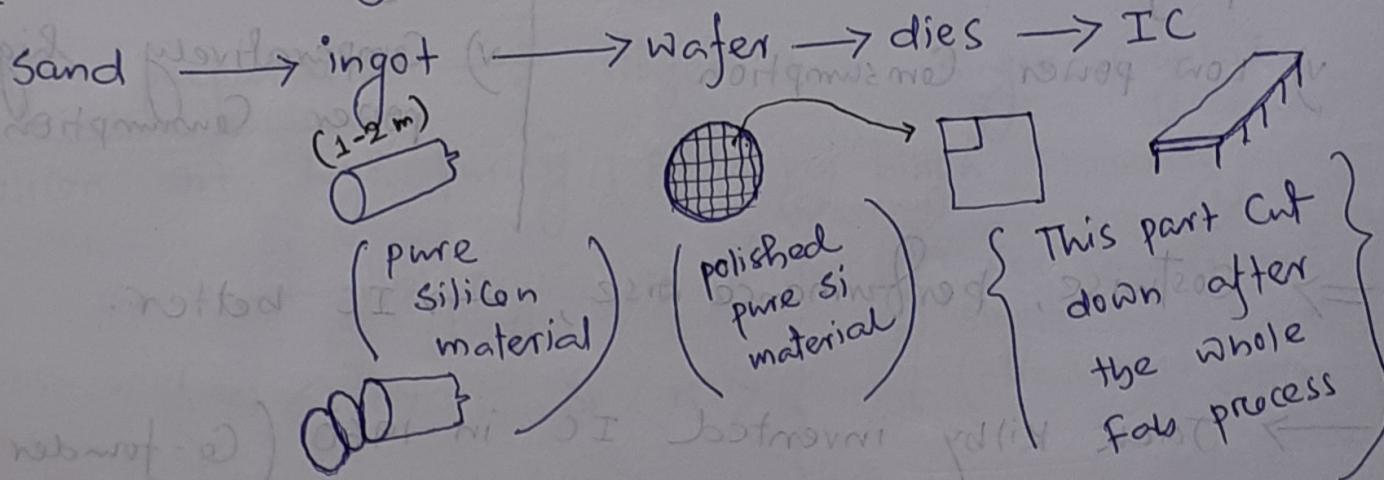


IC fabrication Lab → ISRO, DRDO, BARC, Taiwan Semiconductor Company (Biggest)

→ IIT Mumbai & IISc Bangalore.

→ Fabrication process is very expensive.

∅ principal material of Silicon → SiO_2 (sand).
} which is easily abundant in earth crust } → low cost.



Comparison between IC and Discrete Circuit :-

Integrated circuit is nothing but a single electronic device in which many circuit components are integrated on single crystal wafer →

Called monolithic IC.

→ Here Connection between Components, through layers not wires.

Integrated Circuit	Discrete Circuits
i) It works at low voltage.	i) It's require comparatively high voltage.
ii) very small in size.	ii) It need large space.
iii) It is cheap / low cost.	iii) Costlier than IC.
iv) Complex circuit on chip used to obtain improved performance.	iv) performance is not so good.
v) Low power Consumption.	v) comparatively high power Consumption.

⇒ Costwise, performance wise, → IC better.

→ Jack Kilby invented IC in 1960 (Co-founder of INTEL) but it was Ge based.

→ Robert Noyce (working with Fairchild Corporation) invented IC, which was silicon based.

→ In the evaluation process of IC → related to to how many transistors can easily be fabricated in a particular area of silicon wafer.
~~~~~  
( $\sim 300$  mm diameter of wafer)

→ To increase integration density → size of components need to reduce (Called scaling process).

{ Moors Law → In every 18 months, no of transistors in an IC will be doubled.

First era SSI  $\rightarrow 2-150$  (Components)

↓ Evolution process  
VLSI  $\rightarrow 10^5$  to  $10^6$  (Components)

U L S I  $\rightarrow >10^6$  (Components)

In IC

Feature size decreases.

Nowadays  $\rightarrow$  CMOS technology ( $\sim 10$  nm tech).

### Wafer preparation  $\rightarrow$  Wafer is a single crystal

Silicon with high purity (parts per billion, Impurity),  
(Required)

Sand  $\rightarrow$  polycrystalline silicon. { mixer of different single crystalline (orientation) silicon}

{ Si  $\langle 100 \rangle$ , Si  $\langle 111 \rangle$  }

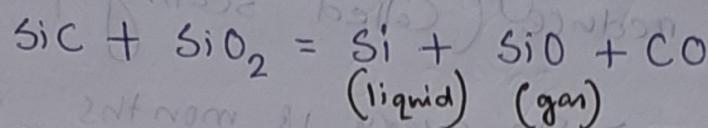
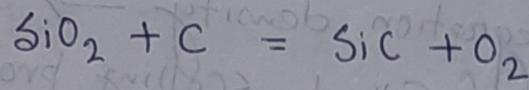
Si  $\langle 110 \rangle$

ii) Metallurgical grade silicon

(parts per million, Al & Fe impurity)

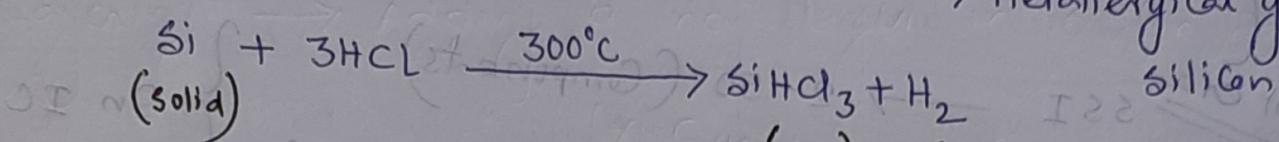
### iii) Electronic Grade Silicon (EGSi)

(parts per billion)  $\rightarrow$  which is required.  
 (Can used as wafer).

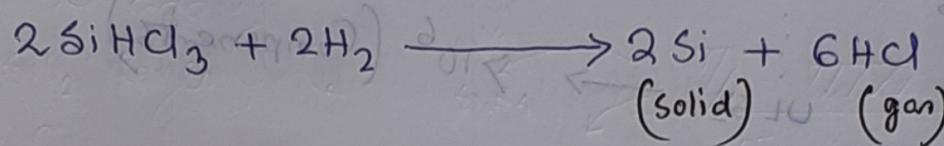


$\text{SiC}$  = Silicon Carbide

(\*) purification of silicon  $\rightarrow$  Metallurgical grade silicon.



fraction distillation,



Electronic grade silicon.

(Can used as wafer formation.)

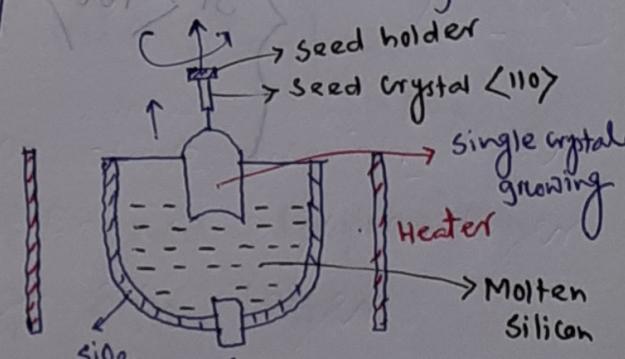
⊕ In case of Electronic Grade silicon (EGSi)  $\rightarrow$  Can change its resistivity ( $\delta$ ), using doping process.

$\rightarrow$  Now, wafer become polycrystalline silicon wafer.

{ need to use 'Czochralski' crystal growth technique }

$\downarrow$   
need to use  
Burnace  
also.

Single Crystalline Silicon wafer { eg.  $\text{Si} <110>$  }



→ After this process, we got 'ingot' of single crystalline silicon.



INGOT (Single crystal) → Cut for wafer disc formation

→ need to use diamond cutter to slice it down.

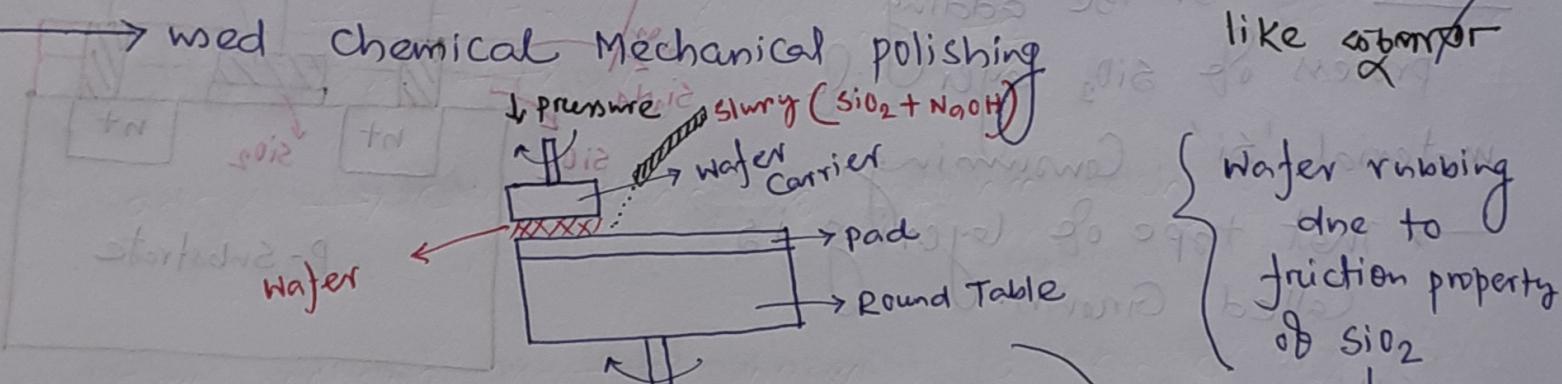


(WAFER)

→ Surface of wafer should be very smooth

→ Wafer surface should be free from any kind of impurity.

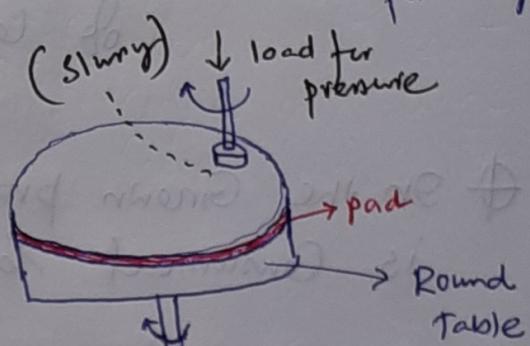
*(Hydrophobic in nature)*



& NaOH used for chemical polishing for smooth surface of wafer.

*(Mirror finished surface)*

for mechanical polishing



GATE Questions → based on process rather than chemical reaction.

## CMOS fabrication :-

- i) Wafer preparation
- ii) Wafer fabrication.

9) Layering

b) Lithography

c) Doping

d) Heat treatment

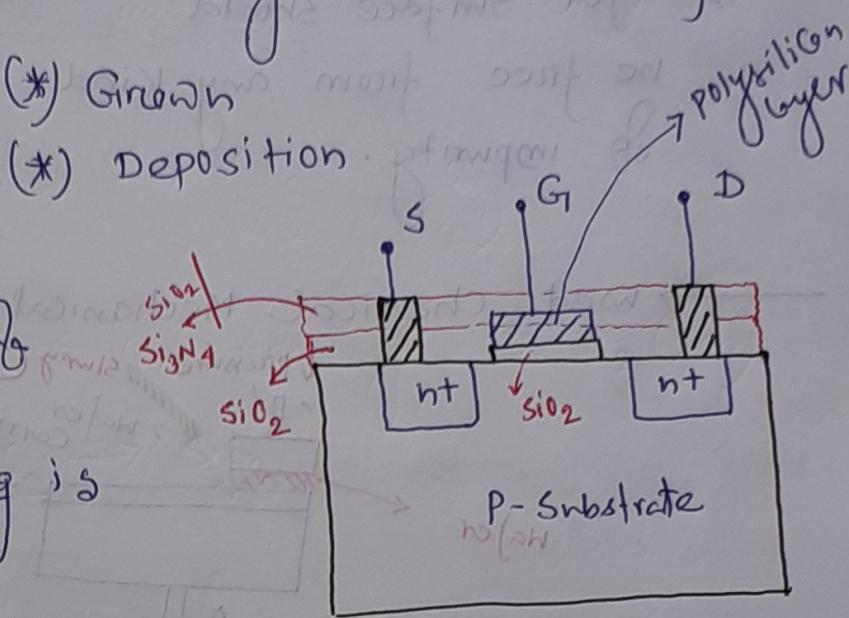
(a) Layering → Adding a new layer in silicon wafer.

(\* ) Growth

(\* ) Deposition

Growth → In the adding process of  $\text{SiO}_2$  layer, material 'Si' Consuming

→ That type of layering is called Growth.



Deposition → When we add a new layer, but it does not Consumed Si-Wafer → That type of layering is known as deposition. (underlying layer does not Consumed).

∅ In the Growth process of  $\text{SiO}_2$  layer, almost 44% [tox] is Consumed by the Si.

∅ formation of polysilicon layer, just above the  $\text{SiO}_2$  layer in the gate region. NO portion of polysilicon layer is Consumed by underlying  $\text{SiO}_2$  layer

→ So, here polysilicon layer formation due to the deposition process.

Grown → a) Oxidation ( $\text{SiO}_2$ ) }  
                                    b) Nitridation ( $\text{Si}_3\text{N}_4$ ) }

Deposition →  
a) Chemical Vapor Deposition } polysilicon  
b) Physical Vapor Deposition } layer  
                                                 → \*) Sputtering  
                                                      \*) Electroplating  
                                                      \*) Thermal evaporation.

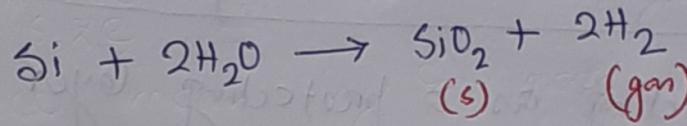
- ⊕ Use of oxidation in IC fabrication:-
- i) It is acting as a protecting layer / mask against diffusion or Ion implantation.
  - ii) Good protective layer against active circuits or it is also act as isolator against active cut.
  - iii) protect against physical / mechanical / chemical protection to the device itself. (External shock)
  - iv)  $\text{SiO}_2$  acting as a good dielectric of Capacitor which is desired for CMOS operation.

Oxidation → It is executed at very high temperature ( $\sim 900^\circ\text{C}$ ), that's why it is also called thermal oxidation.  
to  $1200^\circ\text{C}$   
at furnace (blast furnace)

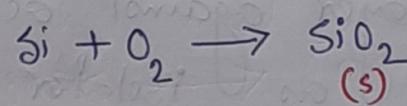
Types :- i) Wet oxidation ii) Dry oxidation.

→ It is used in different position of the IC fabrication.

⊕ On wet oxidation, silicon reacted with water vapour at high temperature.



⊕ On dry oxidation process, silicon reacting with  $\text{O}_2$  (gas).



Used area

- $\text{SiO}_2$  layer formed in the gate region (just below the polysilicon layer) → Dry oxidation. (Capacitor formation)
- $\text{SiO}_2$  layer formed for masking and isolation → Result of wet oxidation.

\* Dry oxidation process is used to form → Thin oxide layer.  
\* Wet " " " " → Thick "

$B_{\text{ox}}$  → Growth rate of wet oxidation is very high.  
" Dry " very poor  $(\mu\text{m})/\text{hr}$   
 $(\text{nm})/\text{hr}$

\*> from dry oxidation process  $\rightarrow$  produce high dielectric constant ( $\epsilon$ ).

\*> In wet oxidation  $\rightarrow$  not good dielectric  $\rightarrow$  leakage current is high  $\rightarrow$  mainly used for mechanical support / isolation process.

# Si<sub>3</sub>N<sub>4</sub>: -

⊕ In the outermost layer of MOS  $\rightarrow$  we Si<sub>3</sub>N<sub>4</sub> layer for isolation Compare to SiO<sub>2</sub>  $\rightarrow$  bcz it provide better isolation.

Melting point of Si<sub>3</sub>N<sub>4</sub> > Melting point of SiO<sub>2</sub>

Bcz  $\rightarrow$  In the heat treatment process need to provide,  $\rightarrow$  for proper annealing process (proper connection), to reduce surface defects (in ion implementation process, spow may occur in the surface, not smooth surface)  $\rightarrow$  very high temperature ( $\sim 8000^\circ\text{C}$ )  $\rightarrow$  so outermost surface of MOS need to have very high melting point material.

$\rightarrow$  Technically Called Passivation (outermost layer of IC) act as glam Covering..

$\rightarrow$  protect from Sodium and Moisture. (protect the device)

↓

## Deposition Layering

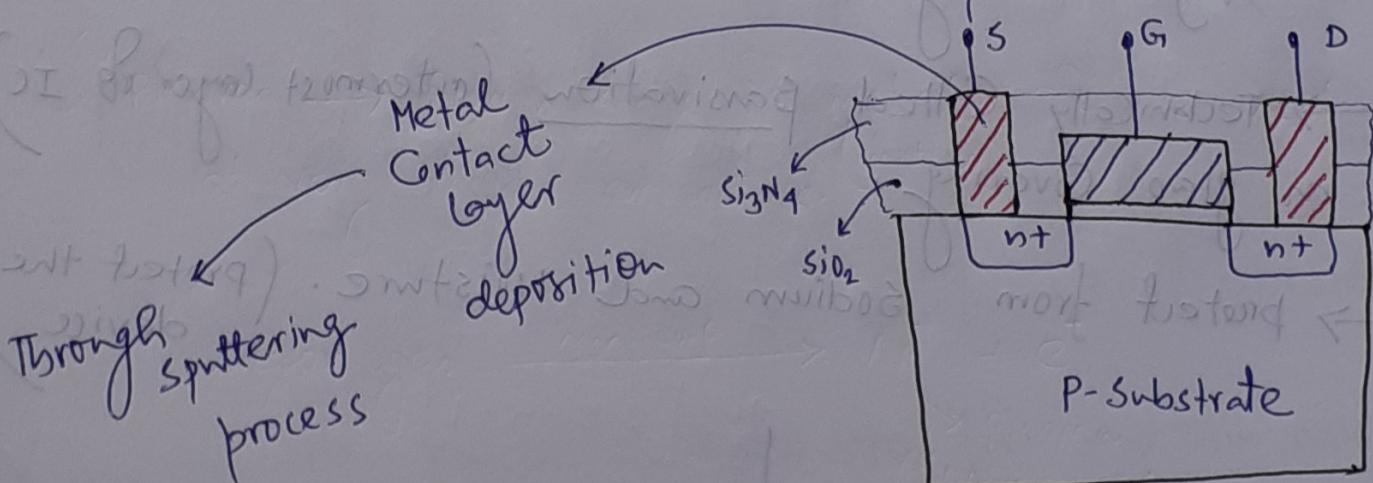
- i). CVD
  - ii) Sputtering { under, physical vapour }
- Deposition technique

CVD → By using chemical process, by which getting vapour → going to deposited on the surface of the wafer.

\* In physical vapour deposition technique → need to apply <sup>physical</sup> force to deposite ion's on the surface of the wafer.

→ physical force, mean by applying voltage (Electrical process).

\* Sputtering process → mainly used for the deposition of Metal (Al) { used for inter- } Connects.



→ So, Metallization, is basically Completed through sputtering process → Which is basically a deposition technique.

→ Chemical Vapour Deposition (CVD) technique

- is used to form 'polysilicon' layer;
- formation of  $\text{Si}_3\text{N}_4$  layer through CVD.

for 'Polysilicon' layer formation  $\Rightarrow$  prA

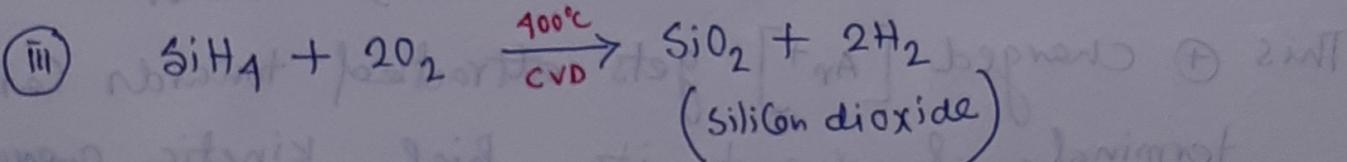
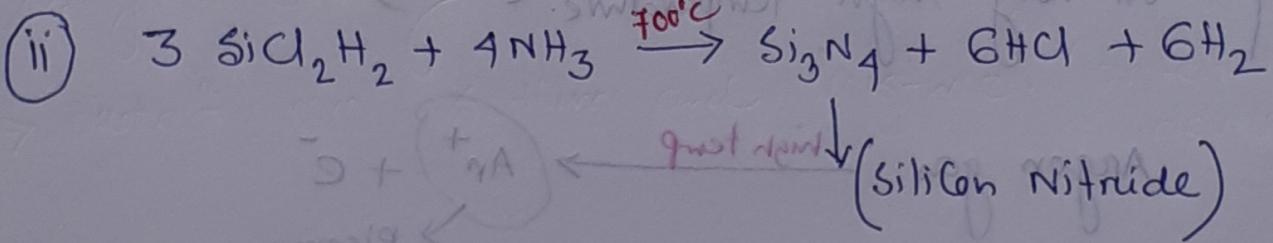
- $\text{SiH}_4$  (Silicon Compound)  $\xrightarrow[1000^\circ\text{C}]{}$  Si +  $2\text{H}_2 \uparrow$  (polysilicon)

⊕ previously Gate material was made of metal (A)  
 → That's why it is called 'Metal oxide Semiconductor FET'  
 → Now a days it is replaced by polysilicon.

↓ Advantages

i)  $V_{th}$  less (power consumption less.)

ii) Melting point high (bcz, heat treatment can be easily done.)



## \* Metallization through sputtering:

Here, plasma of the inert gas (Argon gas) is used

to dislodge the material from

the metal surface

→ which is deposited on the surface of wafer.

(A) Iation of atom

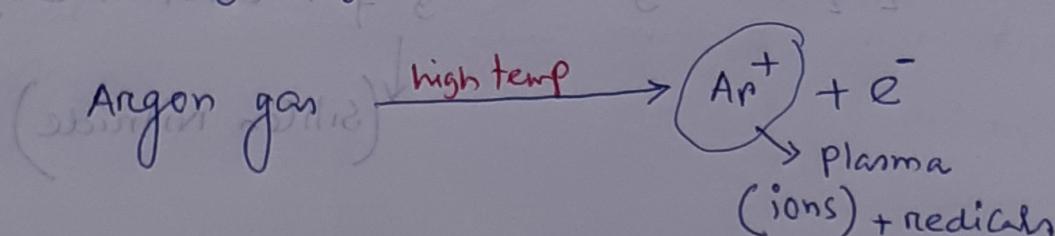
So, Argon atoms will be ionized by the electric field.

Metallization → layering the surface of the wafer.

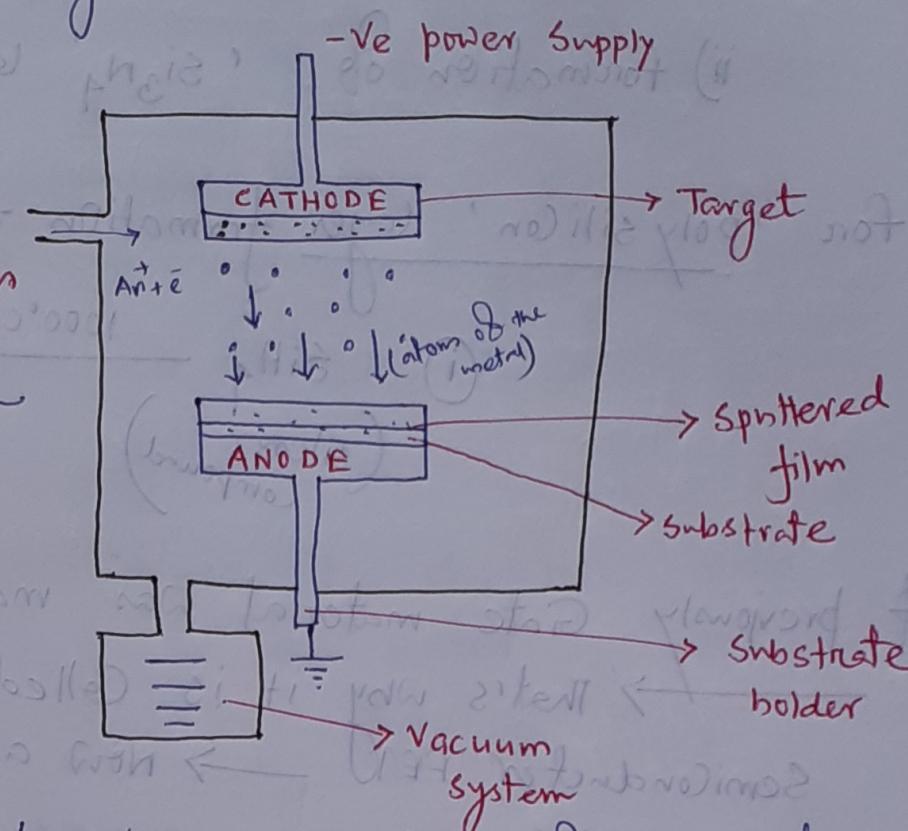
Generally used for 'Electrical metal Contact'.

→ The Kinetic energy of Plasma (ions) is used to remove metal atoms from the metal surface and it is deposited on the surface of the wafer.

{'plasma' → fourth stage of metal. If we heat gas at very high temperature. (matter)}



This  $\oplus$  charged  $[\text{Ar}^+]$  gets attracted towards Cathode terminal & due to its high kinetic energy it will remove atoms from metal surface (process is sputtering)



Here, metallization done → all the top side of  
the substrate → After using etching process,  
Can etched out surface, where metallization not  
required. { Only required in source, gate and }  
drain region.