

VLSI (Numericals)

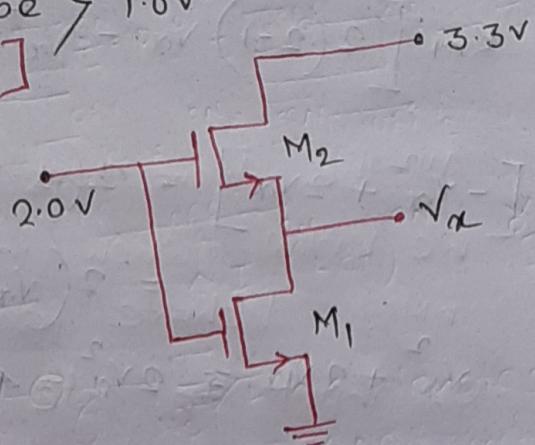
Q1.) On the CKT given below, $\left(\frac{W}{L}\right)_{M_2} = 2 \left(\frac{W}{L}\right)_{M_1}$
 $V_T = 1.0\text{ V}$ for both the transistors. find V_x .

Note that, V_{GS} for M_2 must be $> 1.0\text{ V}$.

[Gate 2018]

\Rightarrow for M_1 ,

$$V_{GS1} - V_T = 2 - 1 \\ = 1 \text{ volt}$$



Now, for M_2 ,

$$V_{GS2} = V_T \\ = [(2 - V_x) - 1] = (1 - V_x) < 1 \text{ volt}$$

and, $V_{DS2} = (3.3 - V_x) > (V_{GS2} - V_T)$... i

So, here clearly M_2 will be in saturation.

As, V_{GS} of $M_2 > 1.0\text{ V}$

$$\Rightarrow 2 - V_x > 1 ; 1 > V_x \quad \text{ii}$$

Now, $V_{DS_{M_1}} = V_x$; we also know that, $[V_{GS} - V_T = 1\text{ V}]$

$$\text{so, for } M_1 \rightarrow [V_{DS}]_{M_1} < [V_{GS} - V_T]_{M_1}$$

→ Clearly operating in linear region.

But, Current across them should be same.

$$I_{D1} = I_{D2}$$

$$\Rightarrow K_{n1} \left[(V_{GS1} - V_T) V_{DS1} - \frac{V_{DS1}^2}{2} \right] = \frac{K_{n2}}{2} (V_{GS2} - V_T)^2$$

$$\Rightarrow K_{n1} \left[2(2-1)V_x - V_x^2 \right] = 2K_{n1} (2-V_x-1)^2 \quad \left. \begin{array}{l} A_3, \\ K_{n2} = 2K_{n1} \end{array} \right\}$$

$$\Rightarrow [-V_x^2 + 2V_x] = 2(1-V_x)^2$$

$$= 2(V_x^2 - 2V_x + 1)$$

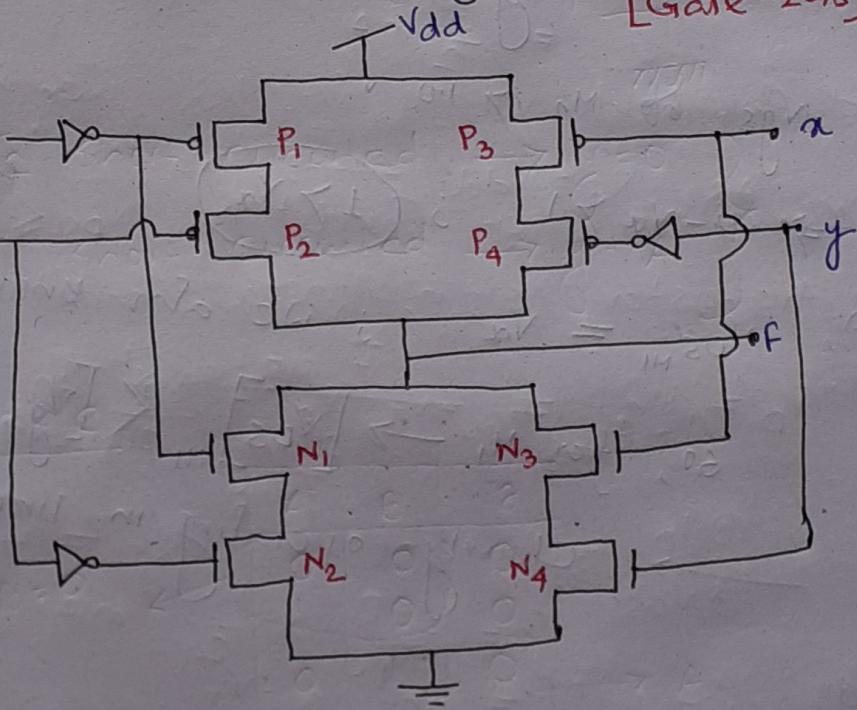
$$\Rightarrow -V_x^2 + 2V_x = 2V_x^2 - 4V_x + 2$$

$$\Rightarrow 3V_x^2 - 6V_x + 2 = 0 \quad ; \quad V_x = 1 \pm \sqrt{\frac{1}{3}} \text{ volt}$$

As, $1 > V_x$ → from Condition no (ii)

$$V_x = \left(1 - \sqrt{\frac{1}{3}}\right) = 0.4226 \text{ volt} \quad (\text{Ans})$$

Q2. The logic function realized by the ckt, is → [Gate 2018]



Now, the truth table of the logic CKT,

x	y	P ₁	P ₂	P ₃	P ₄	N ₁	N ₂	N ₃	N ₄	F
0	0	off	on	on	off	on	on	off	off	0
0	1	off	off	on	on	on	off	off	on	1
1	0	on	on	off	off	off	on	on	off	1
1	1	on	off	off	on	off	off	on	on	0

Here, $f = \bar{x}y + xy = x \oplus y \Rightarrow$ This denotes X-OR function.

Q3) for a long channel nMOSFET,

$$g_m = 0.5 \mu A/V \text{ for } V_{DS} = 50 mV \text{ & } V_{GS} = 2V$$

$$g_d = 8 \mu A/V \text{ for } V_{DS} = 0V \text{ & } V_{GS} = 2V$$

$$\left\{ \text{where, } g_m = \frac{\partial I_D}{\partial V_{GS}} \text{ and } g_d = \frac{\partial I_D}{\partial V_{DS}} \right\} \quad \begin{matrix} \text{[Gate 2016]} \\ \text{Set 2} \end{matrix}$$

find threshold voltage of the given nMOSFET.

\Rightarrow from the given Condition, $V_{DS} \leq V_{GS} - V_T$, so transistor is in linear Condition.

$$I_D = K_n \left[(V_{GS} - V_T) V_{DS} - \frac{V_{DS}^2}{2} \right]$$

$$\therefore \frac{\partial I_D}{\partial V_{GS}} = K_n V_{DS} \quad K_n = \frac{0.5 \times 10^{-6}}{50 \times 10^{-3}} = 10^{-5} A/V^2$$

$$\text{and, } g_d = \frac{\partial I_D}{\partial V_{DS}} = K_n (V_{GS} - V_T)$$

$\xrightarrow{\text{during partial differentiation higher order of } V_{DS} \text{ eliminated}}$

$$\Rightarrow 8 \times 10^{-6} = 10^{-5} (2 - V_T)$$

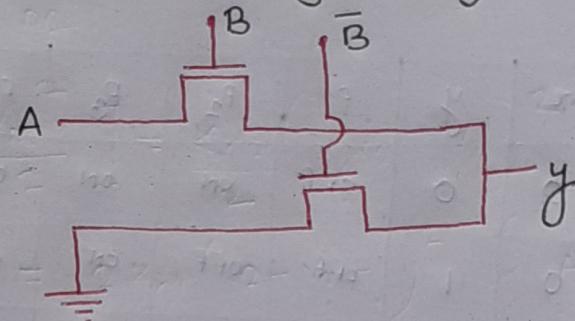
$$\Rightarrow V_T = 1.2 \text{ volt} \quad (\text{Ans})$$

$\xrightarrow{\text{as, } V_{DS} \leq V_{GS} - V_T}$

Q4.7 The logic functionality realized by the given ckt,

[Gate 2016]

Set 3

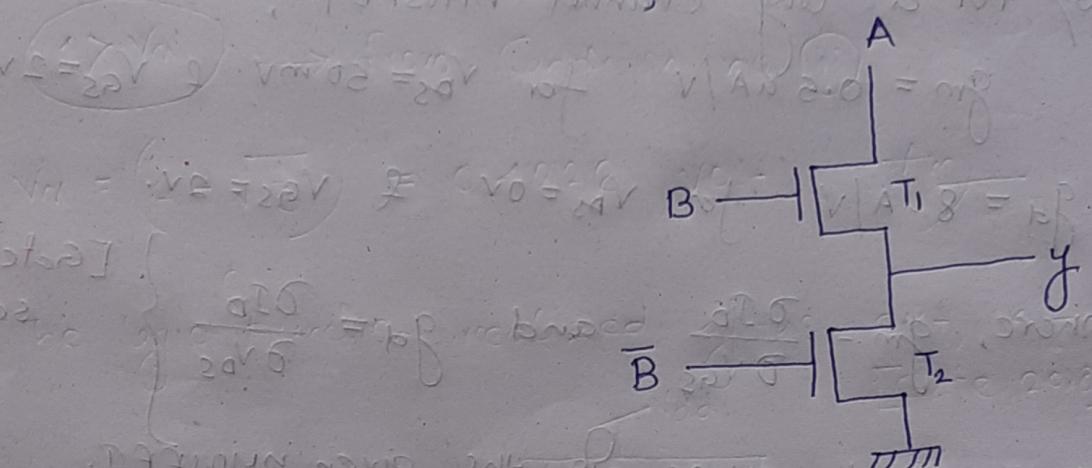


⇒ All the transistors are nMOS.

We know, when input to gate is '0' → nMOS behave as open ckt.

If input to gate is '1' → nMOS short ckt.

We can redraw the ckt as



if $B = 0$; T_2 short circuited $\rightarrow y = 0$

if $B = 1$; T_1 short circuited $\rightarrow y = A$

Truth table

A	B	y
0	0	0
1	0	0

When $B = 0$

When $B = 1$

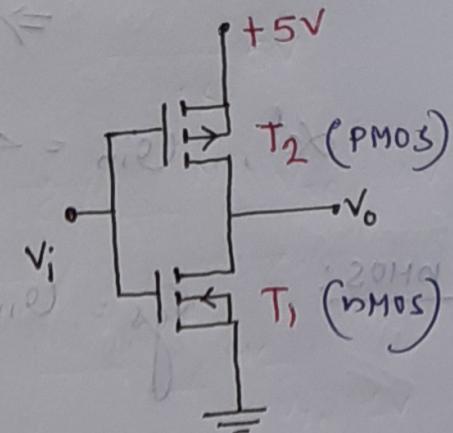
→ Given ckt behaves like AND gate.

Q1) In the given fig. Both MOS have threshold voltage of 2V. [Gate 2002]

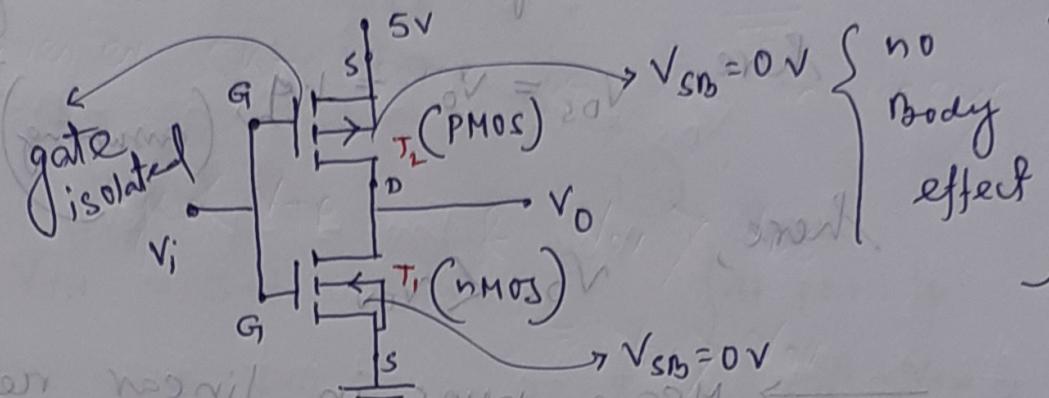
Statement 1: T_1 Conducts when $V_i > 2V$

Statement 2: T_1 always in saturation when $V_o = 0V$.

\Rightarrow Both MOS are enhancement type.



$$nV - pV = vV \quad i \quad nV < pV$$



In NMOS, $V_{TN} = 2V$

$$\text{if } V_{TP} = -2V \quad (\text{or } |V_{TP}| = 2V)$$

In Case of NMOS, $V_i = V_{GS} > 2V$; $V_{GS} > V_{TN}$

\therefore Statement 1 Correct. It will Conduct

for, Statement 2 \rightarrow we see the VTC curve, when

$V_o = 0V$, $\rightarrow T_1$ (NMOS) in linear region.

\hookrightarrow so, statement 2 is false.

\hookrightarrow Statement 1 \rightarrow TRUE
Statement 2 \rightarrow FALSE

Q27) In the CMOS inverter circuit [Gate 2007]

$$K_n = K_p = \mu_n \cdot C_{ox} \cdot \left(\frac{w}{L}\right)_n = \mu_p \cdot C_{ox} \cdot \left(\frac{w}{L}\right)_p$$

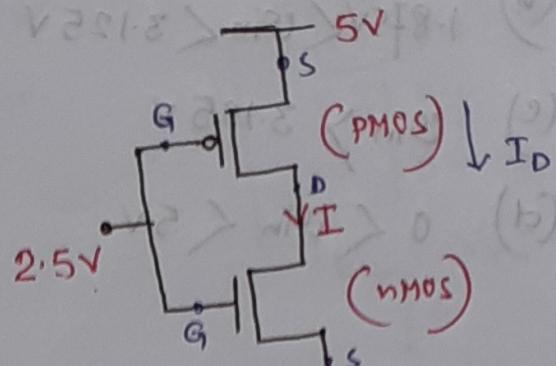
and, $V_{TN} = |V_{TP}| = 1\text{V}$

$V_L = 2.5\text{V}$ find Current I ?

According to the question,

$$V_L = V_T$$

It's Symmetric Inverter
Ckt.



Here, $V_{in} = 2.5\text{V} = \frac{V_{DD}}{2}$

This is the value of

Input, when both PMOS & NMOS are in saturation.

$$I = I_D = \mu_n \cdot C_{ox} \cdot \left(\frac{w}{L}\right)_n \left[\frac{(V_{GS} - V_{TN})^2}{2} \right]$$

$$= \frac{40 \times (2.5 - 1)^2}{2} \mu\text{A}$$

$$= 20 \times 2.25 = 45 \mu\text{A} \quad (\text{Ans})$$

$$I = I_D = \mu_p \cdot C_{ox} \cdot \left(\frac{w}{L}\right)_p \left[\frac{V_{SG} - (V_{TP})^2}{2} \right]$$

$$= \frac{K_p}{2} \left[V_{in} - 5 + 1 \right]^2$$

$$= \frac{90}{2} \left[2.5 - 5 + 1 \right]^2$$

$$= 20 \times 2.25 = 45 \mu\text{A} \quad (\text{Ans})$$

Q3.) $\mu_n = \mu_p$ & M_1 and M_2 equally sized. [Gate 2012]
 The device M_1 is in the linear region if,

- (a) $V_{in} < 1.875 V$
- (b) $1.875 V < V_{in} < 3.125 V$
- (c) $V_{in} > 3.125 V$
- (d) $0 < V_{in} < 5 V$

\Rightarrow for CMOS inverter CKT, PMOS will be in linear region, if

$$V_{gs} < V_{TP} = V_F + V_{ov} > V_{DS}$$

$$\Rightarrow V_{DS} > V_{ov}$$

$$\Rightarrow V_{DS} > V_{gs} - V_{TP}$$

$$V_{gs} = V_g - V_s \quad \text{and,}$$

$$= V_{in} - 5$$

$$V_{in} - 5 < -1$$

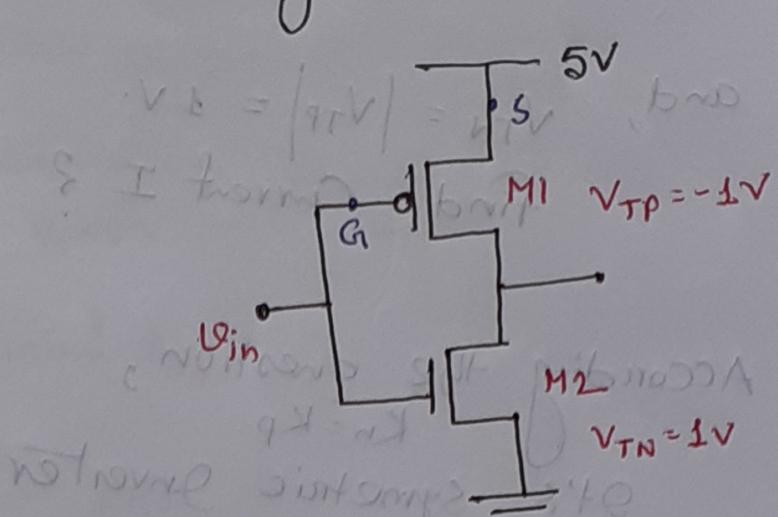
$$\Rightarrow V_{in} < 4 \text{ volt}$$

According to the NTC curve of CMOS inverter

$$[1 + \alpha_{in}] \text{ should be in between } 0 \text{ & } \frac{V_{DD}}{2}$$

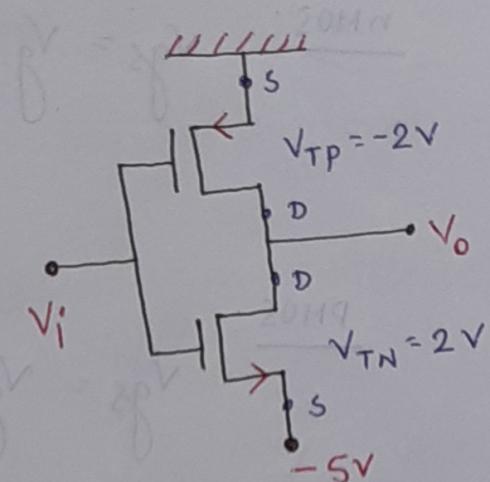
$$[1 + 2 - 2.5] \Rightarrow 0 < V_{in} < 2.5$$

∴ According to option (a) is correct.



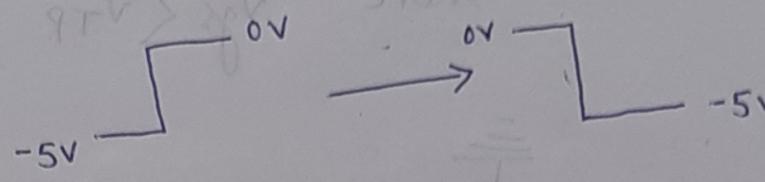
89) $V_{TN} = |V_{TP}| = 2V$ for this ckt work as a inverter
 Q: i must take the values, \rightarrow [Gate 1998]

- (a) -5V and 0V
- (b) -5V and 5V
- (c) 0V and 3V
- (d) 3V and 5V



According to the ckt, based on

(negative logic)



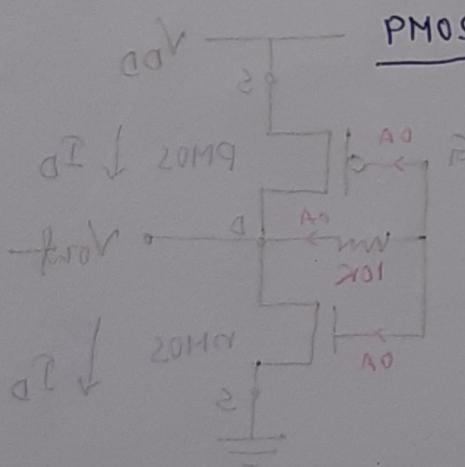
Case 1

$$\text{no overdrive} \quad V_{in} = 0V ;$$

$$\text{nMOS: } V_{gs} = V_g - V_s = (V_i + 5) \\ V_2 = 0 + 5 = 5V$$

Now, $V_{gs} > V_{TN}$ \rightarrow nMOS on condition

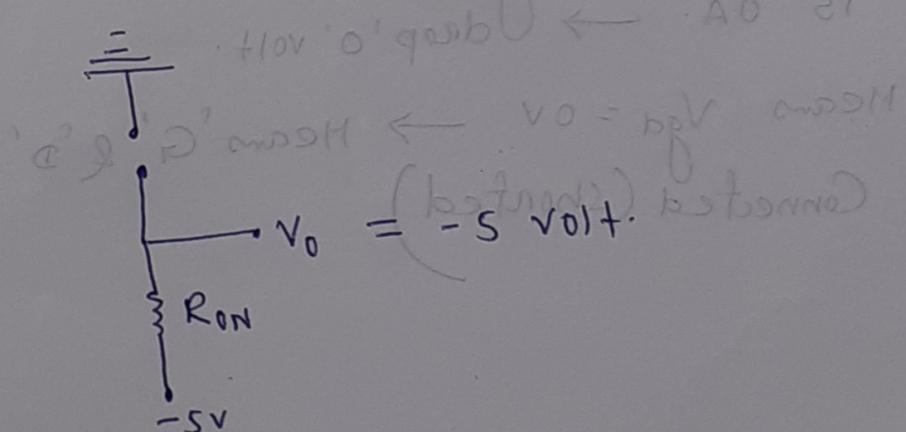
[idle state]

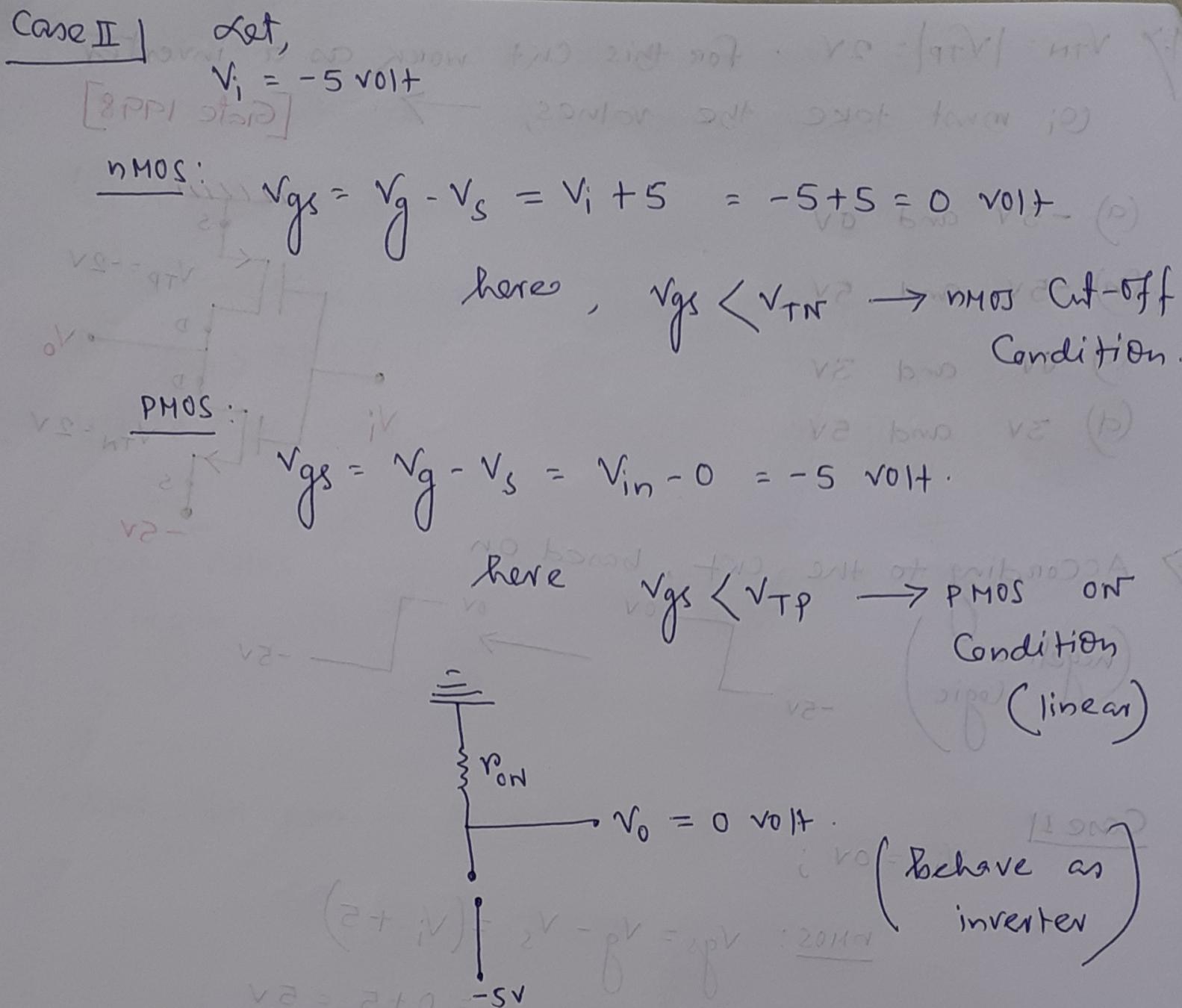


PMOS:

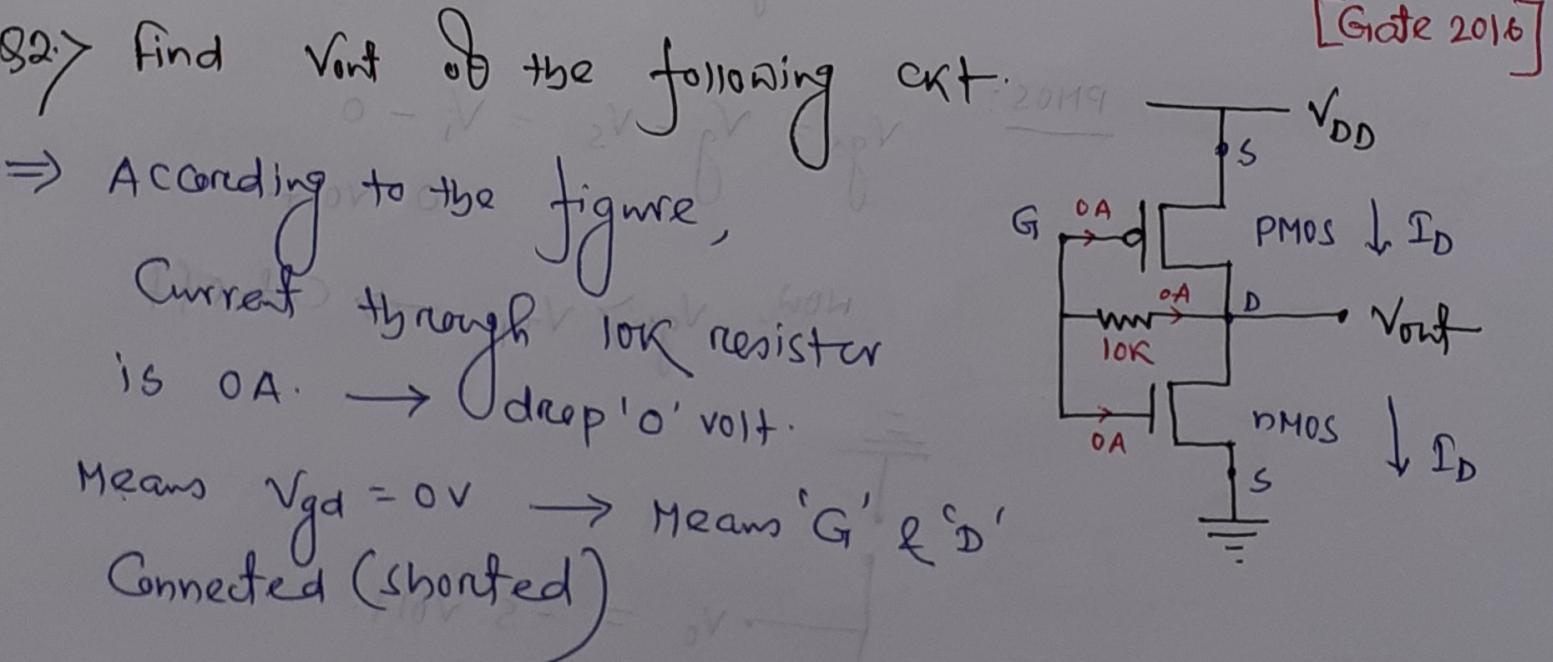
$$V_{gs} = V_g - V_s = V_i - 0$$

Now, $V_{gs} > V_{TP}$ \rightarrow Cut-off





Hence option (a) is Correct.



for nMOS $\rightarrow V_{DS} = V_{GS} - V_{TN}$

$$\downarrow$$

$$V_{DS} > V_{GS} - V_{TN} \text{ (always)}$$

$$V_{DS} = V_{GS} \Rightarrow V_{DS} > V_{OV}$$

\rightarrow Means always operate in saturation Condition

Similarly, for pmos \rightarrow It also operate in saturation Condition. ($V_{DS} < V_{OV}$)

\therefore According to the figure, both PMOS & nMOS are in saturation Condition.

\rightarrow switching occurs (V_0) between $\left\{ \frac{V_{DD}}{2} + |V_{TP}| \right\}$ to $\left\{ \frac{V_{DD}}{2} - V_{TN} \right\}$ for $V_{in} = \frac{V_{DD}}{2}$.