③ Design & verify 1-Bit Magnitude Comparator.

If we have two inputs each of single bit i.e. A & B, then comparing them

Truth table:

A	B	A<B	A=B	A>B
0	0	0	1	0
0	1	1	0	0
1	0	0	0	1
1	1	0	1	0

K-map

For $A = B$

A \ B	B' (0)	B (1)
A' (0)	(1)	0
A (1)	0	(1)

$A = B : A'B' + AB$

$= A \odot B$

For $(A < B)$

A \ B	B' (0)	B (1)
A' (0)	0	(1)
A (1)	0	0

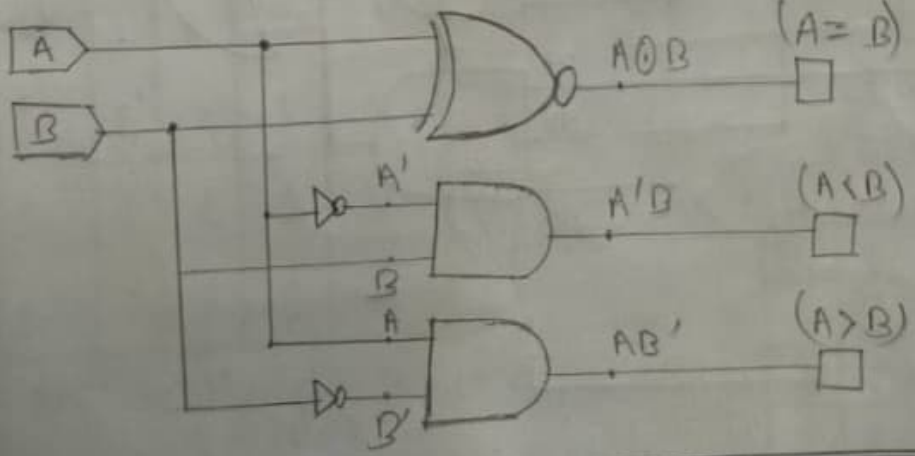
$A < B : A'B$

For $(A > B)$

A \ B	B' (0)	B (1)
A' (0)	0	0
A (1)	(1)	0

$A > B : AB'$

Circuit Diagram:-



Veer Surendra Sai University of Technology, Burla

④ Design & verify 2-bit Magnitude Comparator.

Truth table:

Inputs				Outputs		
A1	A0	B1	B0	A<B	A=B	A>B
0	0	0	0	0	1	0
0	0	0	1	1	0	0
0	0	1	0	1	0	0
0	0	1	0	1	0	0
0	1	0	0	0	0	1
0	1	0	1	0	1	0
0	1	1	0	1	0	0
0	1	1	1	1	0	0
1	0	0	0	0	0	1
1	0	0	1	0	0	1
1	0	1	0	0	1	0
1	0	1	1	1	0	0
1	1	0	0	0	0	1
1	1	0	1	0	0	1
1	1	1	0	0	0	1
1	1	1	1	0	1	0

K-map:-

For A < B

A1A0 \ B1B0	00	01	11	10
00	0 (0)	1 (1)	1 (3)	1 (2)
01	0 (4)	0 (5)	1 (7)	1 (6)
11	0 (12)	0 (13)	0 (15)	0 (14)
10	0 (8)	0 (9)	1 (11)	0 (10)

(A<B): $A1'B1 + A1'A0'B0 + A0'B1B0$

For A > B

A1A0 \ B1B0	00	01	11	10
00	0 (0)	0 (1)	0 (3)	0 (2)
01	1 (4)	0 (5)	0 (7)	0 (6)
11	1 (12)	1 (13)	0 (15)	1 (14)
10	1 (8)	1 (9)	0 (11)	0 (10)

(A>B): $A1B1' + A1A0B0' + A0B1'B0'$

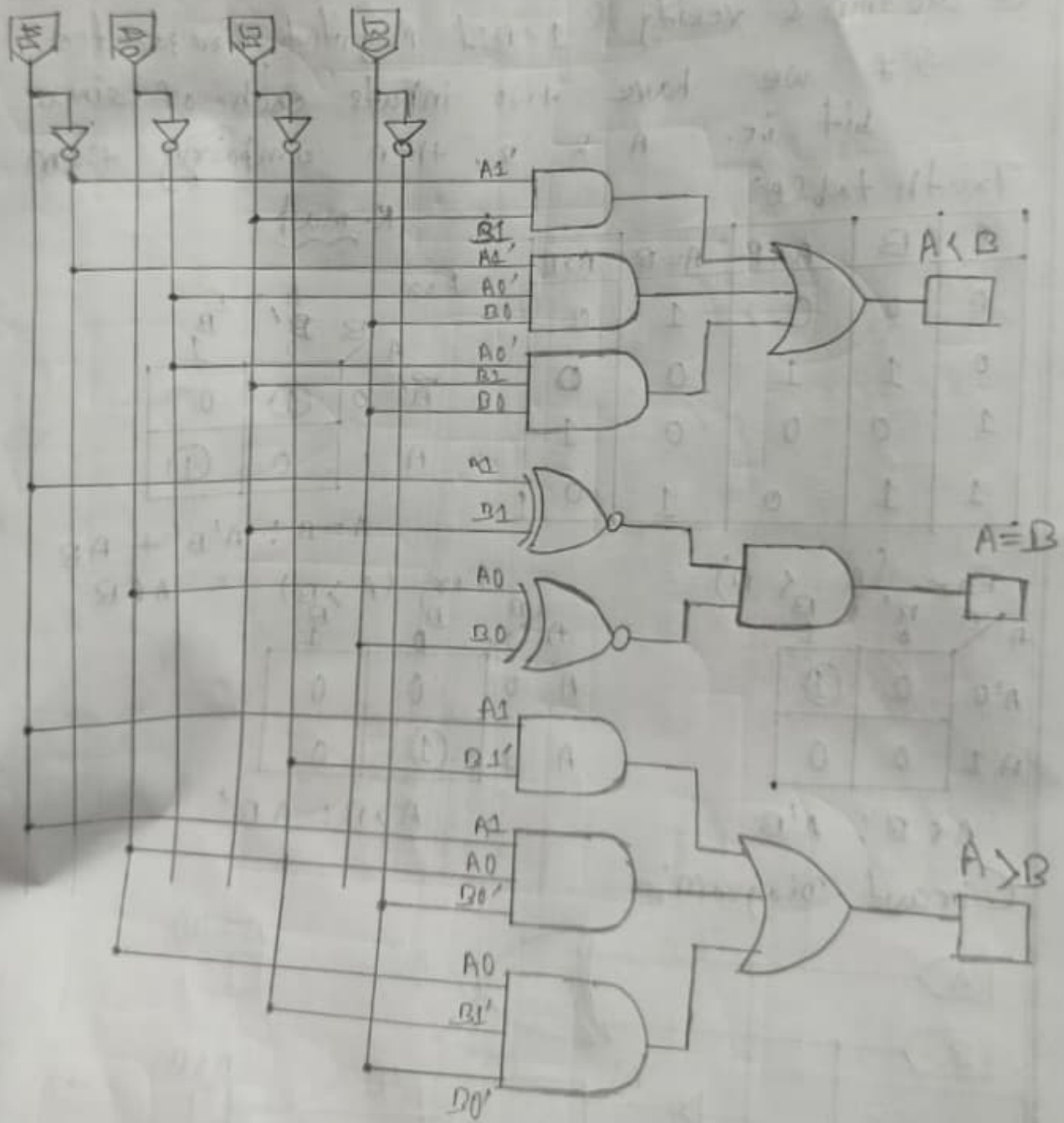
For (A=B)

A1A0 \ B1B0	00	01	11	10
00	1	0	0	0
01	0	1	0	0
11	0	0	1	0
10	0	0	0	1

$(A=B) = A1'A0'B1'B0' + A1'A0B1'B0 + A1A0B1B0 + A1A0'B1B0'$

$(A=B) = (A0B0 + A0'B0')(A1B1 + A1'B1')$

Circuit Diagram:



Veer Surendra Sai University of Technology, Burla

⑤ Design & verify 4-bit Magnitude Comparator.

In a 4-bit Comparator $A = B$, if and only if

$A3 = B3$ and $A2 = B2$ and $A1 = B1$ and $A0 = B0$

if $x_i = A_iB_i + A_i'B_i'$ for $i = 0, 1, 2, 3$

$(A = B)$: $x_3 . x_2 . x_1 . x_0$

$A < B$ is possible, if $A3 = 0$ and $B3 = 1$

or $A3 = B3$, $A2 = 0$ and $B2 = 1$

or $A3 = B3$, $A2 = B2$, $A1 = 0$ and $B1 = 1$

or $A3 = B3$, $A2 = B2$, $A1 = B1$, $A0 = 0$ and $B0 = 1$

so $(A < B)$: $A3'B3 + x_3 A2'B2 + x_3 x_2 A1'B1 + x_3 x_2 x_1 A0'B0$

$A > B$ is possible, if $A3 = 1$ and $B3 = 0$

or $A3 = B3$, $A2 = 1$ and $B2 = 0$

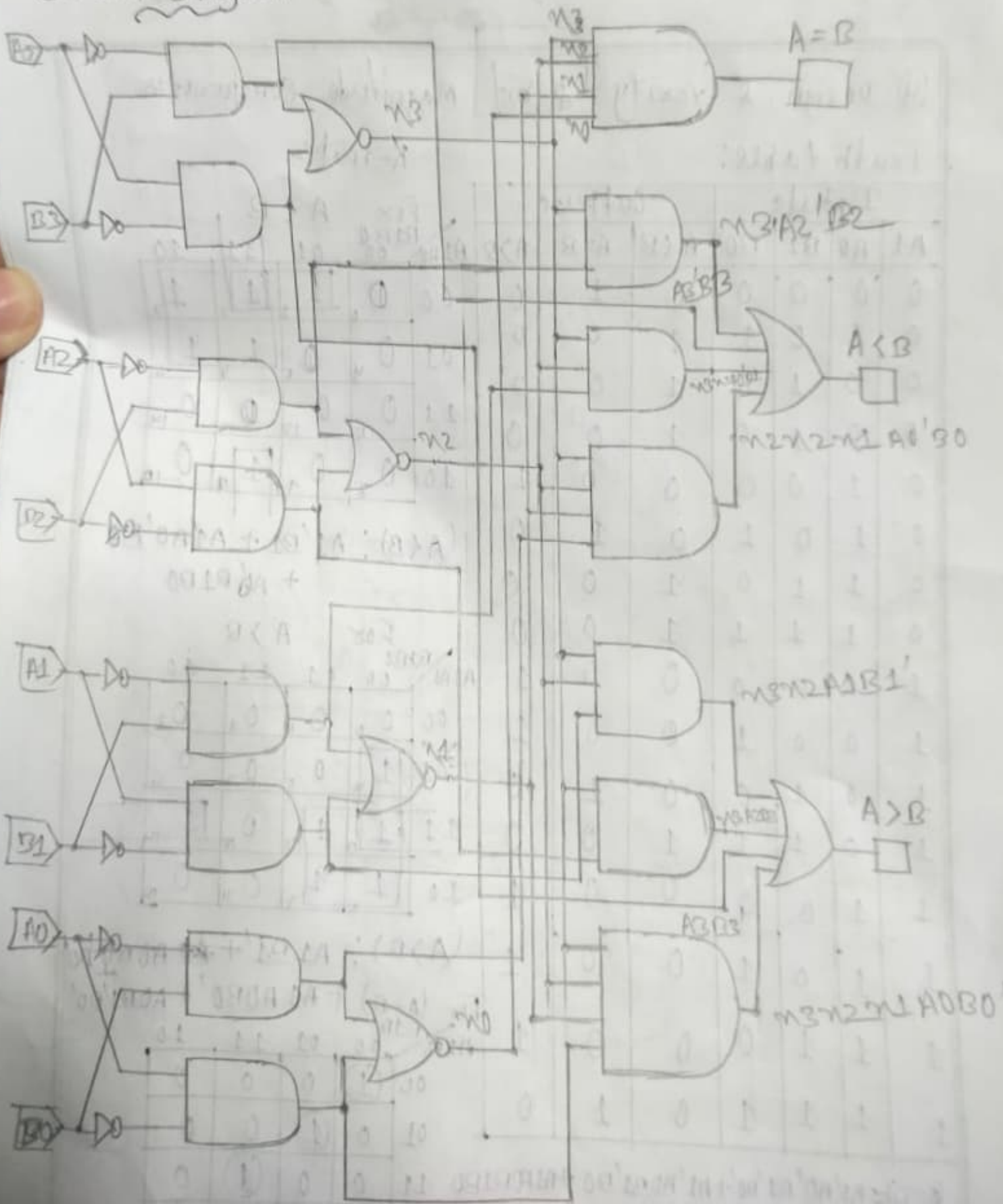
or $A2 = B3$, $A2 = B2$ and $A1 = 1$ and $B1 = 0$

or $A3 = B3$, $A2 = B2$, $A1 = B1$, $A0 = 1$ and $B0 = 0$

so $(A > B)$: $A3B3' + x_3 A2B2' + x_3 x_2 A1B1' + x_3 x_2 x_1 A0B0'$

Name: Sumit Sekhar Kundu
Regd. no.: 2302041051
Section: CSE-2

Circuit Diagram:-



Aim of the Experiment :-

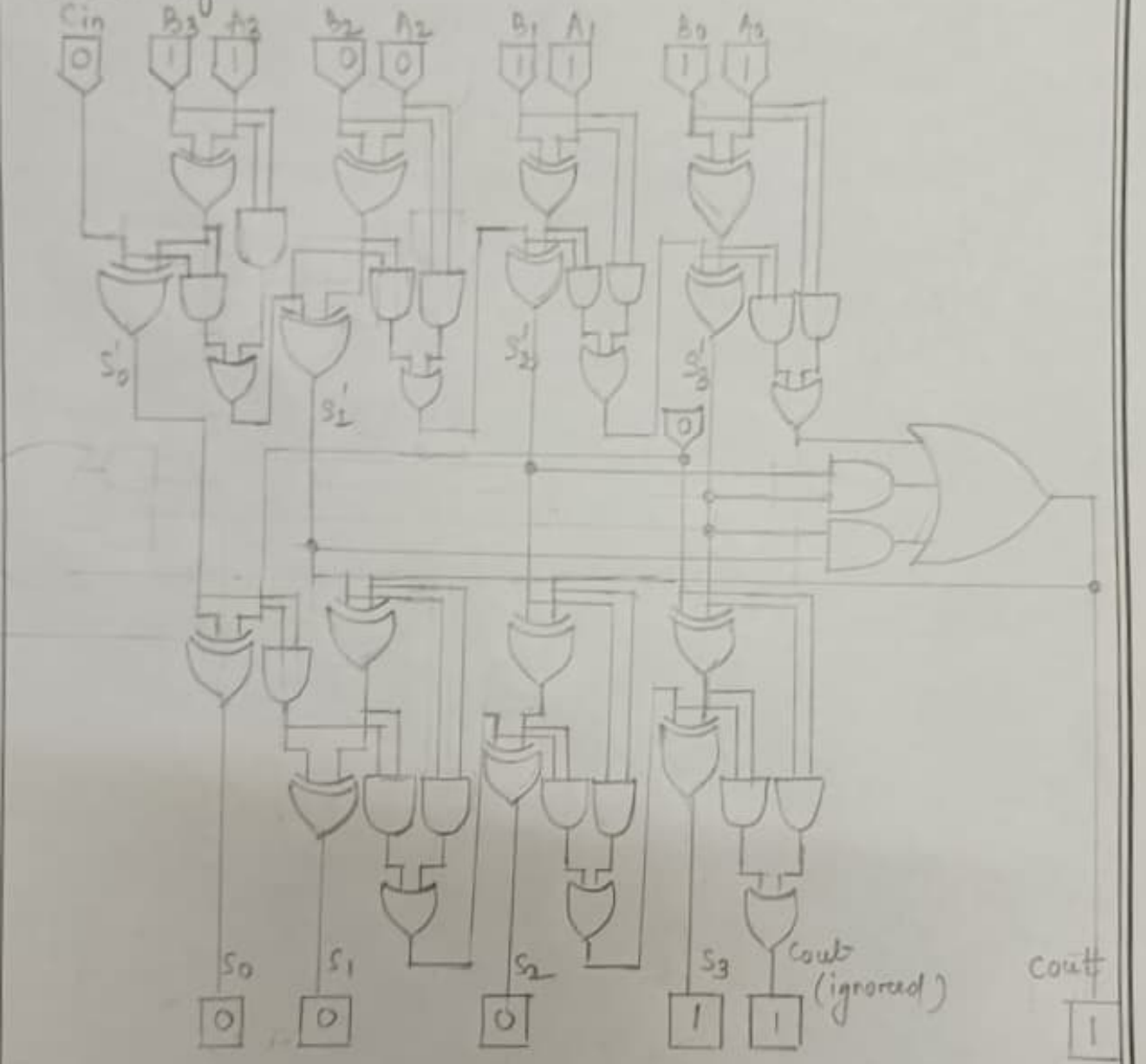
To design and verify BCD adder.

TRUTH TABLE:-

Cin	A				B				BCD Sum				Carry
	A3	A2	A1	A0	B3	B2	B1	B0	S3	S2	S1	S0	Cout
0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	0	1	0	0	0	1	0	0	0	1	0
0	0	0	1	0	0	0	1	0	0	0	1	0	0
0	0	0	1	1	0	0	1	1	0	0	1	1	0
0	0	1	0	0	0	1	0	0	0	1	0	0	0
0	0	1	0	1	0	1	0	1	0	1	0	1	0
0	0	1	1	0	0	1	1	0	0	1	1	0	0
0	0	1	1	1	0	1	1	1	0	1	1	1	0
0	1	0	0	0	1	0	0	0	1	0	0	0	0
0	1	0	0	1	1	0	0	1	1	0	0	1	0
0	1	0	1	0	1	0	1	0	0	0	0	0	1
0	1	0	1	1	1	0	1	1	0	0	0	1	1
0	1	1	0	0	1	1	0	0	0	0	1	0	1
0	1	1	0	1	1	1	0	1	0	0	1	1	1
0	1	1	1	0	1	1	1	0	0	1	0	0	1
0	1	1	1	1	1	1	1	1	0	1	0	1	1
0	0	0	0	0	0	0	0	0	0	1	1	0	1
0	0	0	0	1	0	0	0	1	0	1	1	1	1
0	0	0	1	0	0	0	1	0	1	0	0	0	1
0	0	0	1	1	0	0	1	1	1	0	0	1	1

Veer Surendra Sai University of Technology, Burla

Circuit Diagram :-



...] To design & Verify adder substractor

TRUTH TABLE :-

A					B				Sum				Carry
Cin	A_3	A_2	A_1	A_0	B_3	B_2	B_1	B_0	S_3	S_2	S_1	S_0	Cout
0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	0	1	0	0	0	1	0	0	1	0	0
0	0	0	1	0	0	0	1	0	0	1	0	0	0
0	0	0	1	1	0	0	1	1	0	1	1	0	0
0	0	1	0	0	0	1	0	0	1	0	0	0	0
0	0	1	0	1	0	1	0	1	1	0	1	0	0
0	0	1	1	0	0	1	1	0	1	1	0	0	0
0	0	1	1	1	0	1	1	1	1	1	1	0	0
0	1	0	0	0	1	0	0	0	0	0	0	0	1
0	1	0	0	1	1	0	0	1	0	0	1	0	1
0	1	0	1	0	1	0	1	0	0	1	0	0	1
0	1	0	1	1	1	0	1	1	0	1	1	0	1
0	1	1	0	0	1	1	0	0	1	0	0	0	1
0	1	1	0	1	1	1	0	1	1	0	1	0	1
0	1	1	1	0	1	1	1	0	1	1	0	0	1
0	1	1	1	1	1	1	1	1	1	1	1	0	1

Veer Surendra Sai University of Technology, Burla

Logic 1

Circuit Diagram:-