

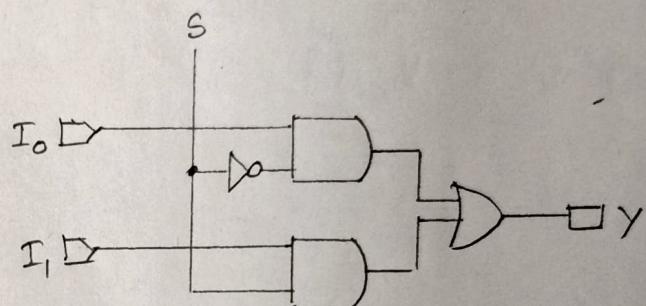
AIM OF THE EXPERIMENT:

- To design and verify 2:1, 4:1, 8:1 & 16:1 multiplexers.
- Implement multiplexers as universal logic circuit.
- Implement circuits using multiplexers.

Design & Verify of 2:1, 4:1, 8:1 & 16:1 multiplexers:-2:1 MultiplexerInput, $n=2$ Control lines, $m = \log_2 2 = 1$

S_0	Y
0	I_0
1	I_1

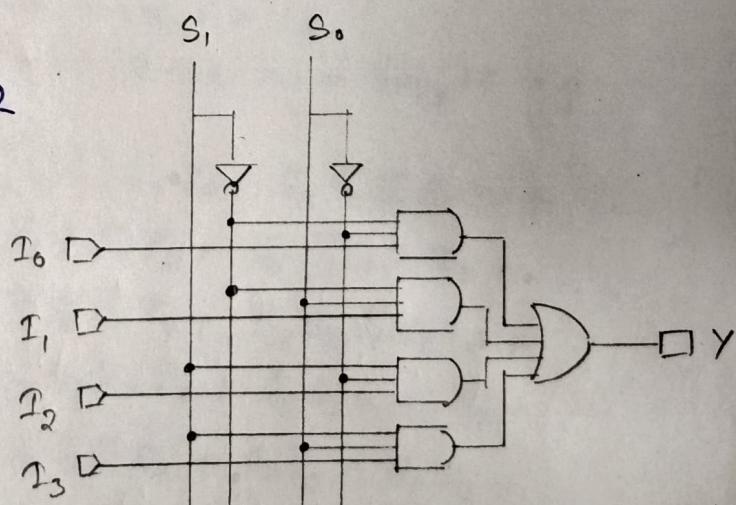
$$Y = \overline{S}_0 I_0 + S_0 I_1$$



Truth Table of 2:1 MUX

4:1 MultiplexerInput, $n=4$ Control lines, $m = \log_2 4 = 2$

S_1	S_0	Y
0	0	I_0
0	1	I_1
1	0	I_2
1	1	I_3



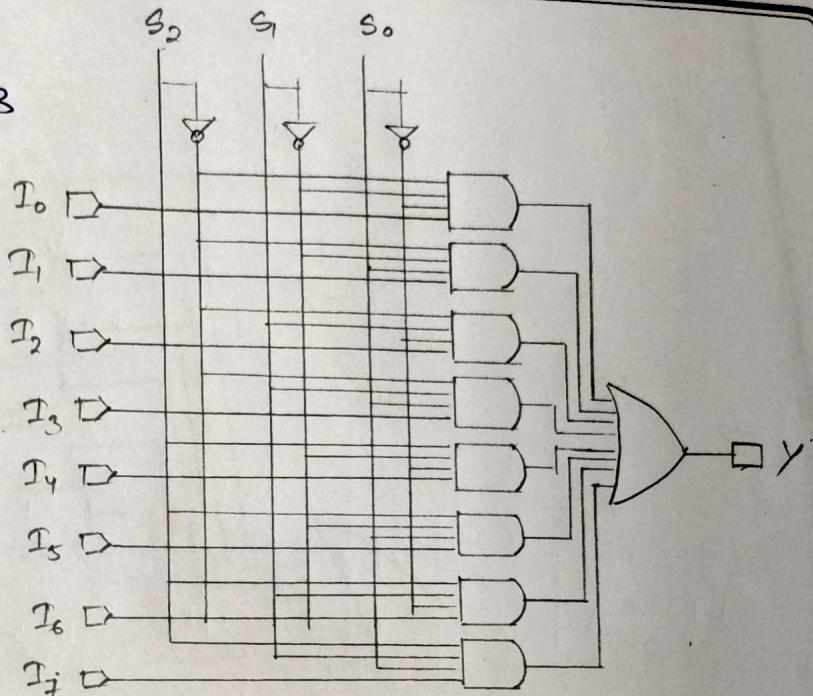
$$Y = \overline{S}_1 \overline{S}_0 I_0 + \overline{S}_1 S_0 I_1 + \overline{S}_1 S_0 I_2 + S_1 S_0 I_3$$

8:1 Multiplexer:-

Input lines, $n = 8$

Control lines, $m = \log_2 8 = 3$

S_2	S_1	S_0	Y
0	0	0	I_0
0	0	1	I_1
0	1	0	I_2
0	1	1	I_3
1	0	0	I_4
1	0	1	I_5
1	1	0	I_6
1	1	1	I_7



$$Y = \bar{S}_2 \bar{S}_1 \bar{S}_0 I_0 + \bar{S}_2 \bar{S}_1 S_0 I_1 + \bar{S}_2 S_1 \bar{S}_0 I_2 + \bar{S}_2 S_1 S_0 I_3 + \\ S_2 \bar{S}_1 \bar{S}_0 I_4 + S_2 \bar{S}_1 S_0 I_5 + S_2 S_1 \bar{S}_0 I_6 + S_2 S_1 S_0 I_7$$

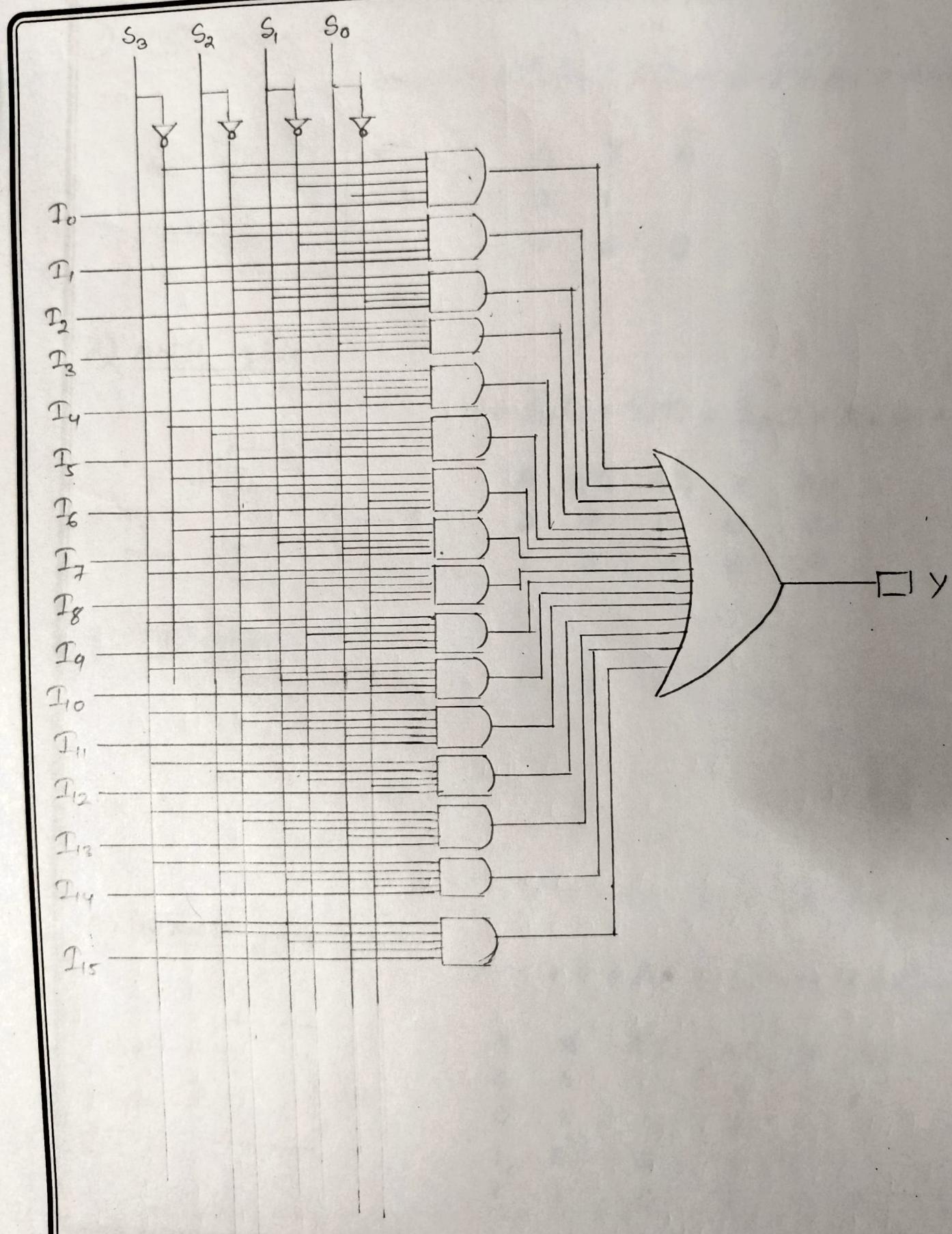
16:1 Multiplexer:-

S_3	S_2	S_1	S_0	Y
0	0	0	0	I_0
0	0	0	1	I_1
0	0	1	0	I_2
0	0	1	1	I_3
0	1	0	0	I_4
0	1	0	1	I_5
0	1	1	0	I_6
0	1	1	1	I_7
1	0	0	0	I_8
1	0	0	1	I_9
1	0	1	0	I_{10}
1	0	1	1	I_{11}
1	1	0	0	I_{12}
1	1	0	1	I_{13}
1	1	1	0	I_{14}
1	1	1	1	I_{15}

Input lines, $n = 16$

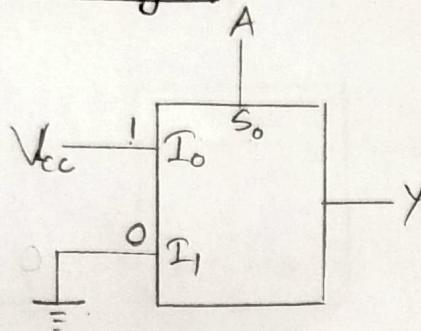
Control lines, $m = \log_2 16 = 4$

$$Y = \bar{S}_3 \bar{S}_2 \bar{S}_1 \bar{S}_0 I_0 + \bar{S}_3 \bar{S}_2 \bar{S}_1 S_0 I_1 + \\ \bar{S}_3 \bar{S}_2 S_1 \bar{S}_0 I_2 + \bar{S}_3 \bar{S}_2 S_1 S_0 I_3 + \\ S_3 \bar{S}_2 \bar{S}_1 \bar{S}_0 I_4 + \bar{S}_3 S_2 \bar{S}_1 \bar{S}_0 I_5 + \\ \bar{S}_3 S_2 S_1 \bar{S}_0 I_6 + \bar{S}_3 S_2 S_1 S_0 I_7 + \\ S_3 \bar{S}_2 \bar{S}_1 \bar{S}_0 I_8 + S_3 \bar{S}_2 \bar{S}_1 S_0 I_9 + \\ S_3 \bar{S}_2 S_1 \bar{S}_0 I_{10} + S_3 \bar{S}_2 S_1 S_0 I_{11} + \\ S_3 S_2 \bar{S}_1 \bar{S}_0 I_{12} + S_3 S_2 \bar{S}_1 S_0 I_{13} + \\ S_3 S_2 S_1 \bar{S}_0 I_{14} + S_3 S_2 S_1 S_0 I_{15}.$$



Multiplexer as universal logic circuit:

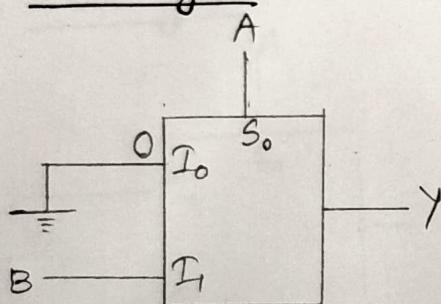
1) NOT gate:



$$Y = \bar{S}_0 I_0 + S_0 I_1 = \bar{A} \cdot 1 + A \cdot 0 = \bar{A}$$

A	Y	\bar{A}
0	1	1
1	0	0

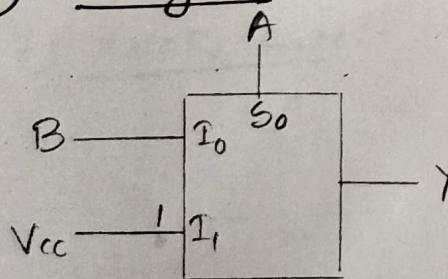
2) AND gate:



$$Y = \bar{S}_0 I_0 + S_0 I_1 = \bar{A} \cdot 0 + A \cdot B = AB$$

A	$\bar{A}I_0$	$A I_1$	Y	AB
0	0	0	0	0
1	0	B	B	B

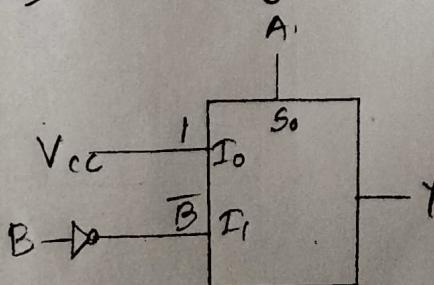
3) OR gate:



A	B	$\bar{A}I_0$	$A I_1$	Y	$A+B$
0	0	0	0	0	0
0	1	1	0	1	1
1	0	0	1	1	1
1	1	0	1	1	1

$$Y = \bar{A}B + A = (A + \bar{A})(A + B) = A + B$$

4) NAND gate:

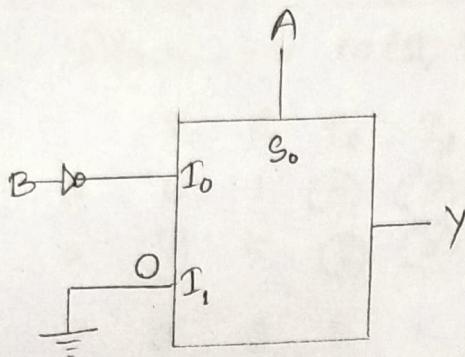


$$Y = 1 \cdot \bar{A} + A\bar{B} = (\bar{A} + A)(\bar{A} + \bar{B}) = \bar{A} + \bar{B} = \overline{AB}$$

A	B	$\bar{A}I_0$	$A I_1$	Y	\overline{AB}
0	0	1	0	1	1
0	1	1	0	1	1
1	0	0	1	1	1
1	1	0	0	0	0

5) NOR gate :-

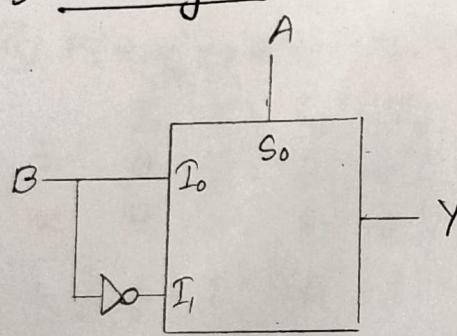
$$Y = \overline{A}\overline{B} + A \cdot 0 = \overline{A}\overline{B} = \overline{A+B}$$



A	B	$\overline{A}I_0$	$A\overline{I}_1$	Y	$\overline{A+B}$
0	0	1	0	1	1
0	1	0	0	0	0
1	0	0	0	0	0
1	1	0	0	0	0

6) XOR gate :-

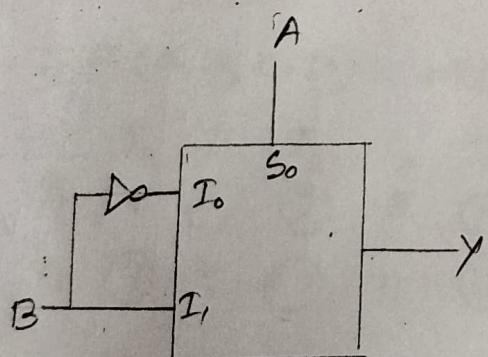
$$Y = \overline{A}B + A\overline{B} = A \oplus B$$



A	B	$\overline{A}I_0$	$A\overline{I}_1$	Y	$A \oplus B$
0	0	0	0	0	0
0	1	1	0	1	1
1	0	0	1	1	1
1	1	0	0	0	0

7) XNOR Gate :-

$$Y = \overline{A}\overline{B} + AB = A \odot B$$



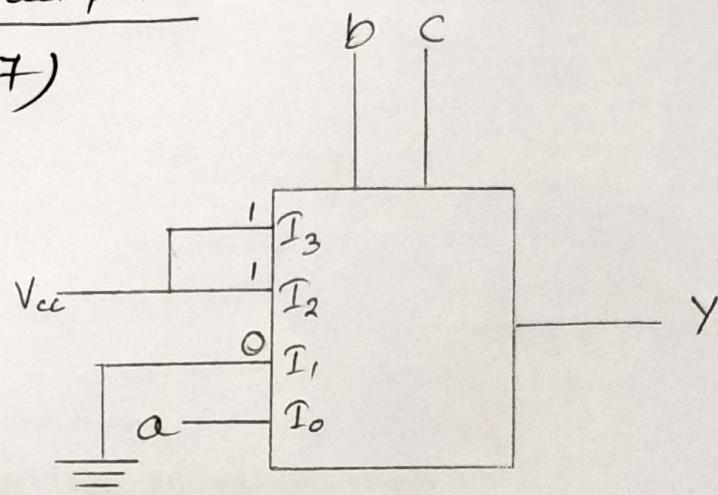
A	B	$\overline{A}I_0$	$A\overline{I}_1$	Y	$A \odot B$
0	0	1	0	1	1
0	1	0	0	0	0
1	0	0	0	0	0
1	1	0	1	1	1

Implement following using multiplexers:

i) $F(a, b, c) = m(2, 3, 4, 6, 7)$

	I_0	I_1	I_2	I_3
\bar{a}	0	1	2	3
a	4	5	6	7
a	0	1	1	

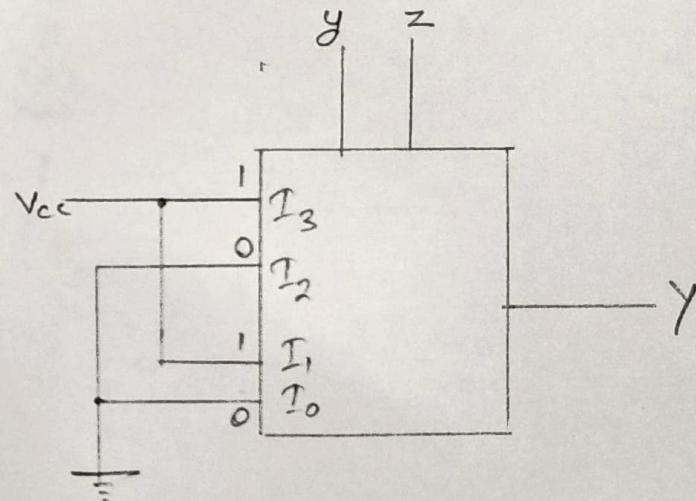
b, c are select lines



ii) $F(x, y, z) = m(1, 3, 5, 7)$

	I_0	I_1	I_2	I_3
\bar{x}	0	1	2	3
x	4	5	6	7
	0	1	0	1

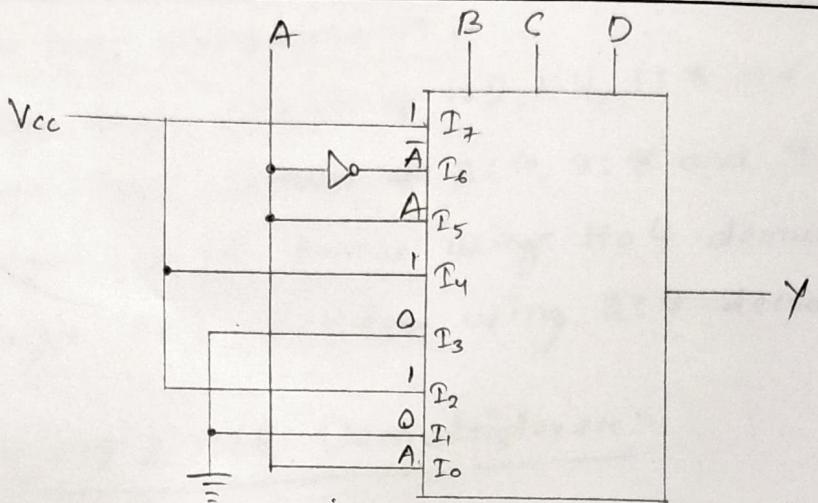
y, z are select lines



iii) $F(A, B, C, D) = m(2, 4, 6, 7, 8, 10, 12, 13, 15)$

	I_0	I_1	I_2	I_3	I_4	I_5	I_6	I_7
\bar{A}	0	1	2	3	4	5	6	7
A	8	9	10	11	12	13	14	15
A	0	1	0	1	A	\bar{A}	1	

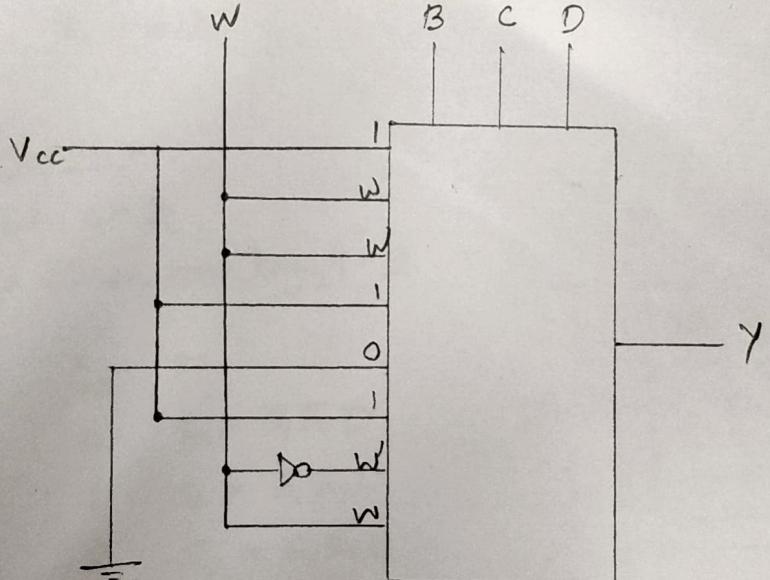
$B, C \& D$ are select lines.



$$iv) F(w, x, y, z) = m(1, 2, 4, 7, 8, 10, 12, 13, 14, 15)$$

	I_0	I_1	I_2	I_3	I_4	I_5	I_6	I_7
\bar{w}	0	1	2	3	4	5	6	7
w	8	9	10	11	12	13	14	15

w \bar{w} 1 0 1 w w 1



AIM OF THE EXPERIMENT :-

- Design logic circuit of 1:2, 1:4, 1:8 and 1:16 demultiplexers
- Design logic circuit of 2:4, 3:8 and 4:16 decoders
- Design 1 to 16 demux using 1 to 4 demux
- Design 3:8 decoder using 2:4 decoder

1:2, 1:4, 1:8 & 1:16 Demultiplexer:-

1:2 Demux:-

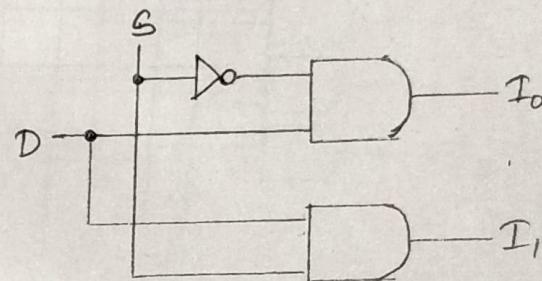
Output, $n=2$

Select lines, $m = \log_2 2 = 1$

$S \quad F$

$$0 \quad I_0 = \bar{S}D$$

$$1 \quad I_1 = SD$$



1:4 Demux:-

Output, $n=4$

Select lines, $m = \log_2 4 = 2$

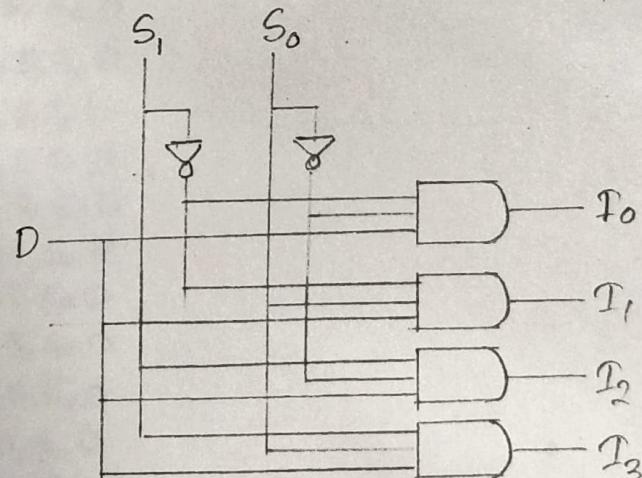
$S_1 \quad S_0 \quad F$

$$0 \quad 0 \quad I_0 = \bar{S}_1 \bar{S}_0 D$$

$$0 \quad 1 \quad I_1 = \bar{S}_1 S_0 D$$

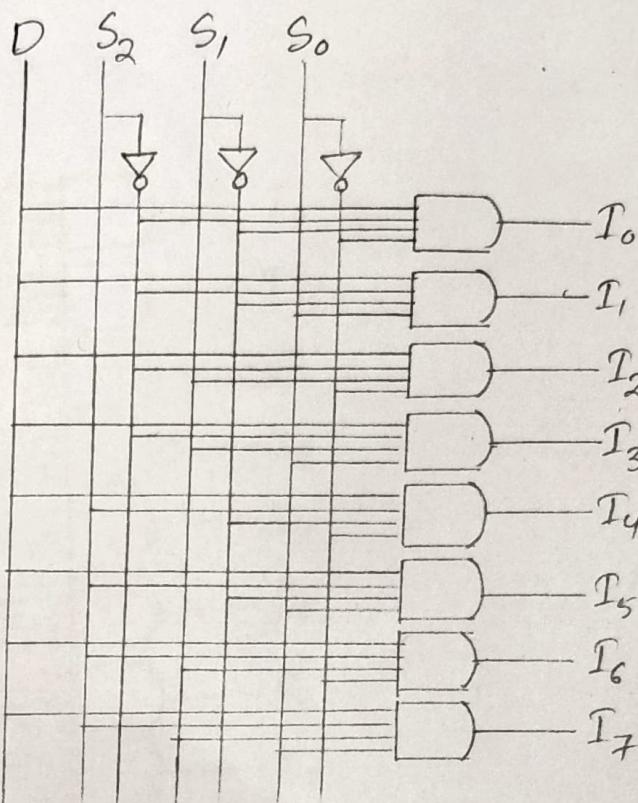
$$1 \quad 0 \quad I_2 = S_1 \bar{S}_0 D$$

$$1 \quad 1 \quad I_3 = S_1 S_0 D$$



1:8 Demux:-

S_2	S_1	S_0	F
0	0	0	$I_0 = \bar{S}_2 \bar{S}_1 \bar{S}_0 D$
0	0	1	$I_1 = \bar{S}_2 \bar{S}_1 S_0 D$
0	1	0	$I_2 = \bar{S}_2 S_1 \bar{S}_0 D$
0	1	1	$I_3 = \bar{S}_2 S_1 S_0 D$
1	0	0	$I_4 = S_2 \bar{S}_1 \bar{S}_0 D$
1	0	1	$I_5 = S_2 \bar{S}_1 S_0 D$
1	1	0	$I_6 = S_2 S_1 \bar{S}_0 D$
1	1	1	$I_7 = S_2 S_1 S_0 D$

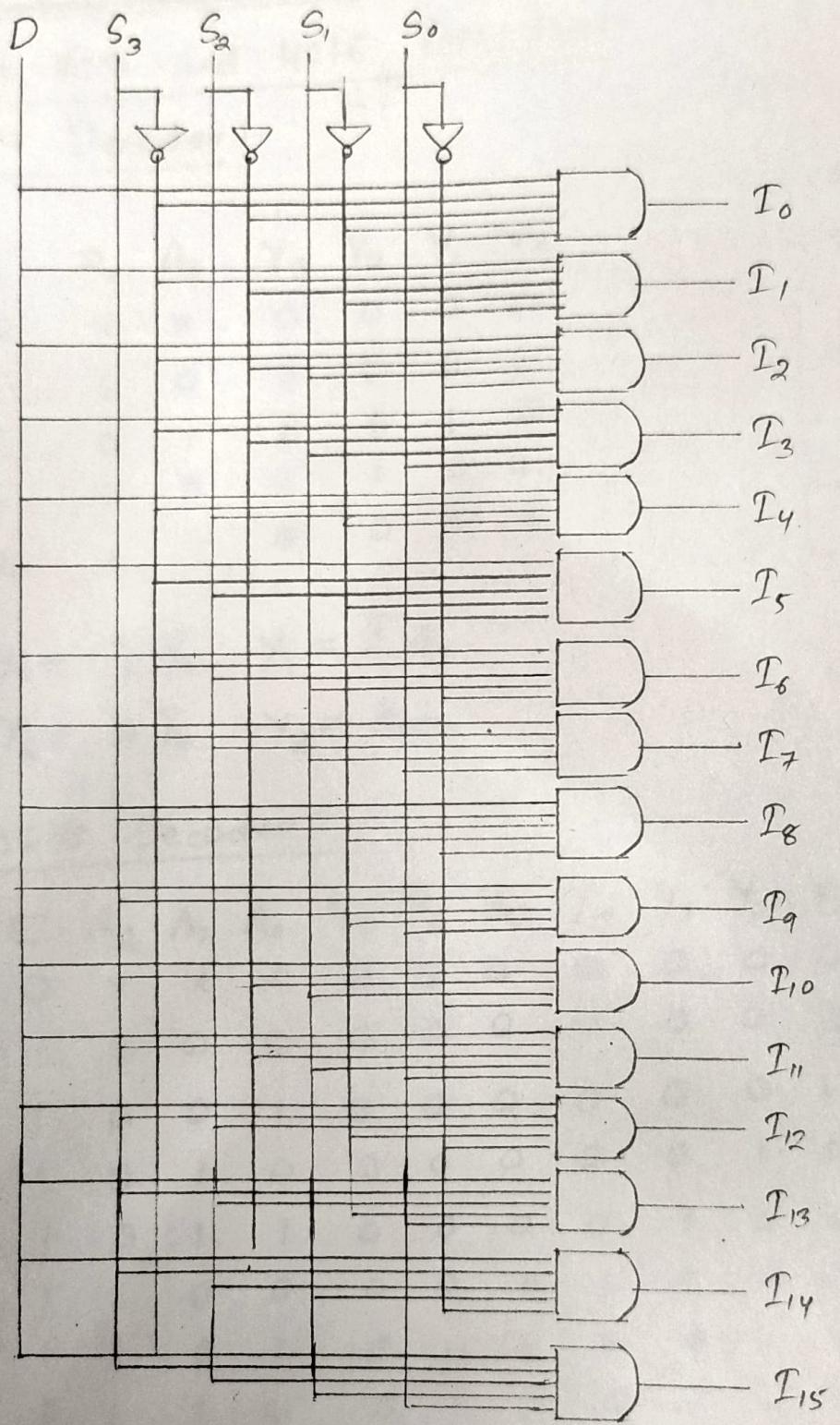


1:16 Demux:-

S_3	S_2	S_1	S_0	F
0	0	0	0	$I_0 = \bar{S}_3 \bar{S}_2 \bar{S}_1 \bar{S}_0 D$
0	0	0	1	$I_1 = \bar{S}_3 \bar{S}_2 \bar{S}_1 S_0 D$
0	0	1	0	$I_2 = \bar{S}_3 \bar{S}_2 S_1 \bar{S}_0 D$
0	0	1	1	$I_3 = \bar{S}_3 \bar{S}_2 S_1 S_0 D$
0	1	0	0	$I_4 = \bar{S}_3 S_2 \bar{S}_1 \bar{S}_0 D$
0	1	0	1	$I_5 = \bar{S}_3 S_2 \bar{S}_1 S_0 D$
0	1	1	0	$I_6 = \bar{S}_3 S_2 S_1 \bar{S}_0 D$
0	1	1	1	$I_7 = \bar{S}_3 S_2 S_1 S_0 D$
1	0	0	0	$I_8 = S_3 \bar{S}_2 \bar{S}_1 \bar{S}_0 D$
1	0	0	1	$I_9 = S_3 \bar{S}_2 \bar{S}_1 S_0 D$
1	0	1	0	$I_{10} = S_3 \bar{S}_2 S_1 \bar{S}_0 D$
1	0	1	1	$I_{11} = S_3 \bar{S}_2 S_1 S_0 D$
1	1	0	0	$I_{12} = S_3 S_2 \bar{S}_1 \bar{S}_0 D$
1	1	0	1	$I_{13} = S_3 S_2 \bar{S}_1 S_0 D$
1	1	1	0	$I_{14} = S_3 S_2 S_1 \bar{S}_0 D$
1	1	1	1	$I_{15} = S_3 S_2 S_1 S_0 D$

Output, $n=16$

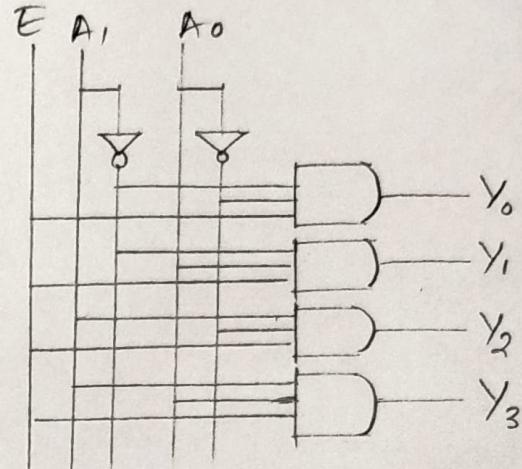
Select Lines, $m = \log_2 16 = 4$



2:4, 3:8 and 4:16 Decoders:-

2:4 Decoder :-

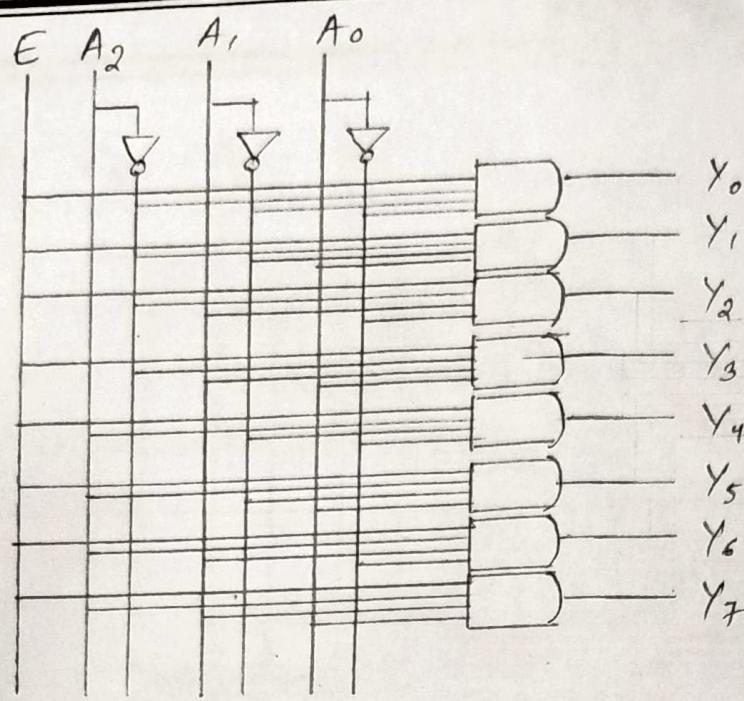
E	A_1	A_0	y_3	y_2	y_1	y_0
0	x	x	0	0	0	0
1	0	0	0	0	0	1
1	0	1	0	0	1	0
1	1	0	0	1	0	0
1	1	1	01	0	0	0



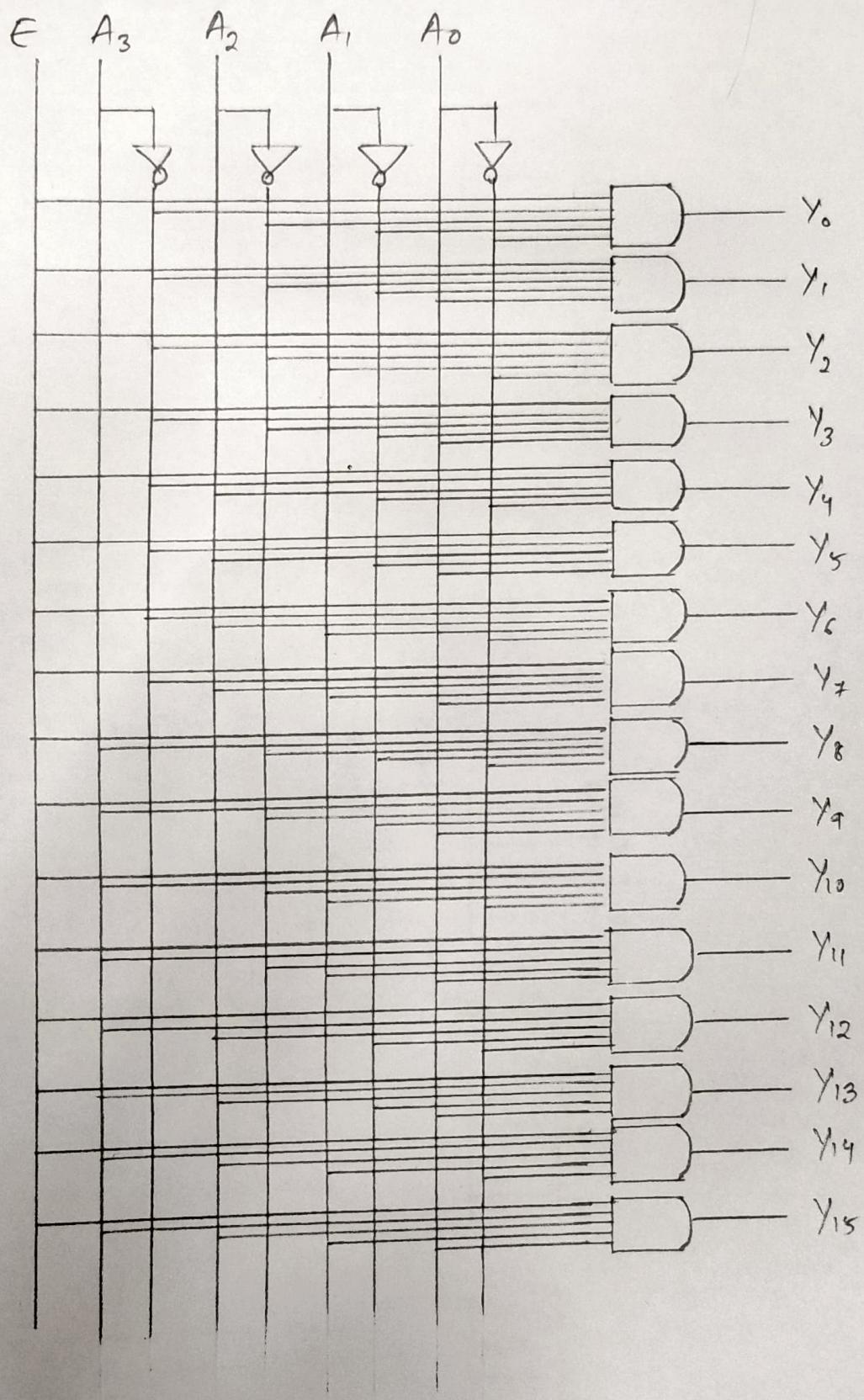
$$Y_0 = \bar{A}_1 \bar{A}_0 \quad Y_1 = \bar{A}_1 A_0$$

$$Y_2 = A_1 \bar{A}_0 \quad Y_3 = A_1 A_0$$

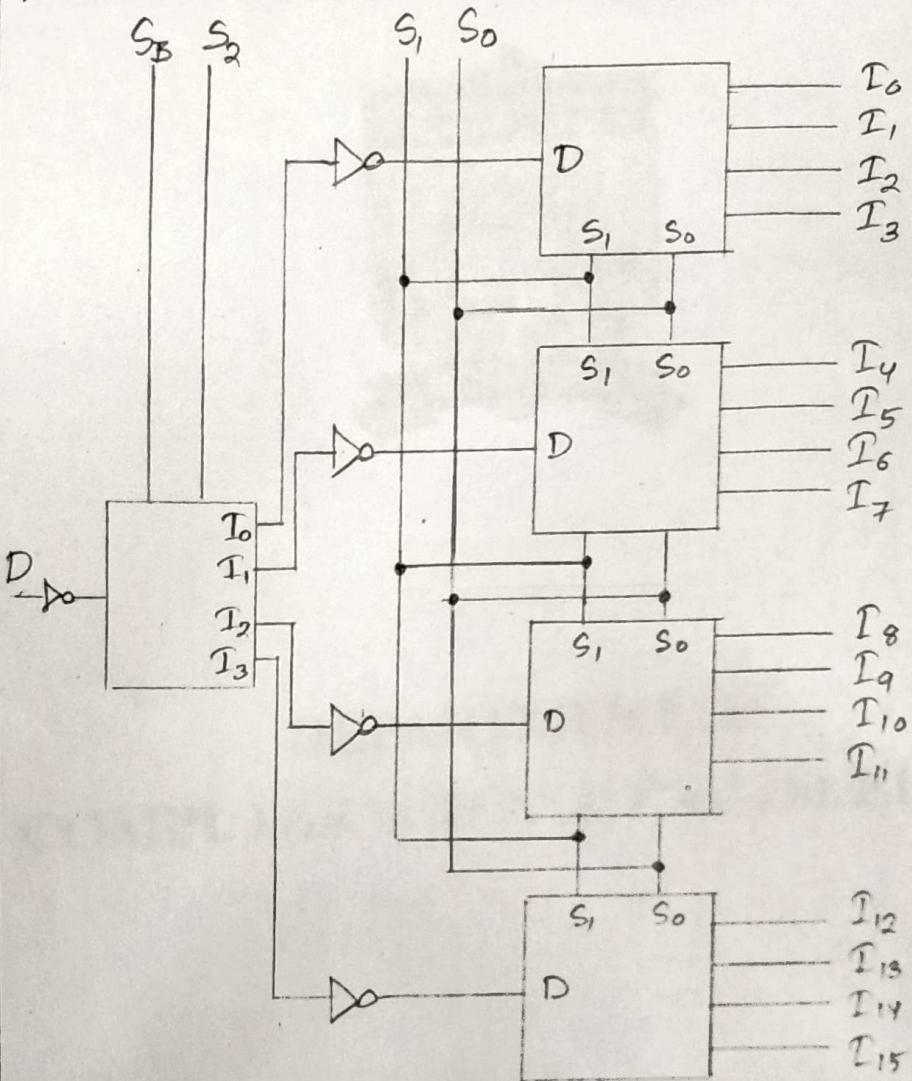
3:8 Decoder :-



4:16 Decoder :-



1:16 Demux using 1:4 Demux:-



3:8 Decoder using 2:4 decoder:-

