• Diode under no biased condition

→ Near the junction the e⁻ from n-type recombine from the free holes from p-type leaving the immoble iones

→ This oppositely charge ions in both sides are called as space charge region

→ The electric field created by the space charge region opposes the diffusion process or recombination process of e⁻ and holes

→ There are two con phenomenon the diffusion ~~and~~ or recombination process

↳ creates more space charge region and electric field (generated by space charge) that tend to counteract the recombination process.

→ Near the junction no free charge carriers are available so it is called 'depletion region'.

• Diode under forward biased condition

Diode current equation

$$I_D = I_S\left(e^{V/\eta V_T} - 1\right)$$

$V_T \rightarrow$ ~~Threshold~~ voltage equivalent of temperature

I_D - current through Diode

V — Voltage across diode

η — constant $= 1 \rightarrow$ (Germanium)

$= 2 \rightarrow$ (silicon) $(V < V_T)$

or 1 ↳ if $(V > V_T)$

$$V_T = \frac{T(K) \times k}{q}$$

$k \rightarrow$ Boltzman constant

$q \rightarrow$ charge

$T \rightarrow$ temp in K.

$1.6 \times 10^{-19} C = 1 eV$

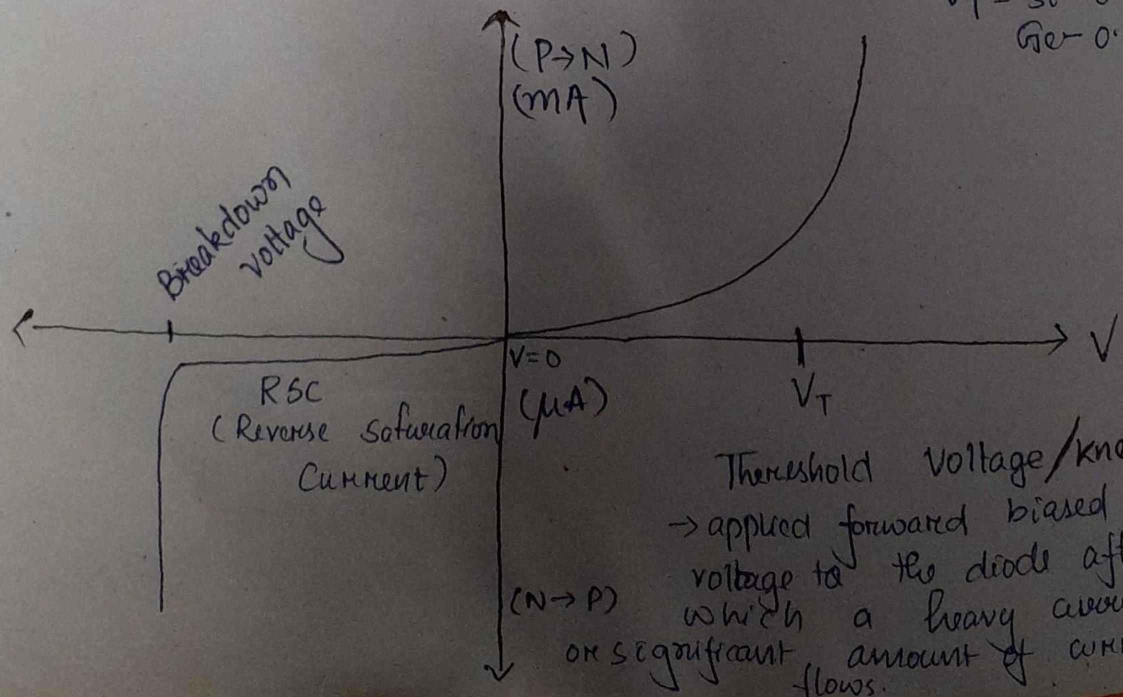
or

$$\boxed{I_D = I_S\left(e^{\frac{KV_D}{T_K}} - 1\right) \quad K = \frac{11600}{\eta}}$$

V-I characteristics of Diode

For → Germanium diode the reverse saturation current is higher.

V_T - Si - 0.7 V
Ge - 0.3 V



Threshold voltage/knee voltage → applied forward biased voltage to the diode after which a heavy current or significant amount of current flows.

- The mechanism due to which there is a current flow due to minority charge carrier is called Avalanche breakdown.
  → It is due to the collision with the covalent Bonds which results in generation of e^- hole pair

Zener

- It occurs in heavily doped diode
- when the reverse voltage increases the E.F across the diode also Increases (the E.F is created due to the wide depletion region near the junction)
- This high E.F exerts a large force on a Bonded electron to tear it out from its covalent bond. Thus a direct rupture of covalent bond produces a large no. of e^- hole pairs, thereby increases the reverse current.
- Zener breakdown occurs at lower reverse voltage than Avalanche breakdown
- Zener breakdown ↑ses with rise in temp.
- Diode Resistances: we can compute 3 types of resistances → DC resistance
  → AC resistance.
  → average resistance

→ DC :- it is the constant voltage by a particular current at that voltage

→ average :- if the voltage varies within a particular range

→ Ac resistance the inst resistance value or Ac resistance value by diff the current eqn w.r.t V_T and

$r_{ac} = \frac{26\eta}{I}$
(dynamic resistance)

• The RSC at 300K for Ge diode is 5μA. Find the voltage to be applied accross the junction to obtain a forward current of 50 mA

$$I_D = I_S \left(e^{\frac{V}{\eta V_T}} - 1 \right)$$

$T = 300$
$I_S = 5\mu A$

$$V_T = \frac{300 \times 1.38 \times 10^{-23}}{1.6 \times 10^{-19}}$$

$= 0.025\ V$

$= 25\ mV$

$= 26\ mV$

$$50 \times 10^{-3} = 5 \times 10^{-6} \left(e^{\frac{V}{10^{-3} \times 26}} - 1 \right)$$

$$10^4 = e^{V/10^{-3} \times 26} - 1$$

$$26 \times 10^{-3} \times \ln(10^4 + 1) = V$$

$0.239\ V$

$= 0.24\ V$

Current flowing through a P-N junction diode (Si diode) is 60 mA for a forward voltage of 0.9 V determine static and dynamic resistance offered by the diode.

$$\text{Static} = \frac{0.9}{60\times10^{-3}} = \frac{900}{60} = 15$$

$$\text{dynamic} = \frac{26\times1}{60\times10^{-3}} = \frac{26000}{60} = 433.34\ \Omega$$

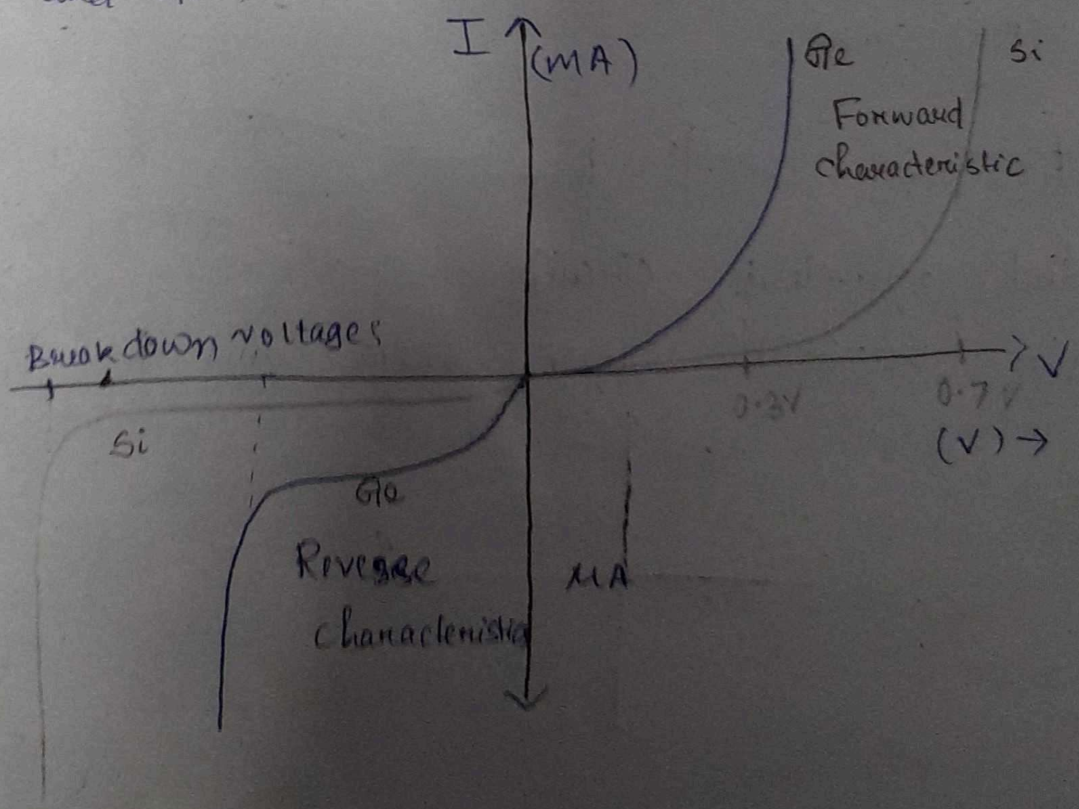
Diode equivalent circuit

An eq circuit is combination of elements properly choosen to best represent the actual characteristics of a component or system in a particular operating loop

For diode we have 3 diff eq circuit

→ Piece wise linear eq circuit
→ Simplified eq circuit
→ ideal eq circuit

Draw and compare V-I characteristics for Si and Ge DIODE.

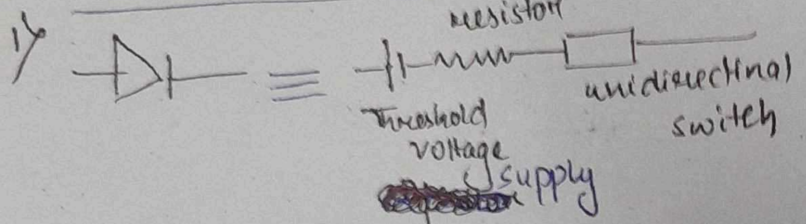


1) The threshold voltage for Germanium is 0.3V.
The threshold voltage for Silicon is 0.7V.

2) Reverse Saturation current is few nanoamperes for Si and few microamperes for Ge diode

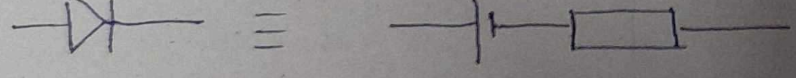
3) The Breakdow voltage in reverse characteristic is more for Si the Ge diode.

To replace a diode

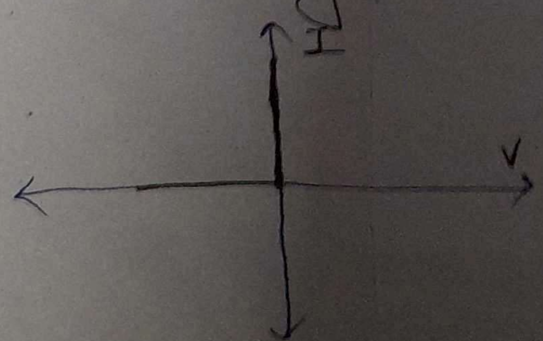
1) 

piece wise linear equivalent circuit

11) simplified equivalent circuit
The resistance is igonored as its value is very small.



111) Ideal equivalent circuit
the threshold voltage is zero and Rsc is also zero.

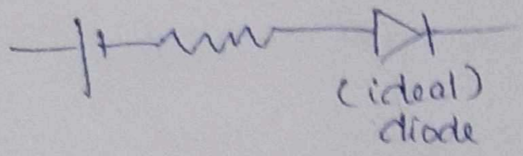


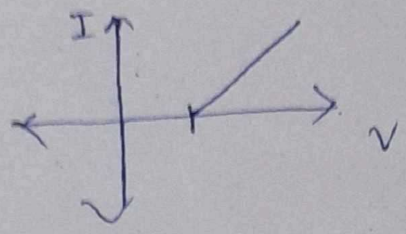
Diode application:-

- It is used as a switch (allows the current in one direction) - ideal diode

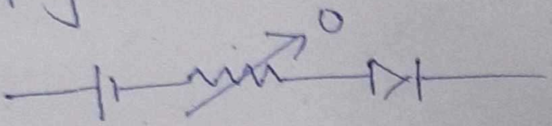
VI characteristics of

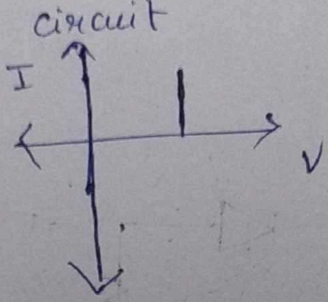
i) Piece wise linear equivalent circuit





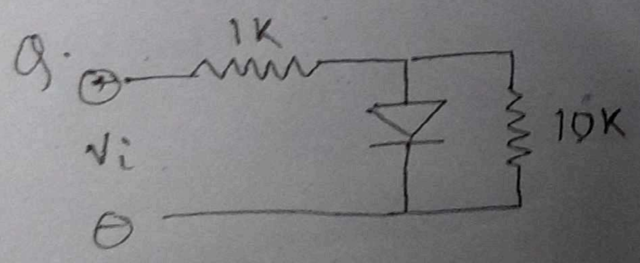
ii) simplified linear equivalent circuit





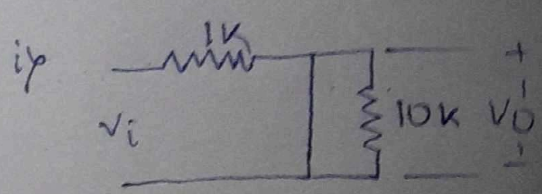
1) Check diode Biasing
2) If diode is reverse Biased then replace it with an open circuit
3) If diode is forward biased check its type
→ if its ideal → short circuit equivalent
→ if its practical diode → threshold voltage

Q.



$V_i = 5V$

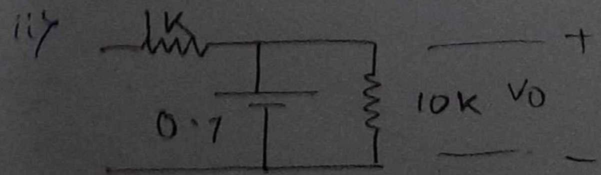
i)



ideal diode

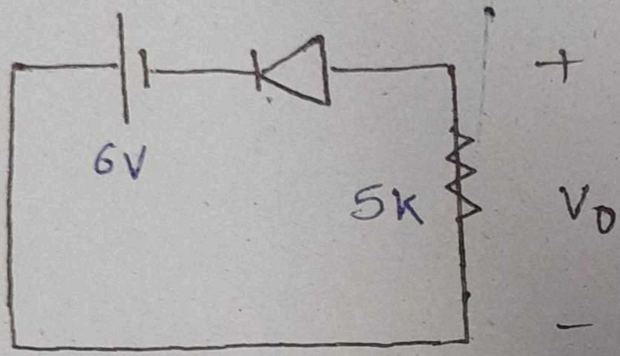
$V_0 = 0$

ii)

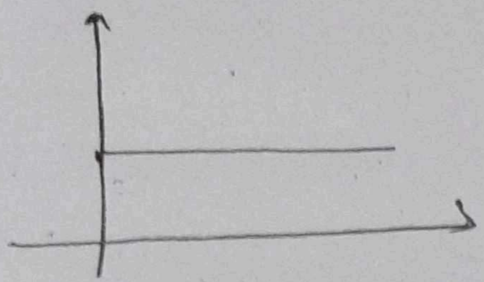


$V_0 = 0.7V$

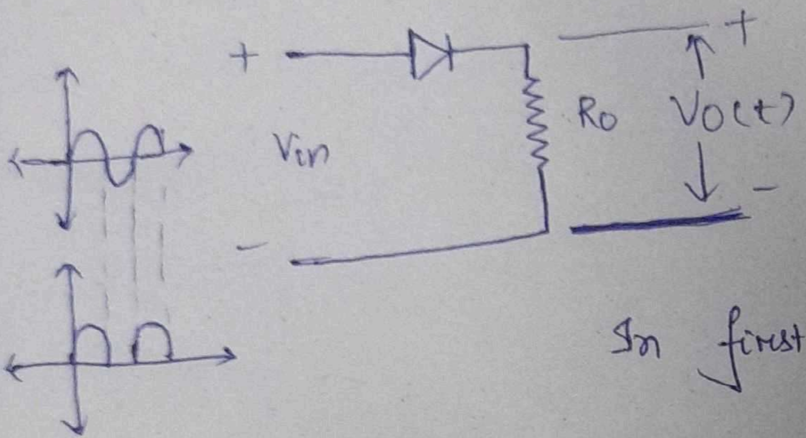
ii)



Pure DC Voltage → Along with direction magnitude also constant



HALF WAVE RECTIFIER

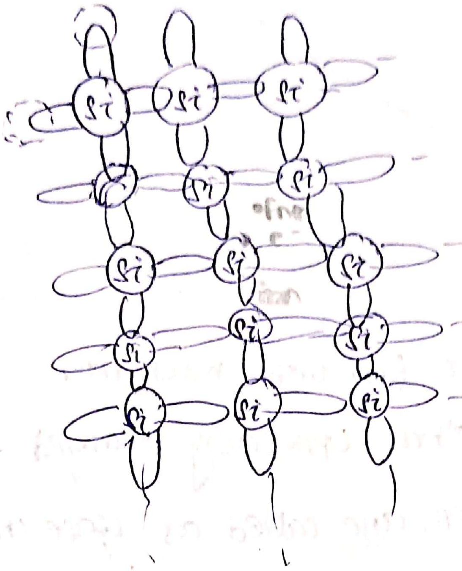


In first half cycle

Q Find the half wave rectifier output if the diode is a Si diode.

electronic components :

- Diode
- Transistor
- BJT
- field Resistance Transistor



Atom

Si → 2, 8, 4

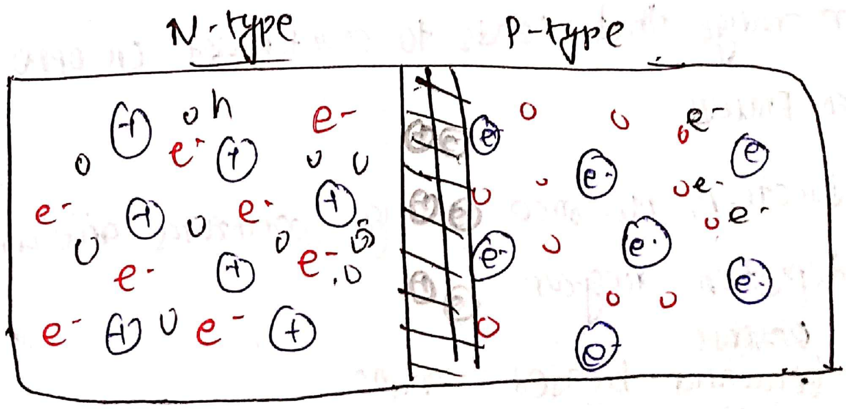
4e⁻ outermost orbital

1 pentavalent dopant generate one free e⁻

1 free e⁻ → 1 + ion

- At room temp. it may happen that covalent bond will absorb energy and the bond break;
- The e⁻ may absorb from cont valency band to conduction band. and absence of e⁻ is created (is called hole)

when 1 covalent bond breaks → 1 hole

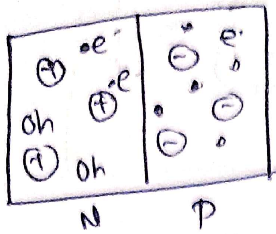


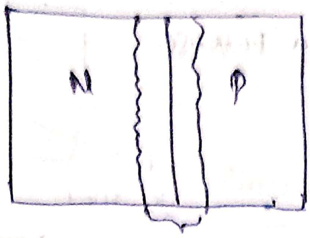
- whenever a covalent pair break, a pair of hole & electron are created. an electron & hole will recombine is known as electron-hole recombination and both will disappear

Electronic component:

Diode

Bipolar junction transistor

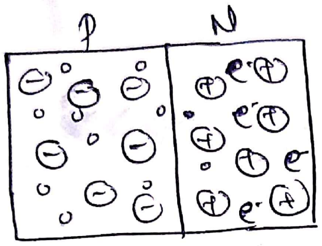




Oh + e⁻ → e⁻ - hole recombination

depletion region - region sandwitched between N & P (Removed region)

Diode under no-bias condition:

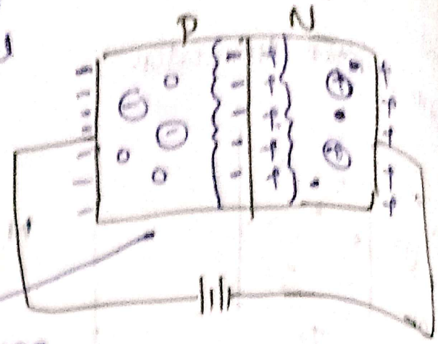


P junction:-
majority - hole
minority - e⁻

N - junction
majority - e⁻
minority - hole

- e⁻ and hole both recombine
- electric field is created inside the diode
- Near the junction, the e⁻ from n-type, recombine with the p-hole, leaving imobile ions
- This oppositely charged ions in both the side of the junction are call space-charge region.
- The electric field created by the space-charge region opposes the diffusion process (recombination process) of e⁻s and holes
- There are 2 concurrent phenomenon, that tends to generate more space charge & the electric field (generated by space charge) that to counteract (or) oppose the recombination process
- Near the junction, no free charge carriers available, which is as depletion region

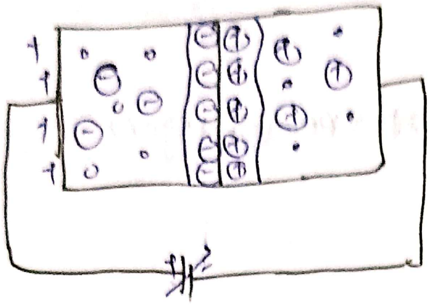
Diodes under Reverse Bias condition:



- Holes are more attracted by ⊖ charge generated by battery
- when P is connected to negative terminal then it is said to be reverse biased.
- That low current is called reverse biased

Diodes under forward biased cond^n

No free charge carriers are there



here depletion region is space charge layer.

Diode current eq^n:

$$I_D = I_S\,(e^{\frac{V}{\eta V_T}} - 1)$$

I_d = current to diode

V = voltage across diode

η is a constant value = 1 (for Germanium)

for $\eta = 2$ (silicon) → $V_{applied}$ is very low

higher diode current ↘ $\eta = 1$ (") → $V_{applied} > V_{Threshold}$

V_T = is volt-equivalent of temprature

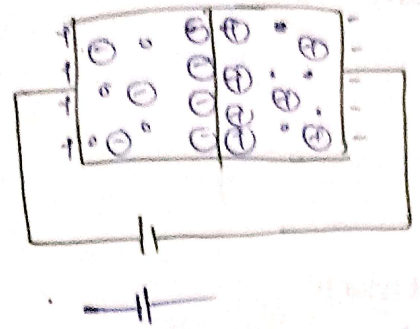
$V_T = T \cdot K / q$ → charge of e⊖ = 1.6×10^{-19} C

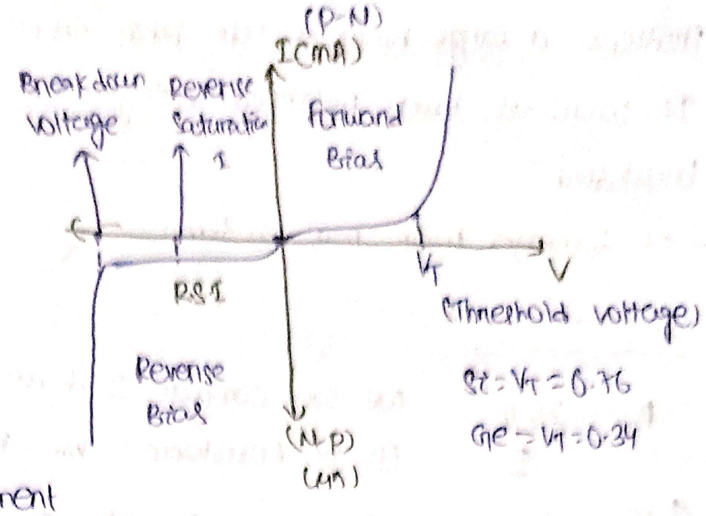
Temprature Boltzman's constant = 1.38×10^{-23} J/atom Columb

$$I_D = I_S\,(e^{\frac{KV_D}{TK}} - 1)$$

$$K = \frac{11600}{\eta}$$

V-I characteristic of Diode:-





RSI → Reverse saturation current (N→P→current flow)
↓
const

Threshold voltage is the applied to forward biased voltage to the diode after which the significant amt of current flows in the diode.

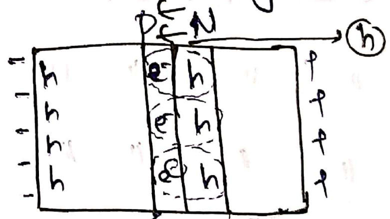
* Covalent Bond breaking → e⁻ hole pair generate → due to collide

Reverse Biased → V↑, K.E↑, lots of covalent bond break, e⁻-hole pair generate↑
↓ minority carrier↑ ; majority

(That mechanism is called avalanche breakdown)

* Diode Breakdown:-

Minority charge carrier concentration subsequently↑ that is called Diode breakdown



[Reverse biased current → flow due to carrier (minority) depletion region↑]

[reversed voltage↑]

Zener Breakdown:-

It occurs in heavily doped diode. When reverse ~~bia~~ voltage increases, the electric field across diode also↑

(The electric field is created due to the wide depletion region near th junction. This high $\vec{E}$ field exerts a large force on a bonded e⁻ to tea out from it's covalent Bond. thus the direct structure of covalent Bor produces a large no. of e⁻ hole pair, there by ↑ reverse current. It occurs at lower reversed voltage as compared to avalanche breakdown.

→ It decreases with rise in temp.

Diode Resistance:-

$R_{ac} = \frac{26\,\Omega}{I}$

↑ Rdynamic
Rinstaneous

We can compute 3 diode Resistance

① DC Resistance = V/I = fixed

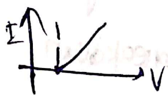
② Average resistance = $\frac{V_{max} - V_{min}}{I_{max} - I_{min}}$

If applied voltage carries with range ($V_{min} \to V_{max}$) corresponding current varies " " ($I_{min} \to I_{max}$)

→ The Instantaneous resistance value = differentiating current eqn wrt I and applied voltage V_d

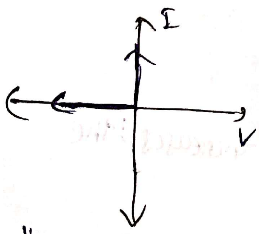
→ A equivalent circuit combination of element properly chosen to best represent the actual characteristics of a component or system in a particular operating region. For diode we have 3 equivalent circuit.

① piece wise linear equivalent circuit —|├—∿∿∿—▷|— (Ideal diode)

② simplify " " " " —|├—▷|— 

③ Ideal " " " " —▷|—

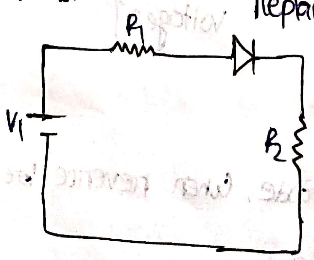
V-I characteristics of Ideal diode:



V_{th} (ideal) = 0

slope = 0.

$\frac{V}{I} = R = 0$



replaced by —|├— (0.7V)

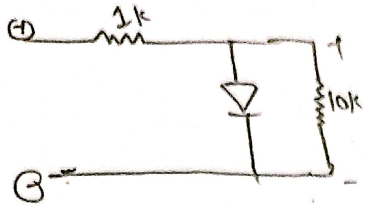
$I = \frac{V_1 - 0.7}{R_1 + R_2}$

Steps: Check diode biasing

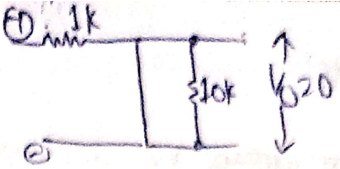
If reverse biased → replace with open circuit

If forward biased → check it's types

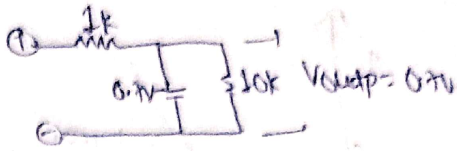
Ideal → short circuit Practical → with threshold

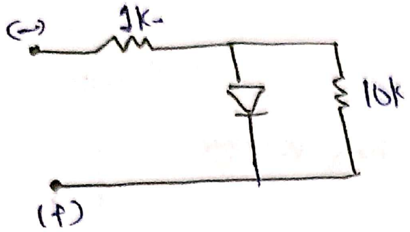


(i) when ideal diode short-circuited
Voutput = 0



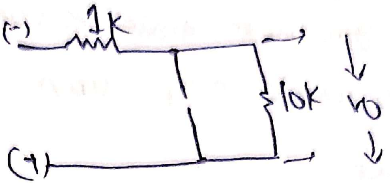
(ii) Silicon diode = 0.7V
Voutput = 0.7V





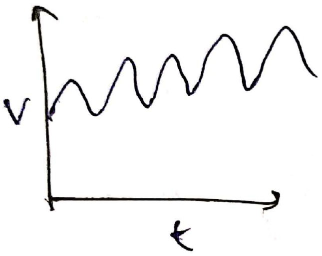
(iii) Germanium diode = 0.4V
Voutput = 0.34V

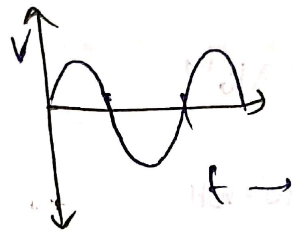
Uses
Zener diode → voltage regulator
LED → Display
Diode → Rectifier
Clipper...

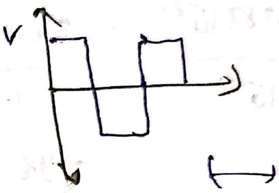


$V_0 = \frac{10}{11} \times 5$
$= \frac{50}{11} = 4.5$

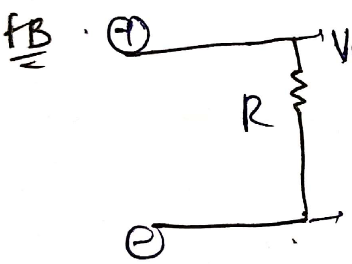
Rectifier:- (DC)





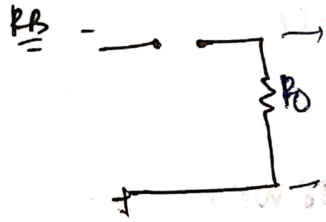


FB



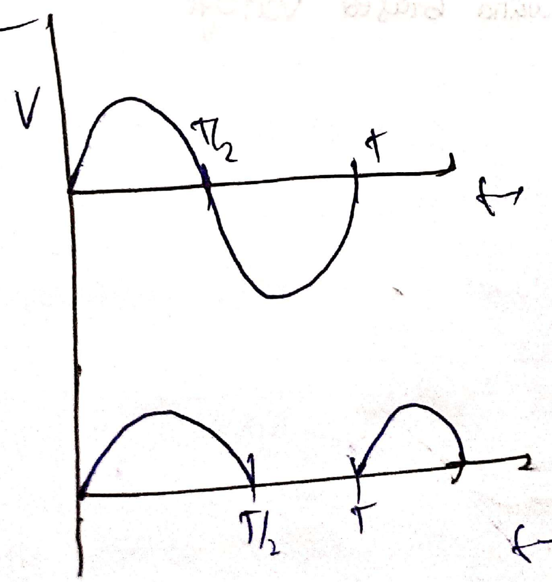
Voutput is obtained

RB



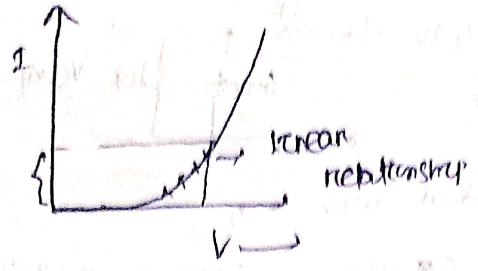
Voutput

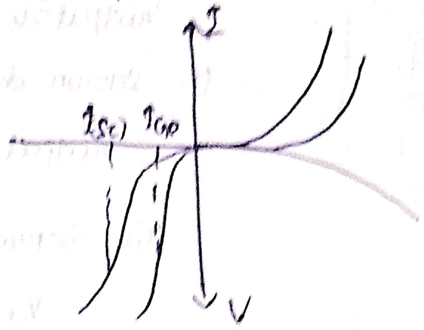
Half wave:-



Assignments:

Draw and compare V-I characteristics of Si & Ge





The reverse S.C at 300K for germanium diode is 5μA. find voltage to be supplied across junction to obtain a I for 50mA

$I_D = I_S\left(e^{\frac{qV}{\eta V_T}} - 1\right)$ T=300K

Ge, n=1 $I_S = 5\times10^{-6}A$ $I_D = 50\times10^{-3}A$

K=11600

$$V_T = \frac{300\times1.38\times10^{-23}}{1.6\times10^{-19}} = \frac{300\times1.38}{1.6}\times10^{-4}$$

$= 25.8\times10^{-3}$ Volt

$= 26$ milli Volt

$$50\times10^{-3} = 5\times10^{-6}\left(e^{\frac{V}{1\times26}} - 1\right)$$

$$10^4 = \left(e^{\frac{V}{26}} - 1\right)$$

$$10^4 + 1 = e^{\frac{V}{26}} \quad (V = 0.238 \text{ Volt})$$

I through P-N junction diode is 60mA. forward biased voltage of 0.9V static & dynamic R altered by diode

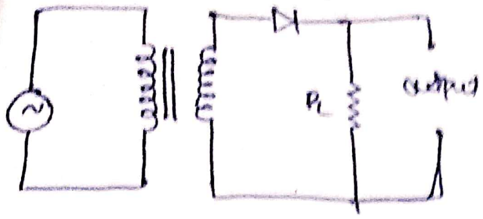
$$R_{static} = \frac{V}{I} = \frac{0.9V}{60\times10^{-3}A} = 15\Omega$$

$$R_{dyna} = \frac{26\times\eta}{I} = \frac{26\times1}{60\times10^{-3}}$$

$= \frac{26}{60}\times10^3$

$= 0.866\times10^3\Omega$

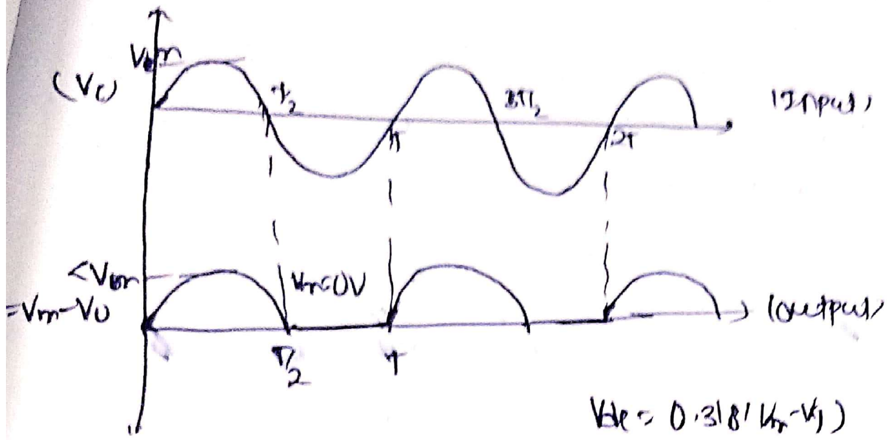
Half wave rectifier for silicon diode

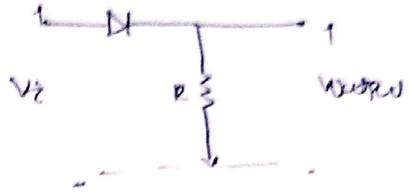


For silicon diode

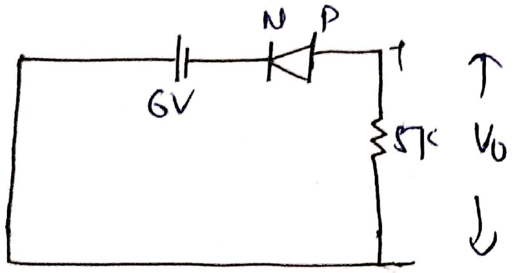
threshold voltage = 0.7V

Diode will conduct from 0.7V

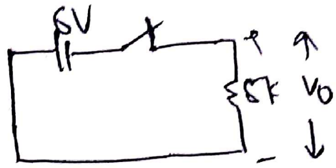




$V_{dc} = 0.318(V_m - V_f)$



(i) when diode is ideal

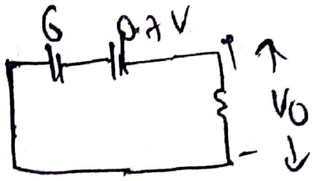


Voutput = 6V

(ii) when diode is reverse biased

Voutput = 0V

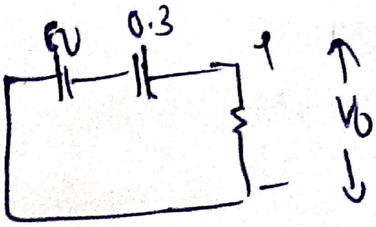
(iii) when diode is silicon



Voutput = 6 + 0.7 =

= ~~6.3V~~

(iv) when diode is germanium



Voutput = 6 + 0.3

= 6.3

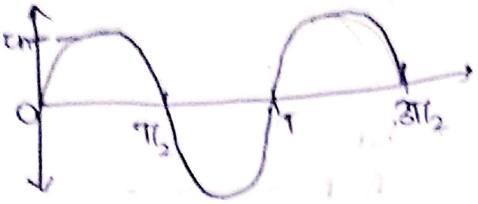
Has the current flows and describe half

① Definition

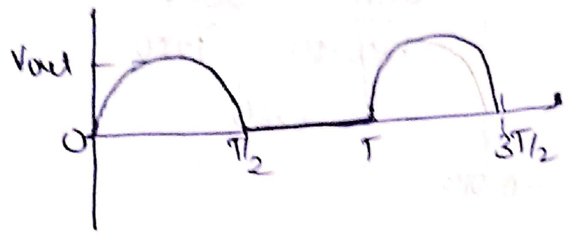
- It converts Ac voltage into dc voltage
- It is a type of rectifier that allows only 1-half cycle of an Ac voltage waveform to pass while blocking other half cycle

② Waveform:

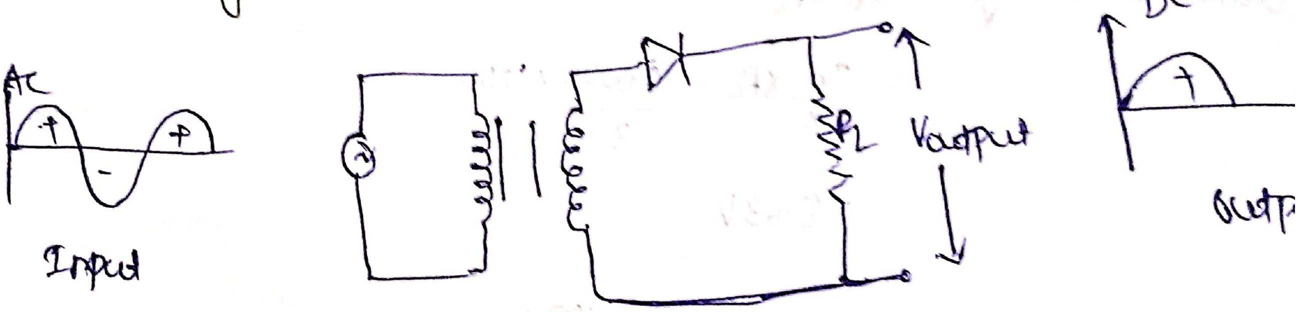
Input :-



Output :-



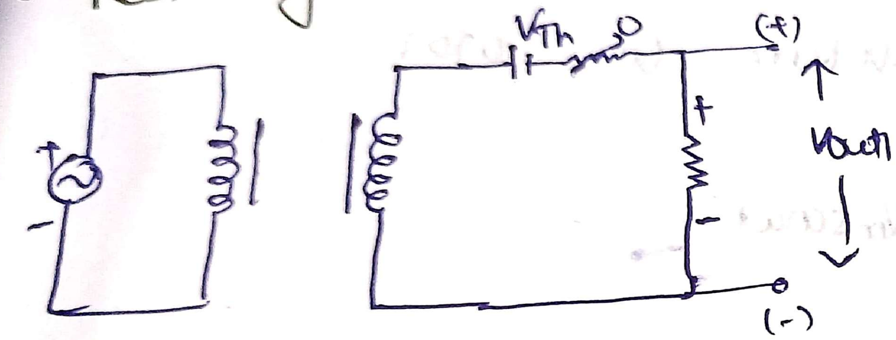
Circuit diagram:

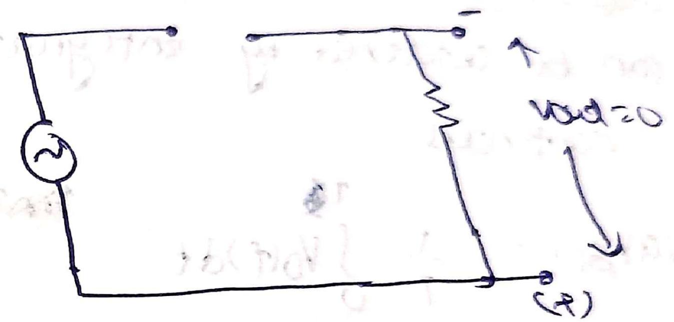


③ Analysis of circuit :

1. A high AC voltage is applied to the primary side of above transformer, the obtained voltage is applied to the diode
2. The diode is forward biased during positive half cycle of and hence desired output is obtained having dc voltage
3. Then diode is reverse biased during negative half cycle and acts like open circuit and no power is obtained

(4) Redrawing of circuit





Forward biased

and hence output is obtained

Reverse biased

hence no output is obtained

i) Average value:-

It can be obtained by integrating waveform from 0 to T

[illegible] continuous

$V = V_m \sin\omega t$

$$V_o(av) = \frac{1}{T}\int_0^T V_o(t)\,dt$$

$$= \frac{1}{T}\int_0^{T/2} V_o(t)\,dt + \cancel{\int_{T/2}^{T} V_o(t)\,dt}^{\,0}$$

$$= \frac{1}{T}\int_0^{T/2} V_m \sin\omega t$$

$$= \frac{1}{T}\left.\frac{-V_m\cos\omega t}{\omega}\right|_0^{T/2}$$

$$= \frac{1}{T}\,\frac{-V_m\,(\cos\omega t - \cos 0)}{\frac{2\pi}{T}}$$

$$= \frac{-V_m}{2\pi}\left(\cos\frac{2\pi}{T}\times\frac{T}{2} - \cos 0\right)$$

$$= \frac{-V_m}{2\pi}(-2) = \frac{V_m}{\pi}$$

ii) Rms value:-

$$V_o(t)_{rms}/I_{dc} = \left[\frac{1}{T_0}\int_0^{T_0} V_o(t)^2\,dt\right]^{1/2}$$

$$= \left[\frac{1}{T_0}\int_0^{T_0} V_m^2\sin^2\omega t\right]^{1/2}$$

$$= \left[\frac{1}{T_0}\int_0^{T_0} V_m^2\left[\frac{1-\cos\omega t}{2}\right]\right]^{1/2}$$

$$= \left(\frac{1}{T_0}\,\frac{V_m^2\,\frac{T_0}{2} - \cancel{\left[\frac{\sin\omega t}{2\omega}\right]_0^{T_0}}^{\,0}}{2}\right)^{1/2}$$

$$= \left[\frac{V_m^2}{4}\right]^{1/2}$$

$$= \frac{V_m}{2}$$

(ii) Ripple factor:

It is defined as rms value of an ac component of signal to average value of signal

$$r = \sqrt{\frac{\text{rms value of ac component}}{\text{average value of signal}}}$$

$$= \sqrt{\frac{V_{rms}^2 - V_{dc}^2}{V_{dc}^2}}$$

$$= \sqrt{\frac{\left(\frac{V_m}{2}\right)^2 - \left(\frac{V_m}{\pi}\right)^2}{\left(V_m/\pi\right)^2}}$$

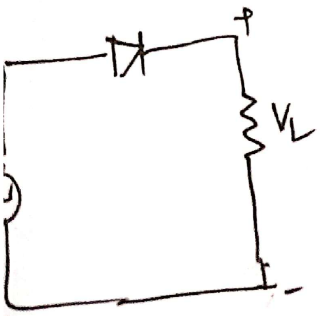
$$= \sqrt{\frac{V_m^2\left(\frac{1}{4} - \frac{1}{\pi^2}\right)}{V_m^2 \times \frac{1}{\pi^2}}} = \sqrt{\frac{\frac{\pi^2-4}{4\pi^2}}{\frac{1}{\pi^2}}}$$

$$= 1.11$$

Efficiency

It is ratio of dc output power delivered to load system to the input power

$$\eta = \frac{\text{Output power delivered}}{\text{Total input power}}$$



$$= \frac{P_{dc} \text{ to } R_L}{P_{dc} \text{ to } R_L + r}$$

$$= \frac{I_{dc}^2 R_L}{I_{dc}^2 (R_L + \cancel{r})} \quad r \to 0$$

$$= \frac{I_{dc}^2}{I_{ac}^2}$$

$$= 40\%$$

A diode (r_f = 50Ω) to a load resistance of $R_L = 1200$ from a 20V rms voltage source. calculate

(i) dc load current (I_m)

$$I_m = \frac{V_m}{R_L + r_f} = \frac{20\sqrt{2}}{1200+50}$$

$$= \frac{20 \times 1.41}{1250}$$

$$= 0.0226$$

(ii) Rms load current (I_{rms})

$$I_{rms} = \frac{I_0}{2} = \frac{0.0226}{2}$$

$$= 0.0113$$

(iii) calculate output dc voltage

$$V_{dc} = I_{dc} \times R_L = \frac{I_m}{\pi} \times R_L = \frac{0.0226}{3.14} \times 1200$$

$$= 8.63V$$

(iv) calculate output power

$$P_{output} = \frac{V_{dc}^2}{R_L} = \frac{(8.63)^2}{1200} = \frac{74.47}{1200}$$

$$= 0.062$$

(v) calculate efficiency

$$\eta = \frac{\text{Output Power}}{\text{Input power}} = \frac{I_{dc}^2 R_L}{I_{ac}^2 (R_L + r_f)} \times 100$$

$$= \frac{I_{dc}^2}{I_{ac}^2} \times 100 \times \frac{R_L}{R_L + r_f}$$

$$= 40\% \times \frac{1200}{1250}$$

$$= 38.4\%$$

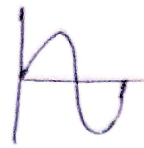
HC

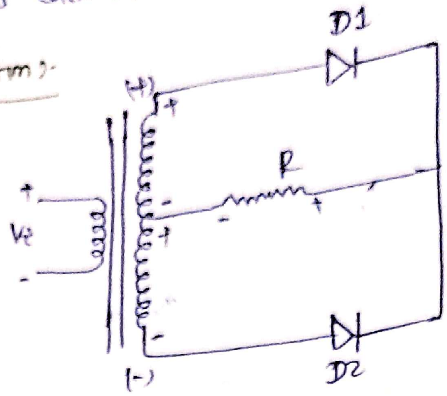
Centre-taped Rectification:-

① Definition :- It requires a centre-taped transformer to establish the input signal across each of the section of secondary transformer

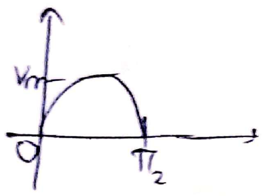
Input/output waveform :-

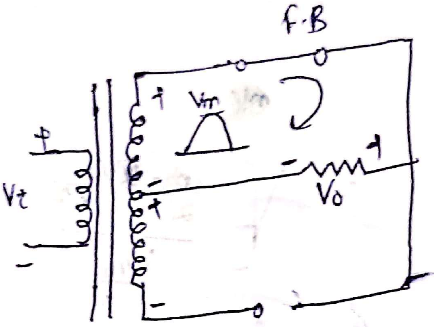
Input

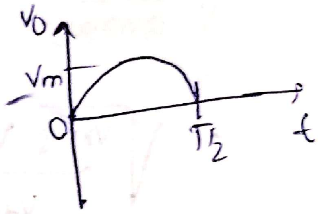
② 



Output



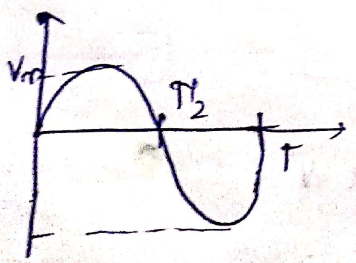


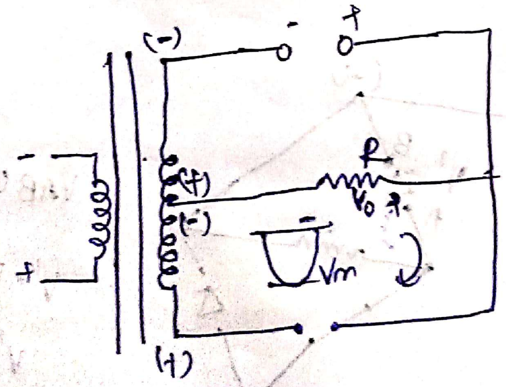


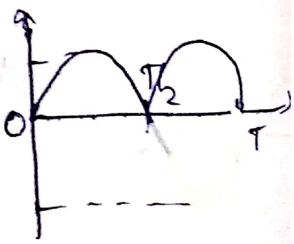
Applying KVL $V_m - V_o = 0$

$$\boxed{V_m = V_o}$$

for $T/2$ to T







Applying KVL to loop

$V_o - V_m = 0$

$$\boxed{V_o = V_m}$$

CIRCUIT ANALYSIS :-

- when +ve V_i is applied to the primary transformer, D1 is assumed to be short-circuit (equivalent) and D2 open-circuit (equivalent). So upper half of the circuit is forward biased, hence some output voltage is obtained across it, while lower-half is reverse-biased, hence no power obtained
- when negative V_i is applied to primary transformer. D2 is assumed to be forward biased and D1 is reverse biased. hence some output is obtained across D2 while no output across D1
- This process repeat itself, and whole waveform is fully rectified

Vo(dc)

$$V_{o(dc)} = \frac{1}{\frac{T_0}{2}} \int_0^{T_0/2} V_o(t)\,dt$$

$$\Rightarrow \frac{2}{T_0}\int_0^{T_0/2} V_m \sin\omega t\,dt = \frac{2}{T_0} -V_m\left[\frac{\cos\omega t}{\omega}\right]_0^{T_0/2}$$

$$= \frac{2}{T_0} \frac{-V_m}{\omega}\left(\cos\frac{2\pi}{T}\times\frac{T}{2} - \cos 0\right)$$

$$= \frac{\cancel{2}}{\cancel{T_0}} \frac{-V_m}{\frac{2\pi}{T_0}} (-2)$$

$$= \frac{2V_m}{\pi}$$

Vo (rms)

$$V_{rms(dc)} = \left[\frac{1}{\frac{T_0}{2}} \int_0^{T_0/2} V_o(t)^2\,dt\right]^{1/2}$$

$$V_{rms}^2 = \frac{2}{T_0}\int_0^{T_0/2} V_m^2 \sin^2\omega t\,dt$$

$$= \frac{2}{T_0} V_m^2 \int_0^{T_0/2} \left[\frac{1-\cos 2\omega t}{2}\right]_0^{T_0/2}$$

$$= \frac{\cancel{2}}{T_0} \times \frac{V_m^2}{\cancel{2}} \int_0^{T_0/2} T - \int_0^{T_0/2} \cos 2\omega t\,dt$$

$$= \frac{V_m^2}{T_0}\left[\frac{T_0}{2} - \cancel{\frac{\sin 2\omega t}{2\omega}}\Big|_0^{T_0/2}\right]$$

$$= \frac{V_m^2}{\cancel{T_0}} \times \frac{\cancel{T_0}}{2} = \frac{V_m^2}{2}$$

$$V_{rms}^2 = \frac{V_m^2}{2}$$

$$V_{rms} = \frac{V_m}{\sqrt{2}}$$

Ripple factor

$$r = \sqrt{\frac{\text{rms component of ac}}{\text{average value}}}$$

$$= \sqrt{\frac{V_{rms}^2 - V_{dc}^2}{V_{dc}^2}} = \sqrt{\frac{\frac{V_m^2}{2} - \frac{4V_m^2}{\pi^2}}{\frac{4V_m^2}{\pi^2}}} = \sqrt{\frac{\frac{1}{2} - \frac{4}{\pi^2}}{\frac{4}{\pi^2}}}$$

$$= \sqrt{\frac{\pi^2 - 8}{8}}$$

$$= 0.48$$

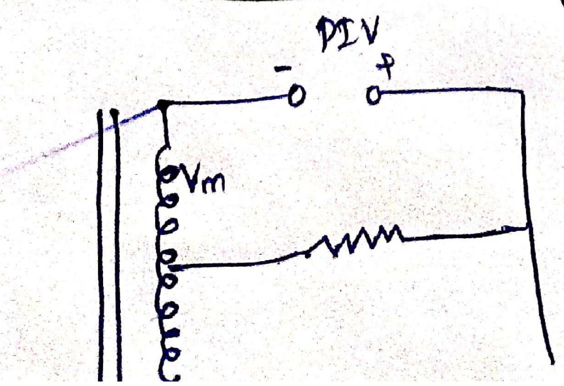
Efficiency

$$\eta = \frac{\text{output power delivered}}{\text{total input power}}$$

$$= \frac{\left(\frac{2I_m}{\pi}\right)^2}{\left(\frac{I_m}{\sqrt{2}}\right)^2} \times 100 = \frac{\frac{4}{\pi^2}}{\frac{1}{2}} \times 100 = \frac{8}{\pi^2} \times 100$$

$$= 80\%$$

Peak Inverse Voltage



$PIV = V_{secondary} + V_R$

$= V_m + V_m = 2V_m$

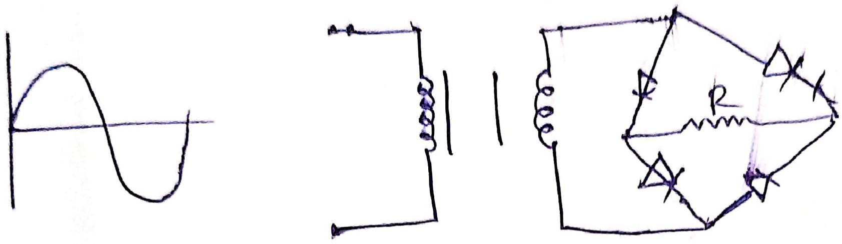
So PIV should be $\geq 2V_m$

Full wave rectifier:-

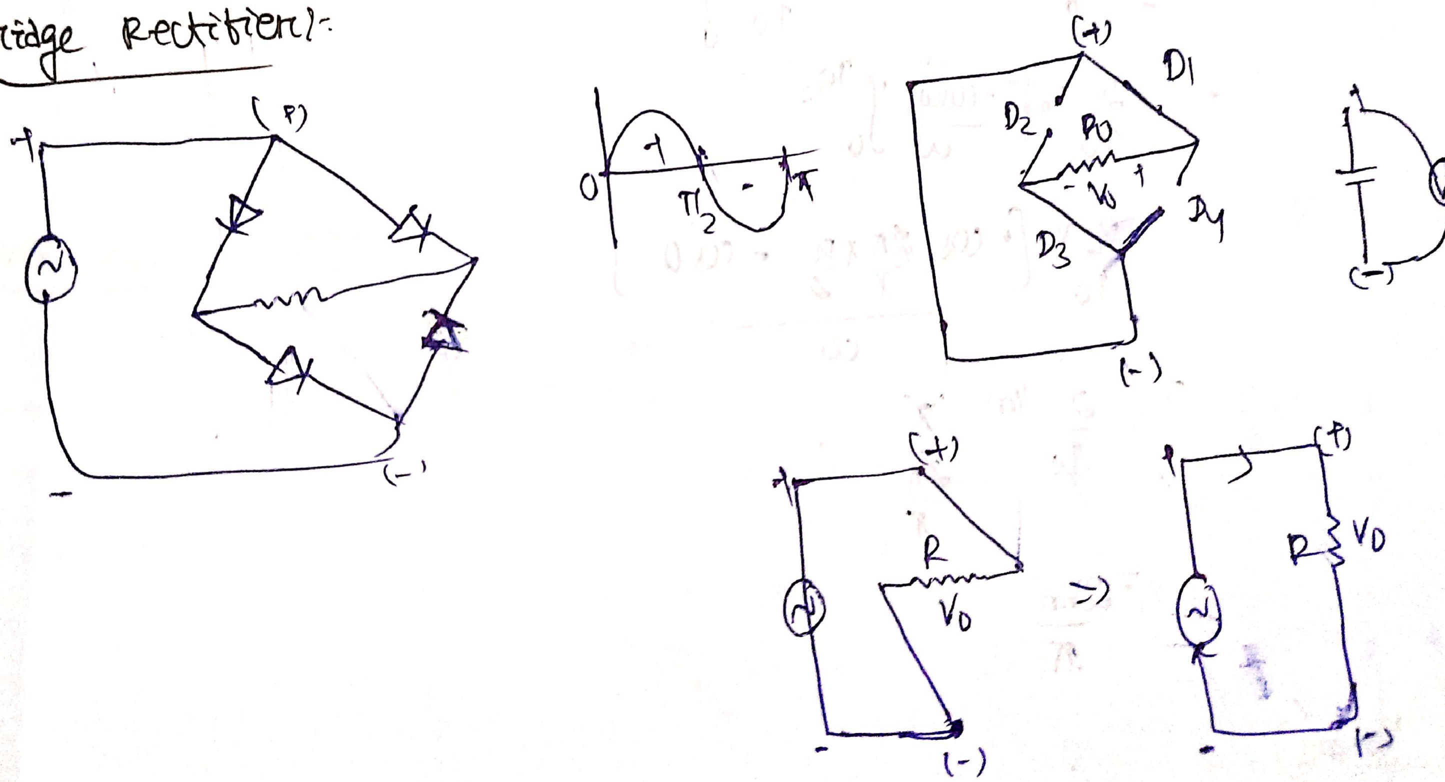
(1) centre-tap rectifier

(2) Bridge rectifier

Bridge

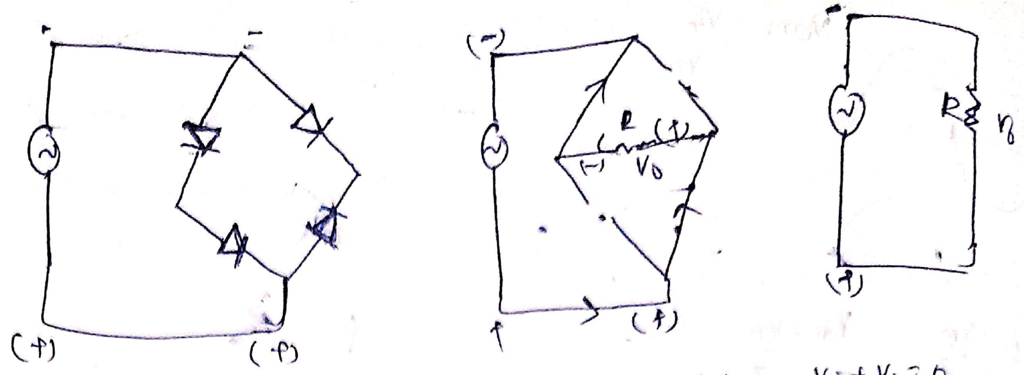


Bridge Rectifier:-



HO

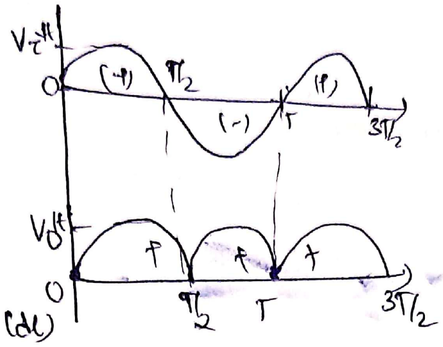
① De



② (

Applying KVL to ckt, $-V_i + V_0 = 0$

$V_0 = V_i$



$V = V_m \sin(2\pi f_0)t$

(i) $V_0(dc)$ (ii) $V_0(rms)$ (iii) $\eta = 80\%$

(i) $V_0(dc)$

$$V_0(dc) = \frac{1}{T_0/2}\int_0^{T_0/2} V_0(t)\,dt = \frac{2}{T_0}\int_0^{T_0/2} V_m \sin\omega t\,dt$$

$$= \frac{2}{T_0} V_m \left[\frac{-\cos\omega t}{\omega}\right]_0^{T_0/2}$$

$$= \frac{2}{T_0} V_m \left[\frac{-\cos \frac{\cancel{2}\pi}{\cancel{T}} \times \frac{T_0}{\cancel{2}} - \cos 0}{\omega}\right]$$

③

$$= \frac{2}{T_0} V_m \frac{2}{\frac{2\pi}{T}}$$

$$= \frac{2V_m}{\pi}$$

(ii) $V_0(rms)$

$$V_{rms}(dc) = \left[\frac{1}{\frac{T_0}{2}} \int_0^{T_0/2} V_0(t)^2\,dt\right]^{1/2}$$

$$V_{rms}^2 = \left(\frac{2}{T_0}\left[V_m^2 \sin^2\omega t\right]_0^{T_0/2}\right]$$

$$= \frac{2}{T_0} V_m^2 \left[\frac{1-\cos 2\omega t}{2}\right]_0^{T_0/2}$$

Scanned with OKEN Scanner

$$= \frac{2V_m^2}{T_0}\left(\left[\frac{T_0}{4}\right] - \left[\frac{\cancel{\sin 2\omega t}}{2\omega}\right]_0^{T_0/2}\right)$$

$$= \frac{2V_m^2}{T_0}\left[\frac{T_0}{4}\right]$$

$$V_{rms}^2 = \frac{V_m^2}{2}$$

$$\boxed{V_{rms} = \frac{V_m}{\sqrt{2}}}$$

Ripple factor :-

$$\gamma = \sqrt{\frac{rms}{average}}$$

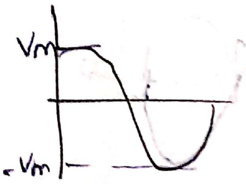
$$= \sqrt{\frac{V_{rms}^2 - V_{dc}^2}{V_{dc}^2}} = \sqrt{\frac{\frac{V_m^2}{2} - \frac{4V_m^2}{\pi^2}}{\frac{4V_m^2}{\pi^2}}}$$

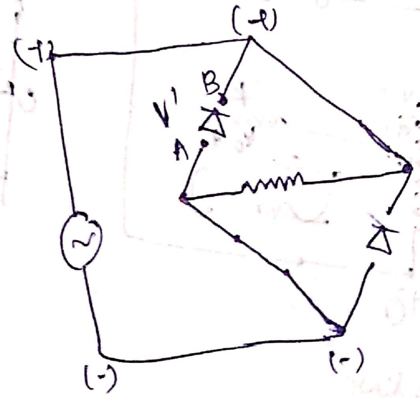
$$= \sqrt{\frac{\frac{1}{2} - \frac{4}{\pi^2}}{\frac{4}{\pi^2}}} = \sqrt{\frac{\frac{\pi^2 - 8}{2\pi^2}}{\frac{4}{\pi^2}}}$$

$$= \sqrt{\frac{\pi^2 - 8}{8}}$$

$$= 0.48$$

peak inverse voltage





V_{AB} or V'

$V' - V_0 = 0$

$V' = V_0$

$V' = V_i = V_m$

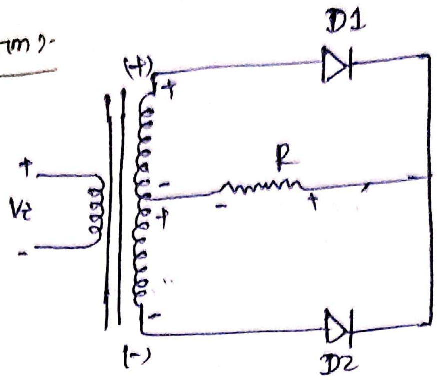
so, peak inverse voltage PIV rating is greater than or equal to V_m

Centre-taped Rectifier:-

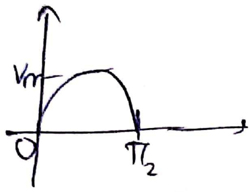
Defination :- It requires a centre-taped transformer to establish the input signal across each of the section of secondary transformer

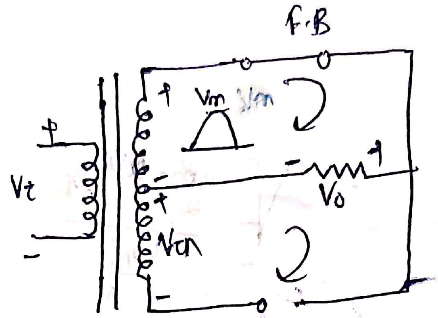
Input/output waveform:-

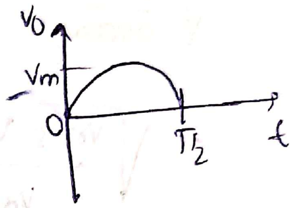
Input



Output







Applying KVL $V_m - V_o = 0$

$$\boxed{V_m = V_o}$$

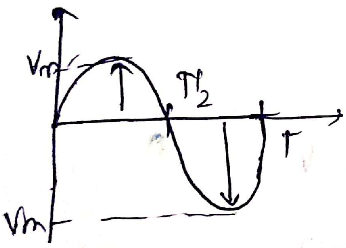
Applying KVL to 2nd loop

$+V_m + V_m = V_o$

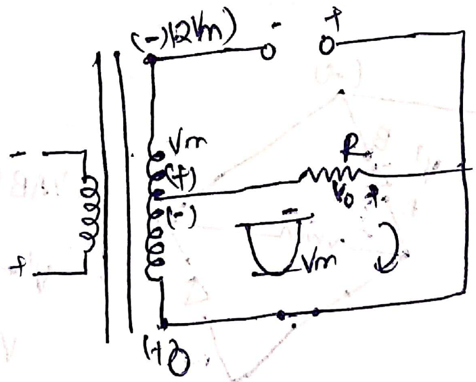
$2V_m = V_o$

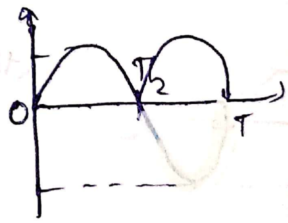
for T/2 to T

Turn ratio = 1:2



2Vm





Applying KVL to loop

$V_o - V_m = 0$

$$\boxed{V_o = V_m}$$

Disadvantages :- exactly at centre, taping should be done (centre)

since PIV ≥ 2Vm. We need costlier diode

CIRCUIT ANALYSIS :-

→ when +ve V_i is applied to the primary transformer. D1 is assumed to be short-circuit (equivalent) and D2 open-circuit (equivalent). So upper half of the circuit is forward biased. hence some output voltage is obtained across it, while lower-half is reverse-biased. hence no power obtained

→ when negative V_i is applied to primary transformer. D2 is assumed to be forward biased and D1 is reverse biased. hence some output is obtained across D2 while no-output across D1

→ This process repeat itself, and whole waveform is fully rectified

Vo(dc)

$$V_{o(dc)} = \frac{1}{\frac{T_0}{2}} \int_0^{T_0/2} V_o(t)\,dt$$

$$\Rightarrow \frac{2}{T_0} \int_0^{T_0/2} V_m \sin\omega t\,dt = \frac{2}{T_0} - V_m\left[\frac{\cos\omega t}{\omega}\right]_0^{T_0/2}$$

$$= \frac{2}{T_0} \frac{-V_m}{\omega} \left(\cos \frac{2\pi}{T} \times \frac{T}{2} - \cos 0\right)$$

$$= \frac{\cancel{2}}{\cancel{T_0}} \frac{-V_m}{\frac{\cancel{2}\pi}{\cancel{T_0}}} (-2)$$

$$= \frac{2V_m}{\pi}$$

Vo (rms)

$$V_{rms(dc)} = \left[\frac{1}{\frac{T_0}{2}} \int_0^{T_0/2} V_o(t)^2\,dt \right]^{1/2}$$

$$V_{rms}^2 = \frac{2}{T_0} \int_0^{T_0/2} V_m^2 \sin^2\omega t\,dt$$

$$= \frac{2}{T_0} V_m^2 \int_0^{T_0/2} \left[\frac{1-\cos 2\omega t}{2} \right]_0^{T_0/2}$$

$$= \frac{\cancel{2}}{T_0} \times \frac{V_m^2}{\cancel{2}} \int_0^{T_0/2} T - \int_0^{T_0/2} \cos 2\omega t\,dt$$

$$= \frac{V_m^2}{T_0} \left[\frac{T_0}{2} - \cancel{\frac{\sin 2\omega t}{2\omega}}^{0} \Big|_0^{T_0/2} \right]$$

$$= \frac{V_m^2}{\cancel{T_0}} \times \frac{\cancel{T_0}}{2} = \frac{V_m^2}{2}$$

$$V_{rms}^2 = \frac{V_m^2}{2}$$

$$V_{rms} = \frac{V_m}{\sqrt{2}}$$

Ripple factor

$$\gamma = \sqrt{\frac{\text{rms component of ac}}{\text{average value}}}$$

$$= \sqrt{\frac{V_{rms}^2 - V_{dc}^2}{V_{dc}^2}} = \sqrt{\frac{\frac{V_m^2}{2} - \frac{4V_m^2}{\pi^2}}{\frac{4V_m^2}{\pi^2}}} = \sqrt{\frac{\frac{1}{2} - \frac{4}{\pi^2}}{\frac{4}{\pi^2}}}$$

$$= \sqrt{\frac{\pi^2 - 8}{8}}$$

$$= 0.48$$

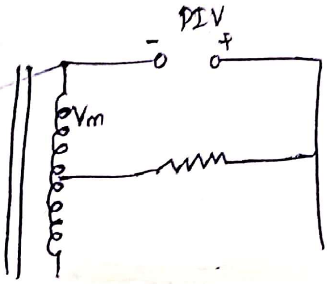
Efficiency

$$\eta = \frac{\text{output power delivered}}{\text{total input power}}$$

$$= \frac{\left(\frac{2I_m}{\pi}\right)^2}{\left(\frac{I_m}{\sqrt{2}}\right)^2} \times 100 = \frac{\frac{4}{\pi^2}}{\frac{1}{2}} \times 100 = \frac{8}{\pi^2} \times 100$$

$$= 80\%$$

Peak Inverse voltage



$PIV = V_{secondary} + V_R$

$= V_m + V_m = 2V_m$

So PIV should be $\geq 2V_m$

Comparison

Comparison	bridge	centre-tap
V_0 (dc)	$\frac{2V_m}{\pi}$	$\frac{2V_m}{\pi}$
V_{rms}	$\frac{V_m}{\sqrt{2}}$	$\frac{V_m}{\sqrt{2}}$
ripple factor	0.48	0.48
η	80%	80%
PIV	$\geq V_m$	$\geq 2V_m$

Hao

① Def

② wr

③

Digital electronics :-

Number system :-

Number system	Base/Radix	Distinct symbols	examples
Binary	2	0, 1	10, 111, 1001
Octal	8	0,1, ·· 7	
Decimal	10	0,1, ····· 9	
hexa-decimal		0, 1 - - 9 A · · - F	

Decimal	binary	octal	hexa-decimal
0	0 0 0		
1	0 0 1		
2	0 1 0		
3	0 1 1		
4	0 1 0 0		
5	0 1 0 1		
6	0 1 1 0		
7	0 1 1 1		
8	1 0 0 0		
9	1 0 0 1		
10	1 0 1 0		
11	1 0 1 1		
12	1 1 0 0		
13	1 1 0 1		
14	1 1 1 0		
15	1 1 1 1		

~~binary~~ decimal → binary.

$$\begin{array}{r|l} 2 & 25 \\ 2 & 12 - 1 \\ 2 & 6 - 0 \\ 2 & 3 - 0 \\ & 1 - 1 \end{array}$$

binary = 11001

↳ from bottom to top

For 25.32 = (11001.(

from top to bottom

.32
× 2
0.64
× 2
1.28
× 2
0.56
× 2

1 0 0 0
↑ ↑ ↑ ↑
$2^3\ 2^2\ 2^1\ 2^0$

54.78 = 1001010.1100

$$\begin{array}{l} 2\,|\,54 \\ 2\,|\,27-0 \\ 2\,|\,18-1 \\ 2\,|\,9-0 \\ 2\,|\,4-1 \\ 2\,|\,2-0 \\ \quad 1-0 \end{array} \qquad \begin{array}{r} 0.78 \\ \times 2 \\ \hline 1.56 \\ \times 2 \\ \hline 1.12 \\ \times 2 \\ \hline 0.24 \end{array}$$

11.01 = 1011.0000

$$\begin{array}{l} 2\,|\,11 \\ 2\,|\,5-1 \\ 2\,|\,2-1 \\ \quad 1-0 \end{array} \qquad \begin{array}{r} .01 \\ \times 2 \\ \hline 0.02 \\ \times 2 \\ \hline 0.04 \\ \times 2 \\ \hline 0.08 \\ \times 2 \\ \hline 0.16 \end{array}$$

decimal → octal

54.78 = 66.617

$$\begin{array}{l} 8\,|\,54 \\ 8\,|\,6-6 \\ \quad 0-6 \end{array} \qquad \begin{array}{r} .78 \\ \times 8 \\ \hline 6.24 \\ \times 8 \\ \hline 1.92 \\ \times 8 \\ \hline 7.36 \end{array}$$

11.01 = 13.005

$$\begin{array}{l} 8\,|\,11 \\ 8\,|\,1-3 \\ \quad 0-1 \end{array} \qquad \begin{array}{r} 0.01 \\ \times 8 \\ \hline 0.08 \\ \times 8 \\ \hline 0.64 \\ \times 8 \\ \hline 5.12 \end{array}$$

6
~~78~~×8
~~62~~ 64×8
4992
192

decimal → hexadecimal

54.78 = 36.127

$$\begin{array}{l} 16\,|\,54 \\ 16\,|\,3-6 \\ \quad 0-3 \end{array} \qquad \begin{array}{r} 0.78 \\ \times 16 \\ \hline 12.48 \\ \times 16 \\ \hline 7.68 \end{array}$$

11.01 = 11.028

$$\begin{array}{l} 16\,|\,11 \\ \quad 0-11 \end{array} \qquad \begin{array}{r} .01 \\ \times 16 \\ \hline 0.16 \\ \times 16 \\ \hline 2.56 \\ \times 16 \\ \hline 8.96 \end{array}$$

2 36×8
736

8/100 ×8
64/100 ×8 = 512

78×16
1248

48×16
768

16×1/100

16×16 = 256

56×16
896

54.78 = 1001010.110

$$\begin{array}{l|l} 2 & 54 \\ 2 & 27 - 0 \\ 2 & 18 - 1 \\ 2 & 9 - 0 \\ 2 & 4 - 1 \\ 2 & 2 - 0 \\ & 1 - 0 \end{array}$$

0.78
× 2
1.56
× 2
1.12
× 2
0.24

11.01 = 1011.0000

$$\begin{array}{l|l} 2 & 11 \\ 2 & 5 - 1 \\ 2 & 2 - 1 \\ & 1 - 0 \end{array}$$

.01
× 2
0.02
× 2
0.04
× 2
0.08
× 2
0.16

decimal → octal

54.78 = 66.617

$$\begin{array}{l|l} 8 & 54 \\ 8 & 6 - 6 \\ & 0 - 6 \end{array}$$

.78
× 8
6.24
× 8
1.92
× 8
7.36

11.01 = 13.005

$$\begin{array}{l|l} 8 & 11 \\ 8 & 1 - 3 \\ & 0 - 1 \end{array}$$

0.01
× 8
0.08
× 8
0.64
× 8
5.12

$\cancel{78} \times 8$
$\cancel{62}4 \times 8$
49.92
192

$\frac{8}{100} \times 8$
$= \frac{64}{100} \times 8 = 512$

decimal → hexadecimal

54.78 = 36.127

$$\begin{array}{l|l} 16 & 54 \\ 16 & 3 - 6 \\ & 0 - 3 \end{array}$$

0.78
× 16
12.48
× 16
7.68

11.01 = 11.028

$$\begin{array}{l|l} 16 & 11 \\ & 0 - 11 \end{array}$$

.01
× 16
0.16
× 16
2.56
× 16
8.96

78×16
1248

48×16
7.68

$16 \times \frac{1}{100}$

$16 \times 16 = 2\text{?}$

56×16
896

HD Conversion of no. from any other number system

① De

$101.10 \rightarrow$

$1 \times 5^1 + 0 \times 5^2$

$(101)_2 = (?)_{10}$

$\times 2^2 + \times 2^1 + \times 2^0$

43210
10101

② a Decimal $= 2^0 \times 1 + 2^2 \times 1 + 2^4 \times 1$

$= 1 + 4 + 16 = 21$

$110.011 = 2^1 \times 1 + 2^2 \times 1 = 6.375 = 6.375$

$0 \times 2^{-1} + 1 \times 2^{-2} + 1 \times 2^{-3}$

c $= \frac{1}{4} + \frac{1}{8} = \frac{3}{8} = 0.375$

$(35.2)_8 = 8^0 \times 5 + 8^1 \times 3 = 5 + 24 = 29$

$= 29.25$

$2 \times 8^{-1} = \frac{2}{8} = \frac{1}{4} = 0.25$

$(57.3B)_{16}$ B → 11

$7 \times 16^0 + 5 \times 16^1 . 3 \times 16^{-1} + 11 \times 16^{-2}$

$= 87.2304$

Binary Base = 2

Octal base = 8 2^3 $00(1\,010) = (12).$

③ Hexadecimal base = 16 1 2

$(12)_8 = (?)_{16}$

$(001\,010)_2 = (A)_{16}$

$0100111010011.01 = (12353.2)_8$

2 3 5 3

$0100\,1110\,1011.0100$ $2^1 + 2^2 + 2^3$ $2^1 \times$

4 14 11

$= 41411.24$

$= (4EB.4)_{16}$

convert $(B9F.AE)_{16}$ to octal = (11915.1014)

1001 1001 1101

B 9 F A E

0 1011 1001 1111 1010 1110 = 010111001 1111 10101110

Complement :-

$$\begin{array}{r} 0 \\ 10 \\ \hline 0 \end{array} \quad \begin{array}{r} 0 \\ 11 \\ \hline 1 \end{array} \quad \begin{array}{r} 1 \\ 10 \\ \hline 1 \end{array} \quad \begin{array}{r} 1 \\ 11 \\ \hline 2 = 10 \end{array}$$

0 +1, 1 +1, 10 +1, 11

111010
000101 → 1 complement
+1
000110 → 2 complement

1111
0000
+1
0001

Assignment

Find 1's & 2's complement of 1011.11

for 2's complement add 1 to last significant digit (may be de or ...)

1011.11

1's → 0100.00
+ 1
2's → 0100.01

Representation of binary numbers:

If no. is +ve put 0 in last
-ve " 1 in last

3 → 011
-3 → 111
} represented as sign magnitude

Hao	Sign	magnitude no	
① Deli +12	0	10	= 010
	sign	magnitude	
It +7	0	111	= 0111
v −5	1	11	= 111
② wa −2	1	10	= 110
Ir −12	1	1100	= 11100
+6	0	110	= 0110

In binary no. system there are 3 different ways to represent or write a −ve number

→ sign magnitude representation
→ 1's complement representation
→ 2's complement representation

Sign-magnitude

5 - 101

— mag

+5 0 101 → 0101
−5 1 101 → 1101

1's complement :

→ check the no
→ If the no is −ve positive no. using sign magnitude format then take 1's complement of that no.

If +ve or −ve
→ +ve sign magnitude
→ then it's 1's complement

+6

SM = 0 110

S1's = 0 110

S2's = 0 110

-6

SM = 1 110

S1's = 1001 $\quad$ $\underline{0110}$

S2's = 1010

sign mag $\quad$ sign 1's

Binary Arithmetic operation

$$\begin{array}{r} 00111010 \\ 00011100 \\ \hline 00100110 \end{array}$$

110.10 + 111.10 = 110.00

$$\begin{array}{r} 110.10 \\ 111.10 \\ \hline 1010.00 \end{array}$$

subtraction:

$$\begin{array}{r} 10110 \\ 11011 \\ \hline 01101 \end{array}$$

$$\begin{array}{r} 0 \\ -0 \\ \hline 0 \end{array} \quad \begin{array}{r} 1 \\ -1 \\ \hline 0 \end{array} \quad \begin{array}{r} 1 \\ -0 \\ \hline 1 \end{array} \quad \begin{array}{r} 0 \\ -1 \\ \hline 1 \end{array} \quad \begin{array}{r} 1 \\ +1 \\ \hline 10 \end{array} -1 \quad \begin{array}{r} 1 \\ \hline 11 \end{array} -1$$

$$\begin{array}{r} 11011 \\ -10110 \\ \hline 00101 \end{array}$$

Subtract 1100 from 11010

$$\begin{array}{r} 11010 \\ -1100 \\ \hline 01110 \end{array}$$

110

Binary multiplication:

$$\begin{array}{r} 1010 \\ 1001 \\ \hline 1010 \\ 0000 \\ 0000 \\ 1010 \\ \hline 1011010 \end{array}$$

$$\begin{array}{r} 1010 \times 1001 \\ \hline 1010 \end{array}$$

$$\begin{array}{r} 1001.11 \\ 10.1 \\ \hline \end{array}$$

$$\begin{array}{r} 100111 \times 101 \\ \hline 100111 \\ 000000 \\ 100111 \\ \hline 11000011 \end{array}$$

$$110 \overline{)100001} (101$$
$$\frac{-110}{001001}$$
$$\frac{110}{0011}$$

$$101 \overline{)11010} | 101$$
$$\frac{1001}{01010}$$
$$\frac{-1001}{0001}$$
10000

Logic gates :-

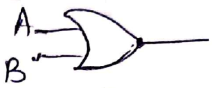
Gate	Symbol	T.T

NOT (A')
0/1

A	A'
1	0
0	1

OR

(It is sensitive to input 1)

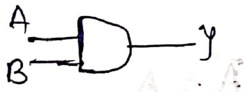


$Y = A+B$

A	B	A+B
0	0	0
0	1	1
1	0	1
1	1	1

AND

(sensitive to input 0)



$Y = A \cdot B$

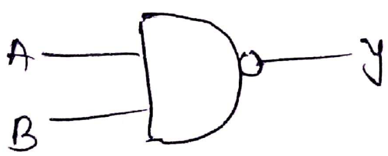
A	B	A.B
0	0	0
0	1	0
1	0	0
1	1	1

NOR

$Y = \overline{A+B}$

A	B	$\overline{A+B}$
0	0	1
0	1	0
1	0	0
1	1	0

NAND

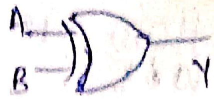


$Y = \overline{A \cdot B}$

A	B	$\overline{A \cdot B}$
0	0	1
0	1	1
1	0	1
1	1	0

Ha EX-OR

① Dei

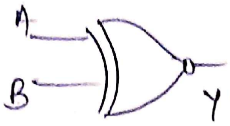


$Y = A \oplus B$

$= A'B + AB'$

A	B	$A \oplus B$
0	0	0
0	1	1
1	0	1
1	1	0

② Q EX-NOR



$Y = \overline{A \oplus B}$

$= \overline{A'B + AB'}$

A	B	$\overline{A \oplus B}$
0	0	1
0	1	0
1	0	0
1	1	1

C

Boolean Algebra:

A

$1 + 1 = 1$

$0 + 0 = 0$

So, (1) $A + A = A$ (5) $A + 0 = A$ (9) $\bar{\bar{A}} = A$

(2) $A \cdot A = A$ (6) $A \cdot 0 = 0$ (10) $A + AB = A$

(3) $A + 1 = A$ (7) $A + \bar{A} = 1$ (11) $A + \bar{A}B = A + B$

(4) $A \cdot 1 = A$ (8) $A \cdot \bar{A} = 0$ (12) $(A+B)(A+C) = A + BC$

③

(10) $A + AB$

$= A(1 + B)$

$= A$

(11) $A + \bar{A}B$

$= (A + \bar{A}).(A + B)$

$= A + B$

(12) $(A+B)(A+C)$

$= AA + AC + AB + BC$

$= A + AC + AB + BC$

$= A + BC$

3 laws of boolen algebra

(1) commutative law:

$A + B = (B + A)$ (OR operator)

$A \cdot B = B \cdot A$ (AND operation)

Associative law:-

$(A+B)+C = A+(B+C)$

Distributive law :-

$A\cdot(B+C) = (A\cdot B)+(A\cdot C)$

$A+(B\cdot C) = (A+B)\,(A+C)$ (Valid in boolean algebra but not in mathematical algebra)

De-morgan's Theorm:-

(1) $\overline{A+B} = \bar{A}\cdot\bar{B}$

De morgan's theorm is defined as,

(2) $\overline{A\cdot B} = \bar{A}+\bar{B}$

$(A+BC) = (A+B)\cdot(B\cdot A+C)$

$= A\cdot A + A\cdot C + B\cdot A + B\cdot C$

(10) $(A+AB) = (A+A)\cdot(A+B)$

$= A(1+B)$

$= A$

(11) $(A+\bar{A}B) = (A+\bar{A})\cdot(A+B)$

$= 1\cdot(A+B)$

$= (A+B)$

(12) $(A+B)\,(A+C) = A\cdot A + A\cdot C + A\cdot B + B\cdot C$

$= A + AC + AB + BC$

$= A(1+C) + B$ $= A(1+C+B) + BC$

$= A +$ $= A+BC$

Proofs of De-morgan's theorem:

Let A and B be 2 input, then According to demorgan's theorem, following can be proved

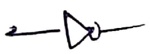
1. $\overline{A \cdot B} = \bar{A} + \bar{B}$

2. $\overline{A+B} = \bar{A} \cdot \bar{B}$

A	B	$A \cdot B$	$A+B$	$\overline{A \cdot B}$	$\overline{A+B}$	$\bar{B}$	$\bar{A}$	$\bar{A}+\bar{B}$	$\bar{A} \cdot \bar{B}$
1	0	0	1	1	0	1	0	1	0
0	0	0	0	1	1	1	1	1	1
0	1	0	1	1	0	0	1	1	0
1	1	1	1	0	0	0	0.	0	0.

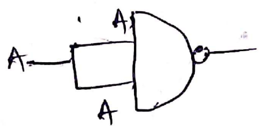
NAND, NOR gates are called universal logic gates
(we can replace any other gate with these 2 gates)

NAND:

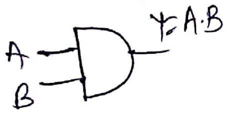


NAND:

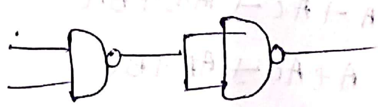
$Y = \overline{A \cdot A} = \bar{A}$ $\quad Y = \overline{A \cdot B}$



AND



using NAND gate

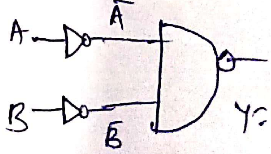


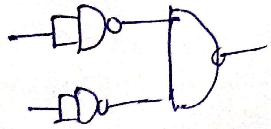
OR

$\overline{A' \cdot B'} = \bar{\bar{A}} + \bar{\bar{B}}$

$= A+B$

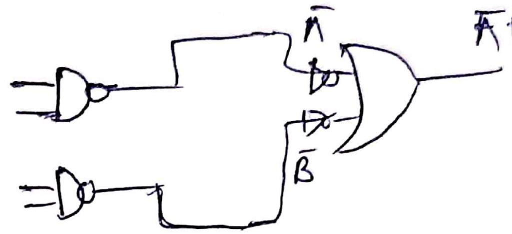
NAND:





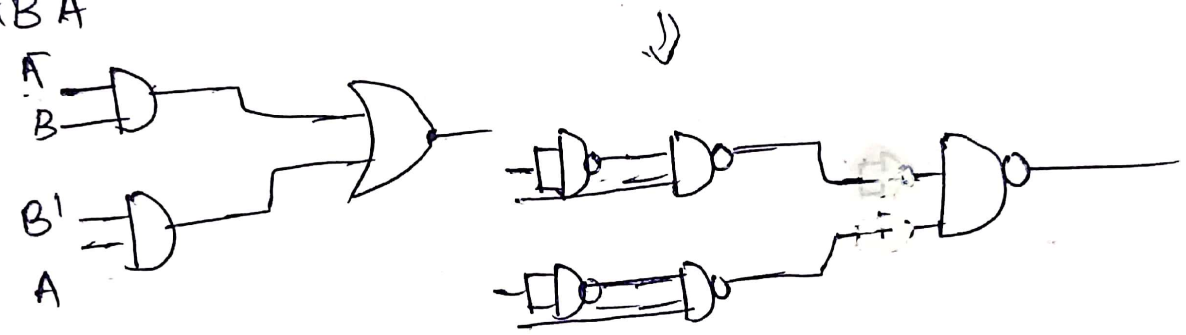
EX-OR gate

NAND



$Y = A'B + B'A$

$Y = \overline{A \cdot B}$



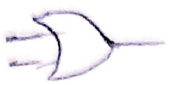
Implement EX-OR, EX-NOR using min NAND gate

Show that NOR gate is also universal gate

... gate is also universal gate

NOR gate as universal gate:

(1) OR



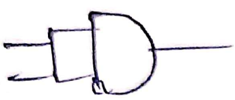
$Y = A+B$

$Y = ((A+B)')'$

$= A+B$

$Y = A+B$

AND

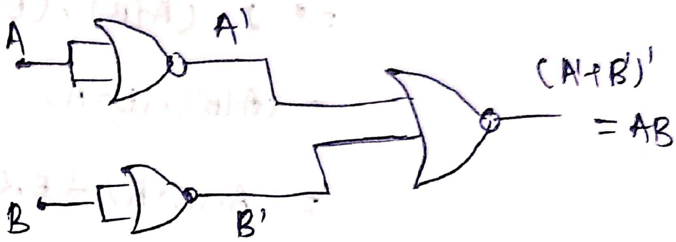


$Y = A \cdot B$

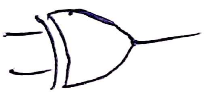
$(A+B)' = A'B'$

$(A'+B')' = A''B'' = AB$

$Y = (A'+B')' = AB$



EX-OR



$Y = A \oplus B$

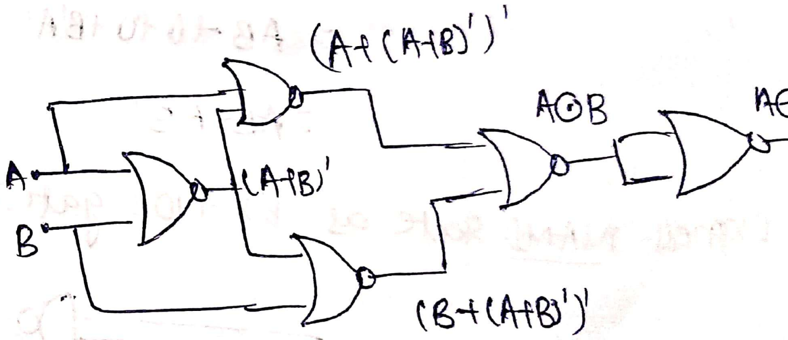
$(A+(A+B)')'$.

$= (A + \overline{(A+B)})$

$= \bar{A} \cdot (A+B)$

$= \bar{A} \cdot A + \bar{A} \cdot B$

$= 0 + A'B = A'B$



$(B+(A+B)')' = \bar{B} \cdot (A+B)$

$= \bar{B} \cdot A + \bar{B} \cdot B$

$= \bar{B} \cdot A$

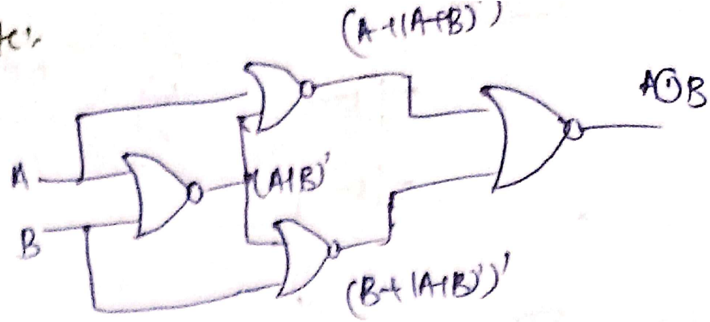
$= B'A$

$Y = (A+(A+B)')' + (B+(A+B)')'$

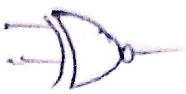
$= A'B + B'A$

Scanned with OKEN Scanner

NOR as EX-NOR gate:-



EX-NOR



$Y = A'B' + AB$

Gate No.	Inputs	Output
1	A, B	$(A+B)'$
2	A, $(A+B)'$	$(A+(A+B)')'$
3	$(A+B)'$, B	$(B+(A+B)')'$
4	$(A+(A+B)')'$, $(B+(A+B)')'$	$AB+A'B'$

$$Y = \overline{(A+(A+B)')' + (B+(A+B)')'}$$

$$= \overline{(A+(A+B)')'} \cdot \overline{(B+(A+B)')'}$$

$$= (A+(A+B)') \cdot (B+(A+B)')$$

$$= (A+A'B') \cdot (B+A'B')$$

$$= (A+A') \cdot (A+B') \cdot (B+A') \cdot (B+B')$$

$$= 1 \cdot (A+B') \cdot (B+A') \cdot 1$$

$$= (A+B') \cdot (B+A')$$

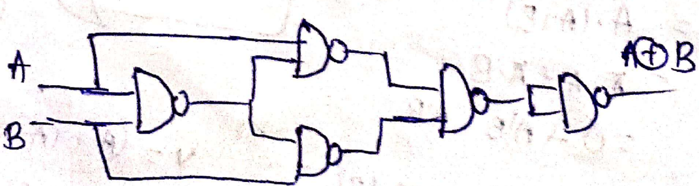
$$= A \cdot (B+A') + B' \cdot (B+A')$$

$$= AB + AA' + B'B + B'A'$$

$$= AB + 0 + 0 + B'A'$$

$$= AB + A'B'$$

Express- NAND gate as EX-NOR gate:-



Boolean Algebra :-

use the Rules of Boolean Algebra express as boolean functions.

$f_1(A,B,C) = A'B'C' + A'BC + AB'C' + AB'C + ABC' + ABC$

$= A'B(C+C') + AB'(C+C') + AB(C+C')$

$= A'B(1) + AB'(1) + AB(1)$ (as $C+\bar{C} = 1$)

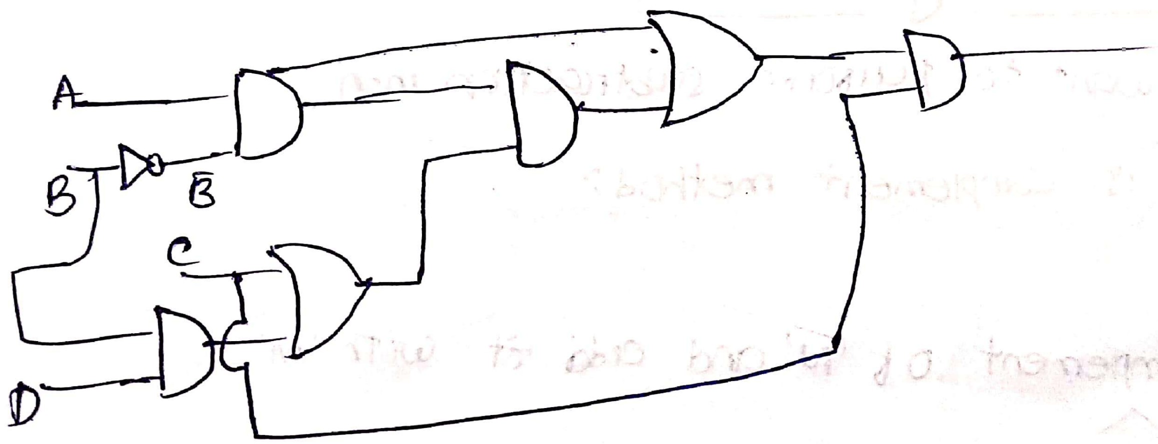
$= A'B + AB' + AB$

$= A'B + A(B+B')$

$= A'B + A$

$= A+B$

$F_2(A,B,C) = (AB'(C+BD) + A'B')C$



$f = (AB'(C+BD)) + A'B')C$

$= (AB'C + \cancel{AB'BD}^{0} + A'B')C$

$= (AB'C + A'B')C = AB'C.C + A'B'.C$

$= AB'C + A'B'C$

$= B'(A'+AC)$

$= B'C(A+A')$

$= B'C(1)$

$= B'C$

$F = \overline{A\bar{B}\cdot(A+1)} + \bar{A}B\cdot\overline{((\bar{A}+B)+\bar{C})}$

$\qquad\qquad\qquad\qquad\qquad\qquad\qquad\quad a \quad\; b$

$= \overline{A\bar{B}} + \overline{(A+C)} + \bar{A}B\cdot\overline{(\bar{A}+B)}\cdot\bar{\bar{C}}$

$= \bar{A}B + \bar{A}\cdot\bar{C} + \bar{A}B\cdot(\overline{\bar{A}+B})\cdot C$

$= \bar{A}B + \bar{A}\cdot\bar{C} + \bar{A}B\cdot\cancel{(\overline{\bar{A}+B})}^{0}\cdot C$

$= \bar{A}B + \bar{A}\cdot\bar{C} + \cancel{\bar{A}B\cdot C}^{0}$

$= \bar{A}B + \cancel{\bar{A}B\bar{C}}^{0} + \bar{A}\cdot\bar{C}$

$= \bar{A}B + \bar{A}\cdot\bar{C}$

$= \bar{A}\cdot(B+\bar{C})$

Simplify $AB + \bar{A}C + BC = AB + \bar{A}C$

$AB + \bar{A}C + BC$

$= AB + C(\bar{A}+B)$

$= AB + C\cdot\bar{A} + C\cdot B$

$= AB + C\cdot\bar{A} + C\cdot B$

$AB + \bar{A}C + BC\cdot 1$

$= AB + \bar{A}C + BC(A+\bar{A})$

$= AB + \bar{A}C + BCA + BC\bar{A}$

$= AB + ABC + \bar{A}C + \bar{A}CB$

$= AB(1+C) + \bar{A}C(1+B)$

$= AB + \bar{A}C$

Binary subtraction using complement:-

Let us say we want to perform subtraction m-n

subtraction using 1's complement method:-

Step :-

(1) Add the 1's complement of 'N' and add it with 'M'.

(2)

if no carry comes

→ Result is -ve (N is higher than M)

→ Put a -ve sign

→ take 1's complement of addition result

if carry comes

110 010

1's complement of N - 101

+ 110
101
(1)011

carry bits

Add the carry with the result

011
1
100

$1+2+8 = 11$
-13
-2

Subtract 010 with 110

N - 110 1's complement 001

010
+ 001
(0) 11

= 011

1's complement - 100

M ← 1011
N ← 1101

'N' 1's → 0010

1011
+ 0010
1101

- (0010)

Subtraction using 2's complement method

(1) Add 2's complement N with M

if carry comes
→ simply discard that carry

If no carry comes
→ Result is -ve
→ put a -ve sign
→ Take 2's complement of addition result

1011
1101

2's complement of N → 1101 → 0010
+1
0011

1011
0011
1010

Result
= -(0101)

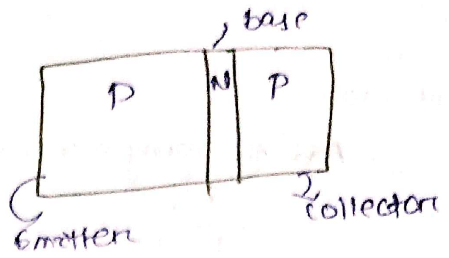
1101
1011

2's complement of N →
0100
+ 1
0101

1101
0101
(1)0010
(X)

Result = (0010)

J_1	J_2
FB	FB
RB	RB
RB	RB
FB	RB
RB	FB



VBE

(1) Structure
(2) Dopping
(3) Physical width

Emitter → heavily doped
base – least doped
collector → moderately doped

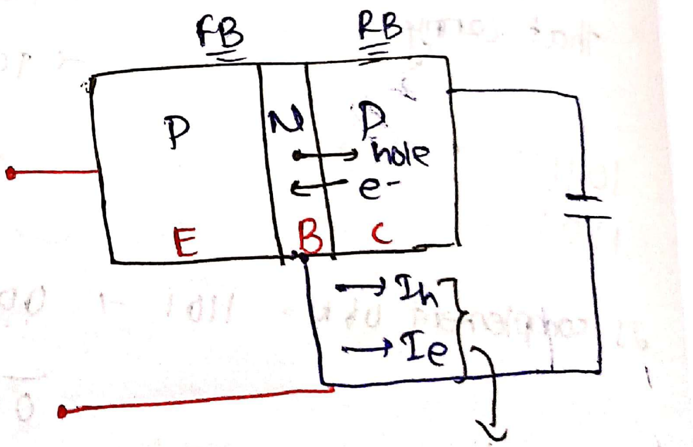
J_1 (E-B) Emitter-base jun^n	J_2 (B-C) base-collector junction	
FB	FB	Saturation region (ON switch)
RB	RB	cutoff region (off switch)
FB	RB	Active region (amplifier)
RB	FB	Reverse Active region (

Reverse Active region:-

* Emitter is heavily doped
  high concentration of holes

* Forward bias (majority carrier can cut the jun^n)

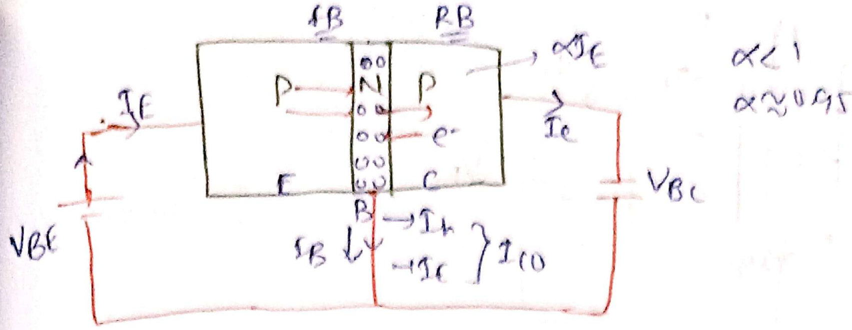
* Reverse bias (minority carrier can cut the junction)



I_{CO} or I_{CBO}

* I_{CO}/I_{CBO} is the current flow through collector & base when junction is open

→ magnitude is sum of I_h

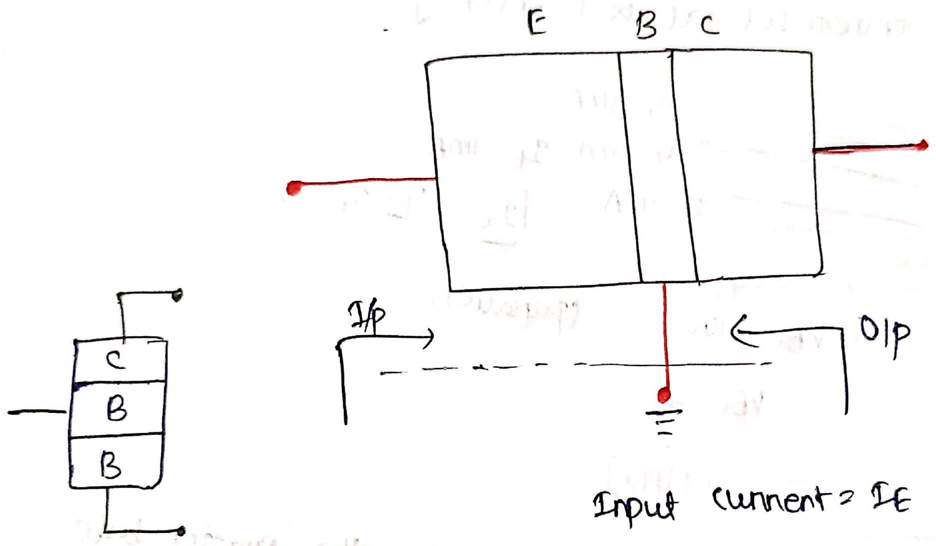


$\alpha < 1$
$\alpha \approx 0.95$

So Net current $I_c = \alpha I_E + I_{CO}$ (as both are flowing from base to collector)

$I_E = I_c + I_B$

Discuss the construction and current flow mechanism of transistor in Active region of operation.



Input current = I_E output current = I_c

Input Voltage = V_{BE} output voltage = V_{CE}

Output characteristics of transistor in common base configuration:-

i) In common base configuration

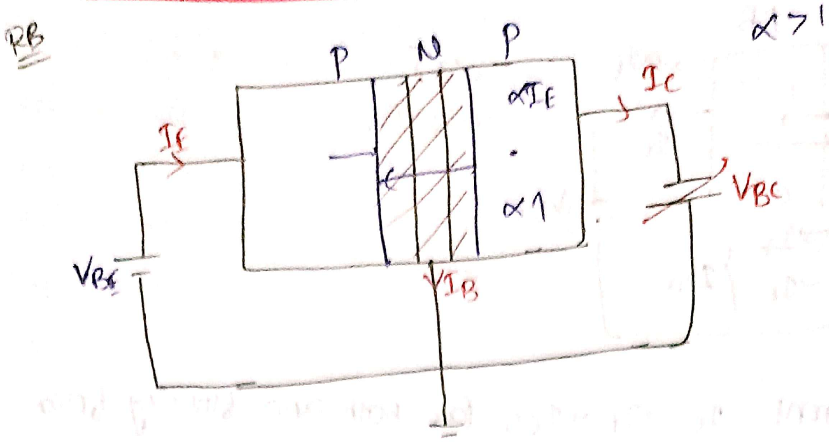
→ output terminals are collector and base

(ii) so, the output characteristics is graph between output voltage (V_{CB}) to output current (I_c) keeping O/P constant

→ BJT is a current controlled voltage source

RB

$\alpha > 1$

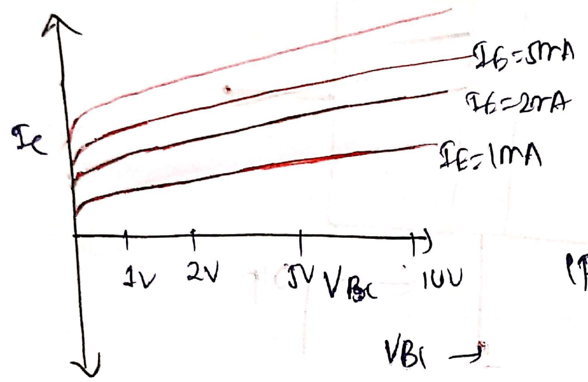


→ when forward biased, depletion layer will increases

$$I_C = \alpha I_E + I_{CO}$$

→ when Reverse biasing potential, Reverse saturation current remains constant

I_C will increases as α 1 (keeping I_E constant)



$I_E = 1mA$

$\uparrow I_C = \uparrow \alpha I_E + I_{CO}$

(parallel)

Active region of operation:- (NPN)

→ The active region is defined as region in which the emitter-base junction is forward biased and collector-base junction is reverse biased

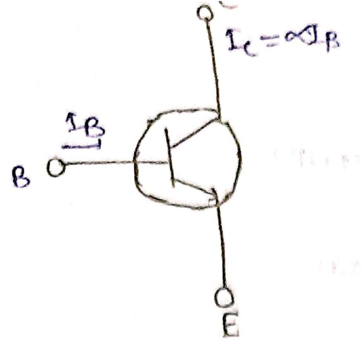
→ A transistor while in this region will act as amplifier

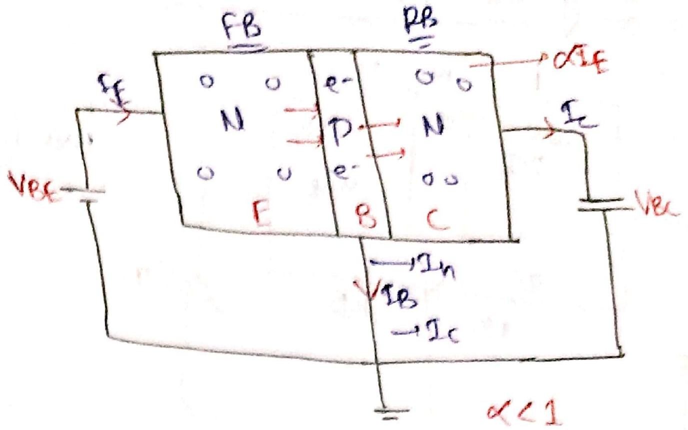
→ This region lies between cutoff and saturation

Here Emitter-base → Forward biased

base-collector → Reverse biased

→ Here width of base-emitter junction is small, while compared to the width of collector-base junction.





Here $V_{BE} = V_B - V_E > 0$

$\Rightarrow V_B > V_E$

$V_{CB} = V_C - V_B > 0$

$V_C > V_B$

So $V_C > V_B > V_E$

$\alpha < 1$

$\alpha \approx 0.95$

Net collector current $I_C = \alpha I_E + I_{CO}$

PRINCIPLE :-

(i) usually base of NPN transistors are thin and lightly doped, so it has fewer holes as compared to the electrons in emitter.

(ii) The recombination of holes in the base with electrons in emitter region will constitute flow of base current.

(iii) Then the remaining large number of electrons in emitter will cross Reverse biased collector junction in the form of collector current

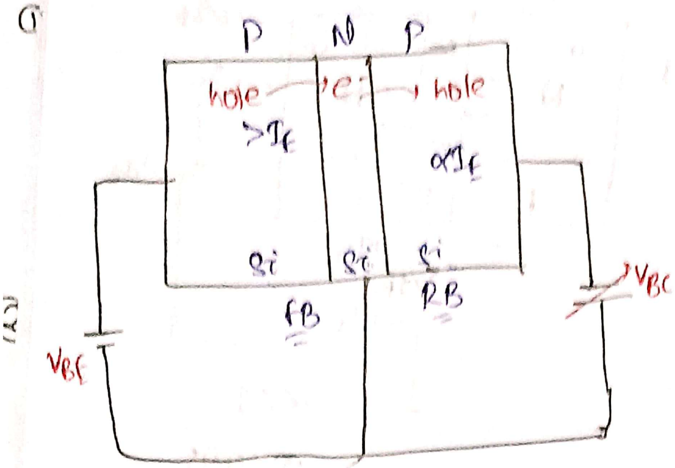
(iv) According to Kirchoff's current law, the emitter current is equal to the sum of collector current and base current.

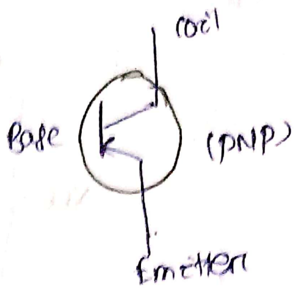
(V) Generally, the base current I_B will remain small when compared to collector current and emitter current

$$I_E = I_C + I_B$$

(vi) In transistor, if collector current ↑ → collector temperature ↑ so, resistance will get reduced hence collector I_C↑, this phenomenon is known as thermal runway in BJT

Early effect / base-width modulation :-





- when $V_{BC} \uparrow$ → depletion layer will ↑
- depletion layer will be more towards base than collector
- → Due to narrower region, electron-hole recomb^n will decrease,

so $V_{CB} \uparrow \rightarrow \alpha \uparrow$

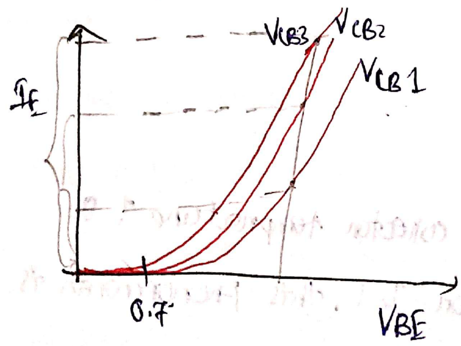
$I_B \downarrow$

$I_E \uparrow$

- I_E value increases due to increasing concentration gradient. this effect of effective width-variation is called as base-width modulation / Early effect due to reverse biasing potential V_{CB}

Input characteristics :-

- It is the curve between VBE and I_E
- It has requirement of (0.7V)



$V_{CB3} > V_{CB2} > V_{CB1}$

$I_C = \alpha I_E + I_{CBO}$

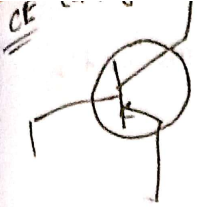
$I_C \simeq \alpha I_E$ Since I_{CBO} is due to min carriers so less th

$I_i = I_E$ $I_o = I_C$

Transistor in common base configuration can never be employed as current amplifier

$\alpha = \frac{I_C}{I_E}$ $\alpha < 1$ α is current amplification factor in common base-configuration

CE



	I/P	O/P
VOH	V_{BE}	V_{CE}
curn	I_B	I_C

$\beta = \frac{I_C}{I_B}$

β is the current amplification factor in common

$\beta = \frac{I_C}{I_B}$

$I_E = I_C + I_B$

$\frac{I_E}{I_E} = \frac{I_C}{I_E} + \frac{I_B}{I_E}$

$1 = \alpha + \frac{I_C}{\beta I_E}$ $\quad (I_B = \frac{I_C}{\beta})$

$1 = \alpha + \frac{\alpha}{\beta}$

$1-\alpha = \frac{\alpha}{\beta}$ $\Rightarrow \boxed{\beta = \frac{\alpha}{1-\alpha}}$

$\alpha = \frac{I_C}{I_E}$

$I_E = \frac{I_C}{\alpha}$

$I_E = I_C + I_B$

$\frac{I_E}{I_B} = \frac{I_C}{I_B} + \frac{I_B}{I_B}$ 1

$\frac{I_C}{\alpha \cdot I_B} = \beta + 1$

$\Rightarrow \frac{\beta}{\alpha} = \beta + 1$ $\Rightarrow \boxed{\alpha = \frac{\beta}{1+\beta}}$

value of β ranges between 40 to 400

$\beta = \frac{0.5}{0.5} = 1$

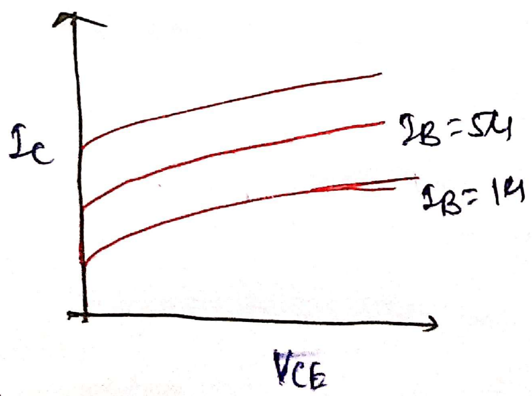
$\beta = \frac{0.6}{1-0.6} = \frac{0.6}{0.4} =$

$= 1.5$

with increasing α, $\beta \uparrow$

Output characteristics of CE:-

output characteristic for CE configuration is the graph between output voltage V_{CE} and I_C keeping input current I_B configuration



$I_C = \alpha I_E + I_{CO}$

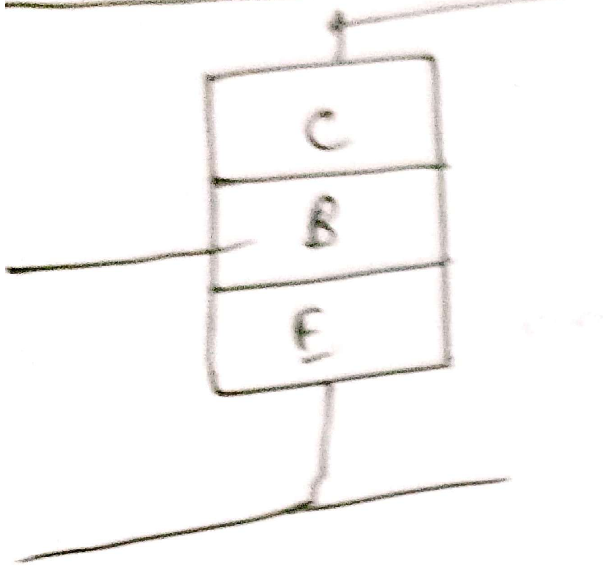
$I_C \approx \alpha I_E$

$I_C \approx \beta I_B$

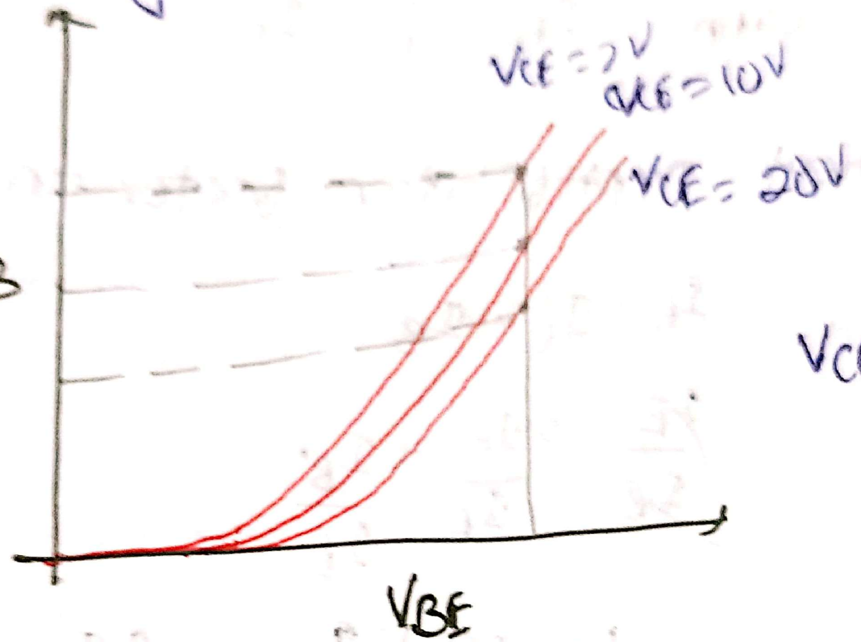
(Increased)

* find Regions. active, saturation and cut-off region in the characteristic curve

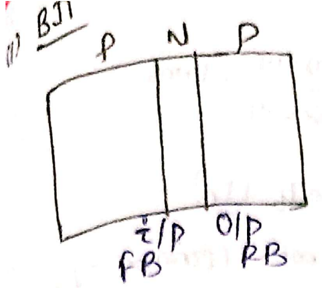
put characteristics:-



Keeping voltage const, curve between V_{BE} and I_B keeping V_{CE} const



$V_{CE_1} > V_{CE_2} > V_{CE_3}$

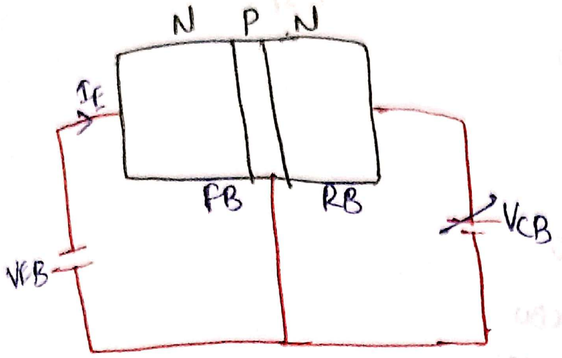


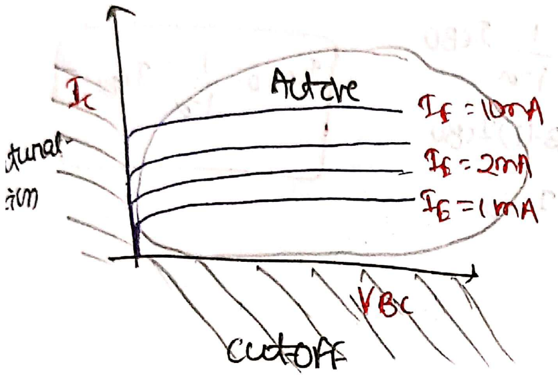
Due to hole e^-

$I_C = \alpha I_E + I_{CO}$ $\quad I_E = I_C + I_B$

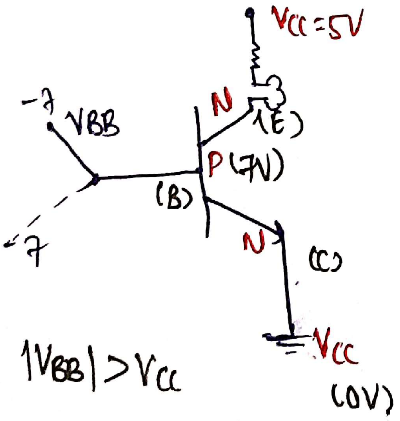
$I_C = \alpha I_E$, $I_C = \beta I_B$

Due to transfer of resistor, it is called transistor





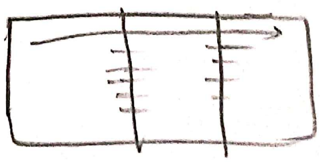
Transistor as a switch:

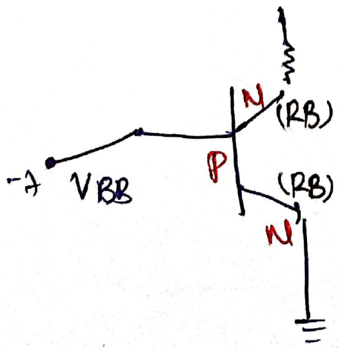


cutoff → (RB) → Off

Saturation → (FB) → ON

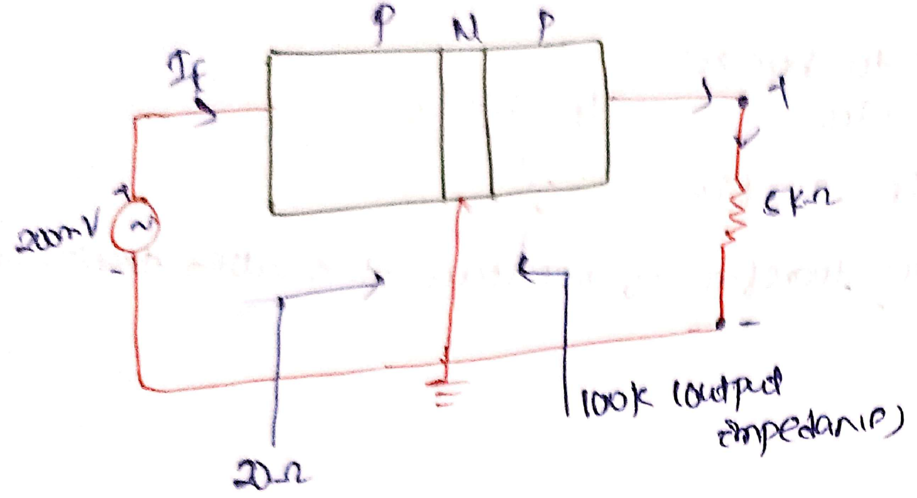
Since both junctions are FB, so it will act as shorted-circuit in Emitter-collector junction.





Since both junc are reverse-biased. it will act as off-switch

(open circuit) → No current will flow through it.

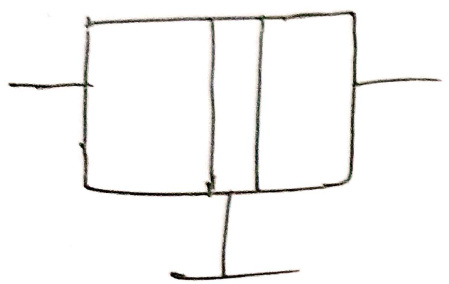


$I_E = \frac{200mV}{20\Omega} = 10mA$

$I_C = \alpha I_E + \cancel{I_{CO}}$

$= \alpha I_E$ (since $\alpha \approx 1$)

$\approx I_E$



$I_C = \alpha I_E + I_{CBO}$

$= \alpha (I_C + I_B) + I_{CBO}$

$I_C - \alpha I_C = \alpha I_B + I_{CBO}$

$I_C (1-\alpha) = \alpha I_B + I_{CBO}$

$I_C = \frac{\alpha}{1-\alpha} I_B + \frac{1}{1-\alpha} I_{CBO}$

$I_C = \beta I_B + (\beta+1) I_{CBO}$

$= \beta I_B + I_{CEO}$

$$\boxed{I_{CEO} = \frac{1}{1-\alpha} I_{CBO}}$$