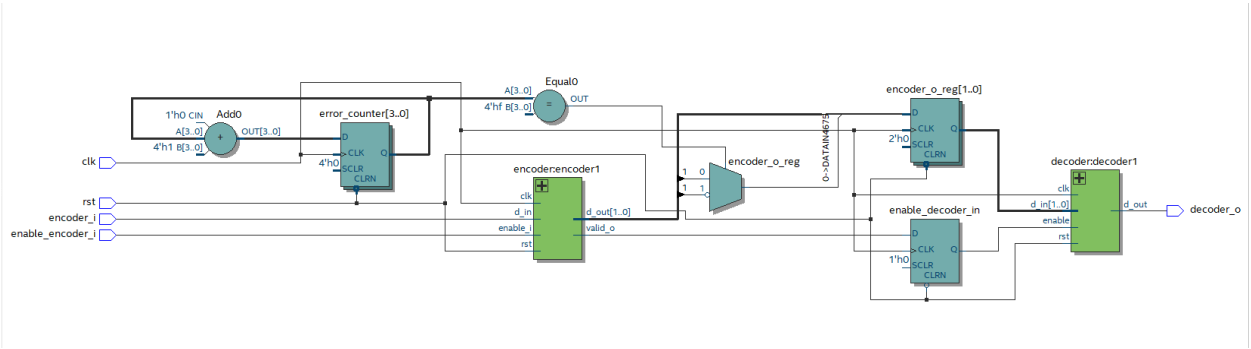
Term Project

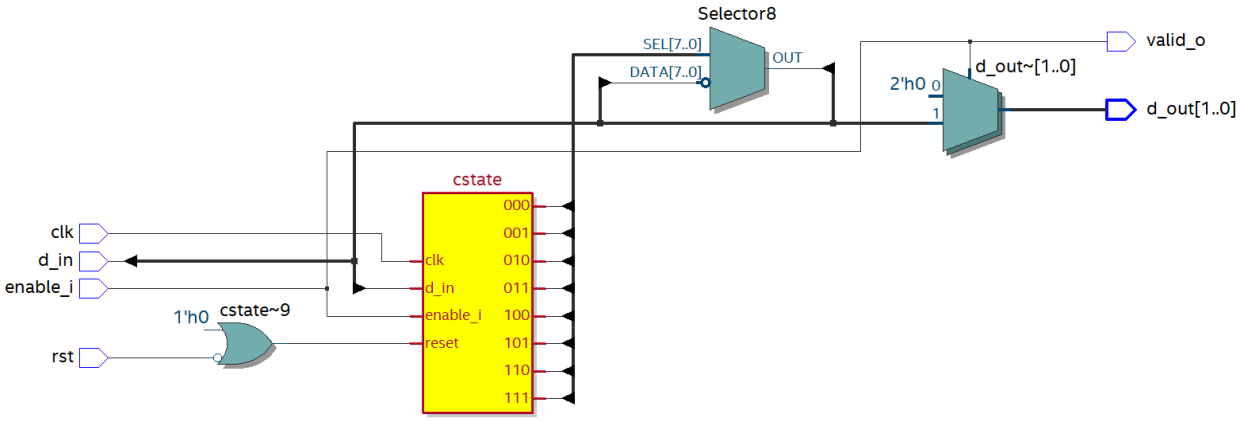
Transcript

```
# yaa! in = 1, out = 1
# yaa! in = 1, out = 1
# good =          256, bad =            0
```

RTL Viewer of top Layer



Encoder

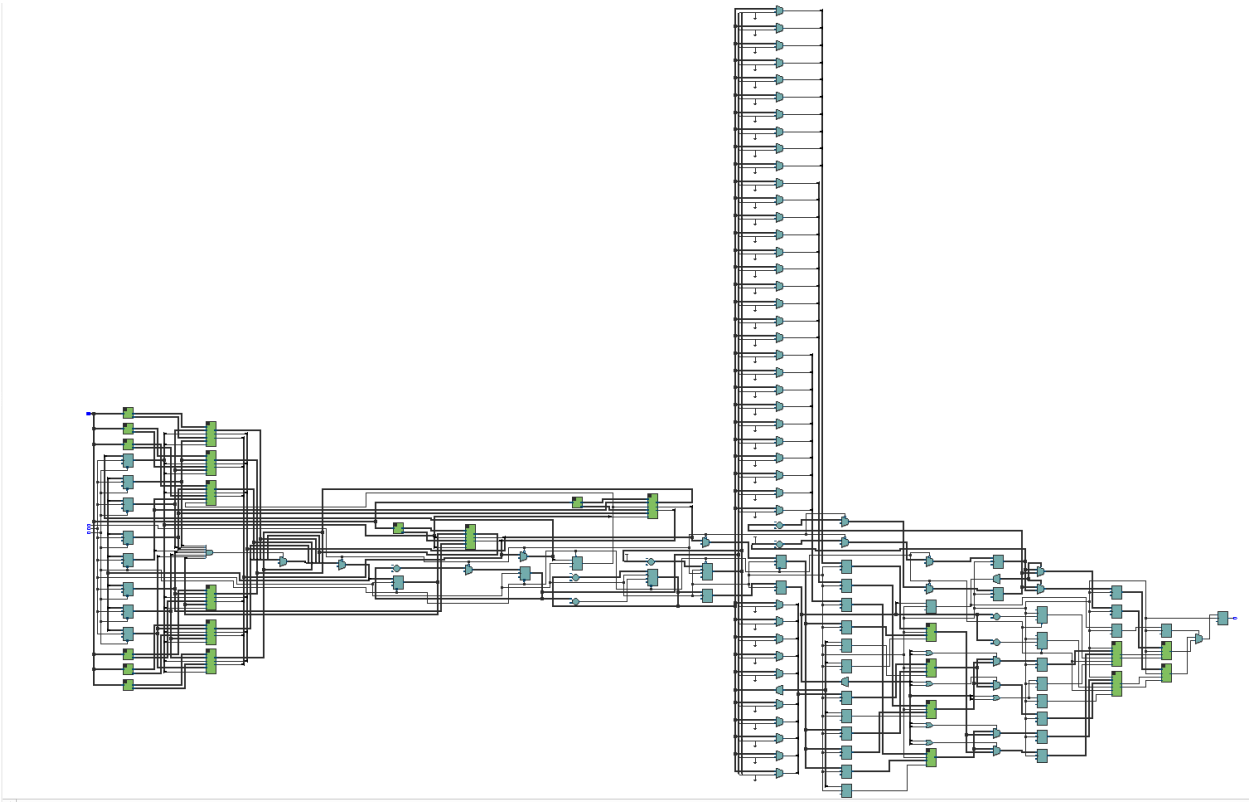


The encoder is a shift register where every clock cycles, the bits shift 1 position to the right. And the left-most bit is determined by the following expression:
nstate[2] = d_in ^ cstate[1] ^ cstate[0]

The encoder also produces a 2-bit output based on the input and the current state:
d_out_reg[1] = d_in ^ cstate[2] ^ cstate[1]
d_out_reg[0] = d_in

	Resource	Usage
1	▼ Estimated ALUTs Used	12
1	-- Combinational ALUTs	12
2	-- Memory ALUTs	0
3	-- LUT_REGs	0
2	Dedicated logic registers	8
3		
4	▼ Estimated ALUTs Unavailable	0
1	-- Due to unpartnered combinational logic	0
2	-- Due to Memory ALUTs	0
5		
6	Total combinational functions	12
7	▼ Combinational ALUT usage by number of inputs	
1	-- 7 input functions	0
2	-- 6 input functions	0
3	-- 5 input functions	0
4	-- 4 input functions	11
5	-- <=3 input functions	1
8		
9	▼ Combinational ALUTs by mode	
1	-- normal mode	12
2	-- extended LUT mode	0
3	-- arithmetic mode	0
4	-- shared arithmetic mode	0
10		
11	Estimated ALUT/register pairs used	12
12		
13	▼ Total registers	8
1	-- Dedicated logic registers	8
2	-- I/O registers	0
3	-- LUT_REGs	0

Decoder



	Resource	Usage
1	▼ Estimated ALUTs Used	392
1	-- Combinational ALUTs	392
2	-- Memory ALUTs	0
3	-- LUT_REGs	0
2	Dedicated logic registers	239
3		
4	▼ Estimated ALUTs Unavailable	85
1	-- Due to unpartnered combinational logic	85
2	-- Due to Memory ALUTs	0
5		
6	Total combinational functions	392
7	▼ Combinational ALUT usage by number of inputs	
1	-- 7 input functions	9
2	-- 6 input functions	86
3	-- 5 input functions	13
4	-- 4 input functions	22
5	-- <=3 input functions	262
8		
9	▼ Combinational ALUTs by mode	
1	-- normal mode	215
2	-- extended LUT mode	9
3	-- arithmetic mode	168
4	-- shared arithmetic mode	0
10		
11	Estimated ALUT/register pairs used	551
12		
13	▼ Total registers	239
1	-- Dedicated logic registers	239
2	-- I/O registers	0
3	-- LUT_REGs	0

	Resource	Usage
1	▼ Estimated ALUTs Used	410
1	-- Combinational ALUTs	410
2	-- Memory ALUTs	0
3	-- LUT_REGs	0
2	Dedicated logic registers	254
3		
4	▼ Estimated ALUTs Unavailable	85
1	-- Due to unpartnered combinational logic	85
2	-- Due to Memory ALUTs	0
5		
6	Total combinational functions	410
7	▼ Combinational ALUT usage by number of inputs	
1	-- 7 input functions	9
2	-- 6 input functions	87
3	-- 5 input functions	13
4	-- 4 input functions	34
5	-- <=3 input functions	267
8		
9	▼ Combinational ALUTs by mode	
1	-- normal mode	233
2	-- extended LUT mode	9
3	-- arithmetic mode	168
4	-- shared arithmetic mode	0
10		
11	Estimated ALUT/register pairs used	570
12		
13	▼ Total registers	254
1	-- Dedicated logic registers	254
2	-- I/O registers	0
3	-- LUT_REGs	0
14		
15		
16	I/O pins	5
17	Total MLAB memory bits	0
18	Total block memory bits	34816
19		
20	DSP block 18-bit elements	0
21		
22	Maximum fan-out node	clk~input
23	Maximum fan-out	288
24	Total fan-out	2747
25	Average fan-out	3.88