

מעבדה VLSI אנלוגי

פרויקט סיכון

מגיש: סמואל ניומן

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Question 1 – Symmetric Inverter

A. Finding the Beta Optimal:

Using cadence virtuso, a simple CMOS inverter was built using a Pmos and Nmos. The width of the NMos was minimum: $W_n = 120nm$, $W_p = 120n * beta$.

$$\text{Beta } (\beta) \text{Ratio} = \frac{\beta_n}{\beta_p} = \frac{\mu_n C_{ox} \frac{W_n}{L_n}}{\mu_p C_{ox} \frac{W_p}{L_p}}$$

Since the oxide capacitance and Length is the same for both NMOS and PMOS transistors, the equation simplifies to:

$$W_n = \beta * W_p.$$

The objective is to find a beta which makes our circuit symmetrical which will give equal rise and fall times for the Inverter.

First the schematic is built using the Pmos and Nmos transistor. Then a symbol is created.

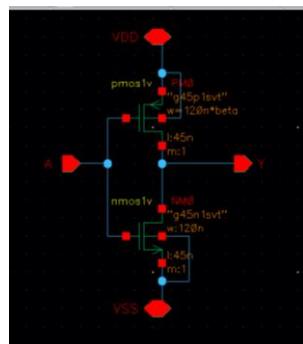


Image 1 - Inverter Beta – Schematic

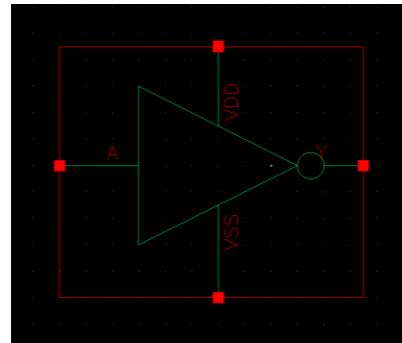


Image 2 - Inverter Beta – Symbol

Then a test bench is created with the Inverter with a pulse input. The Capacitor *Cload* is set as a variable that can be changed in the maestro.

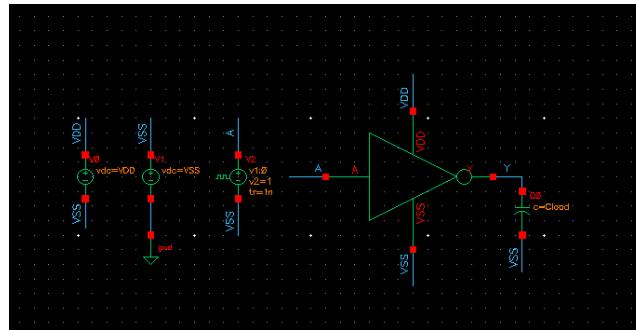


Image 3 - Inverter Beta TB Schematic

In Maestro, the *Cload* is set to 100fF. Beta is swept from 1 to 3 to find at what value the rise and fall times of the circuit are the same. This value will give us the beta that will make our inverter symmetrical. Rise time and Fall time will be investigated in the transient simulation, while the other parameters shown in the maestro will be investigated in the DC analysis.

$$Trise = t(10\%) - t(90\%)$$

$$Tfall = t(90\%) - t(10\%)$$

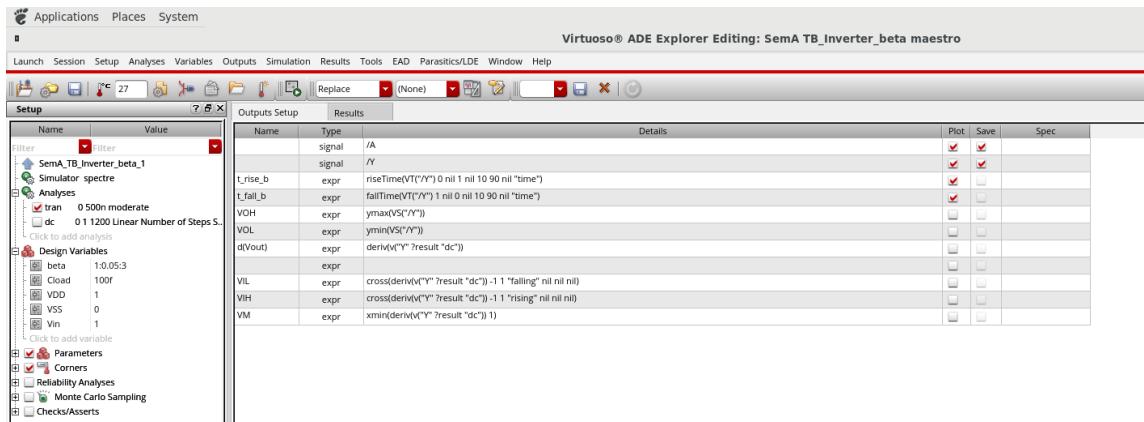


Image 4 - TB Maestro Functions

Since beta is affecting the Width of the PMOS, this will change the rise time of the circuit since the PMOS affects the Pull Up of the CMOS (from 0-VDD).



Image 5 – Transient Simulation

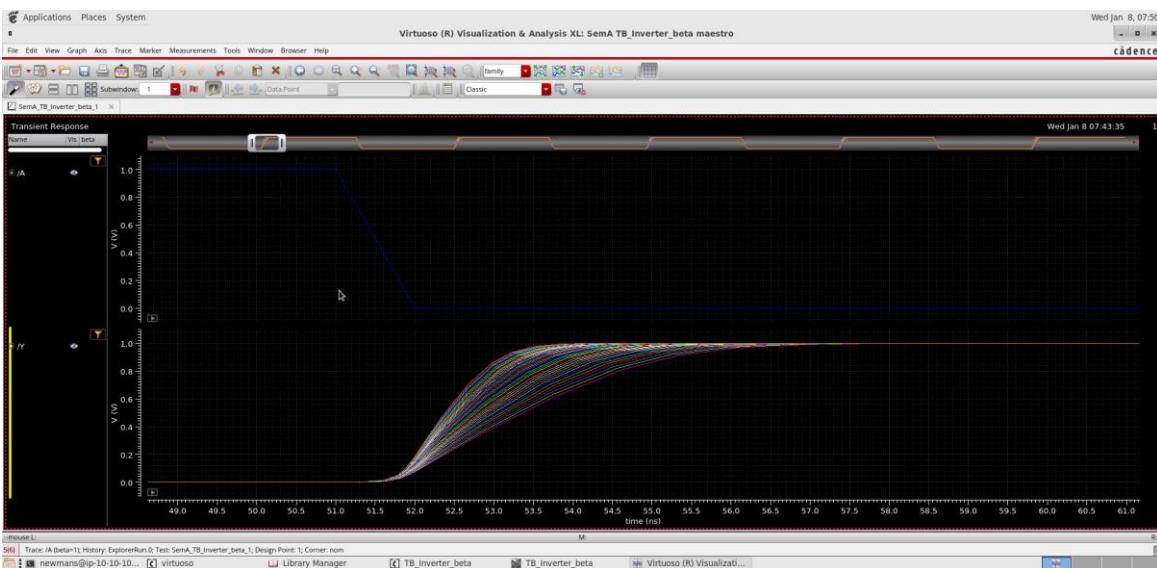


Image 6 – Transient Simulation Zoom-In

From a close up of the graph we can see how the Rise time of the output changes as the beta changes.

One method to find the optimum beta is to graph rise and fall times by a function of beta and observe where they intersect. That point will give us the beta.

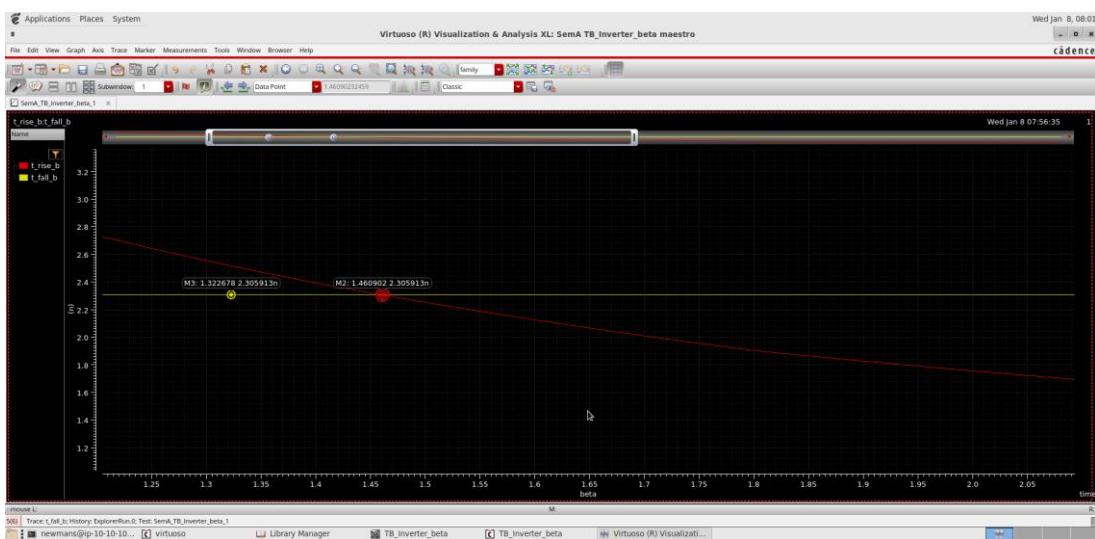


Image 7 - Transient Simulation Trise and Tfall

From this graph we can see that $trise$ and $tfall$ will be equal when **$\betaeta = 1.46$** .

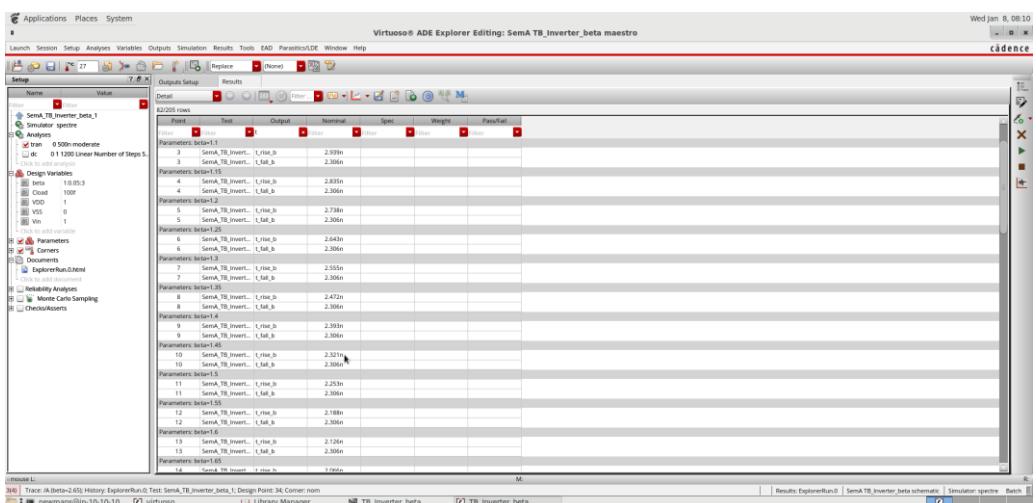


Image 8 – Inverter Transient Simulation Results

Following the Transient Analysis DC Analysis was done on the DC operating points of the circuit. The design variable was Vin and was swept over a range from 0 to 1 with 1200 steps.

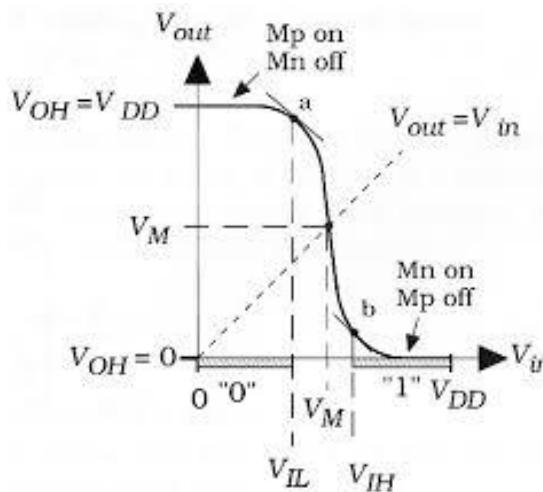


Image 9 – Inverter VTC (Voltage Transfer Curve) Graph

Many of the parameters used in the DC analysis will be explained in part B of this question.

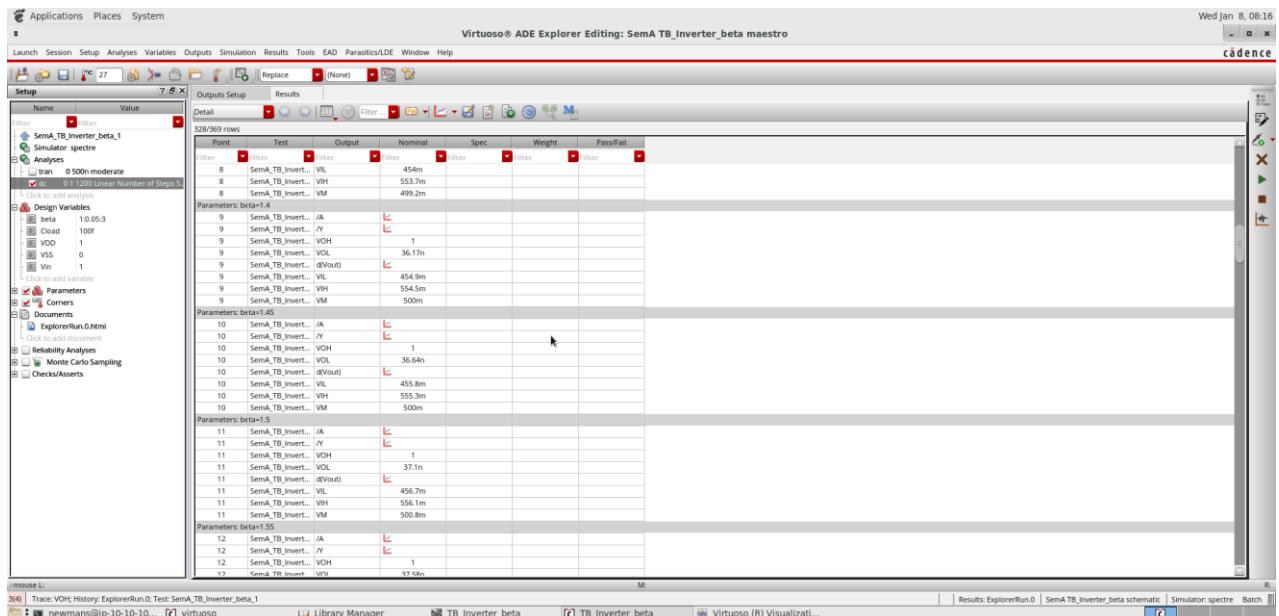


Image 10 – Inverter DC Simulation Results

Another method to find the beta is measuring which beta will give us a V_M of exactly have VDD (500mV). V_M can be found as the x-min of the derivative of $Vout - d(Vout)$.

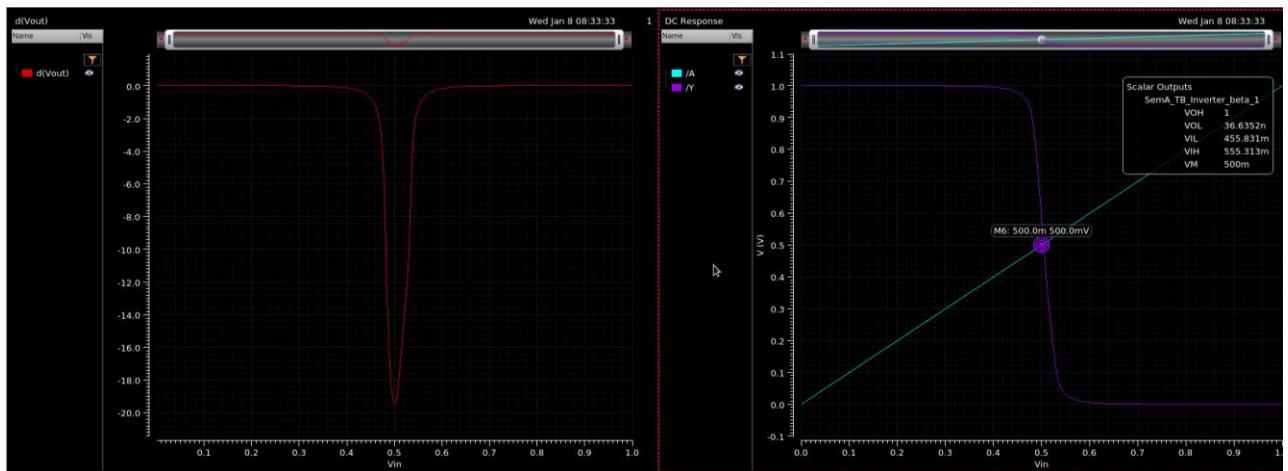


Image 11 – DC Analysis Simulation Graphs

The left graph represents the simulation of $d(V_{out})$. At its minimum the VM can be found. The graph on the right represents the VTC curve. The VM can also be seen at this point being in the middle of the curve, and is at a linear line from the origin.

The point that gives a $VM = \frac{V_{DD}}{2} = 500mV$ will give the value for the correct beta for symmetry.

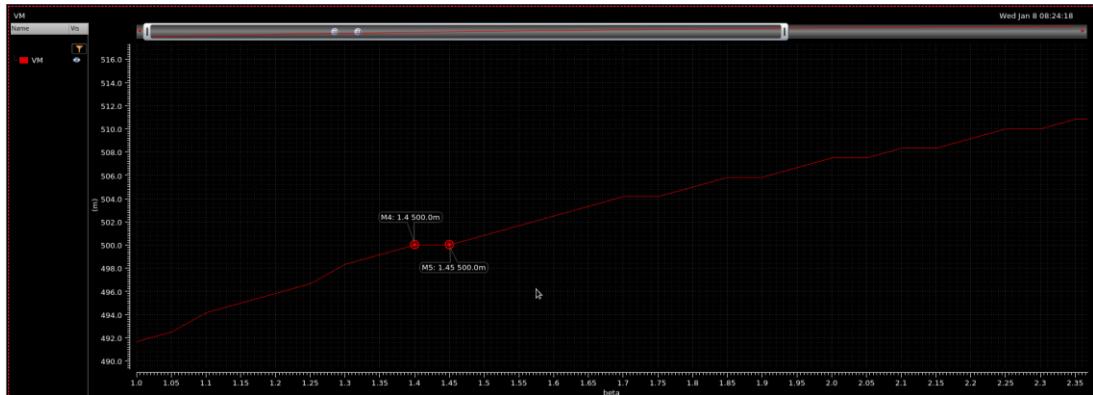


Image 12 - VM /beta graph

Using the graph VM to beta, it can be seen as the $VM = \frac{V_{DD}}{2} = 500mV$ that beta is $1.4 \rightarrow 1.45$.

Going forward we will define 1.45 as our *optimal beta*.

$$\beta_{opt} = 1.45$$

To test that this is the correct beta, T_{rise} and T_{fall} were measured at our β_{opt} .

Name	Type	Details	Value	Plot	Save	Spec
	signal	/A		<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	
	signal	/Y		<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	
t_rise_b	expr	riseTime(VT("Y") 0 nil 1 nil 10 90 nil "time")	2.321n	<input checked="" type="checkbox"/>	<input type="checkbox"/>	
t_fall_b	expr	fallTime(VT("Y") 1 nil 0 nil 90 10 nil "time")	2.321n	<input checked="" type="checkbox"/>	<input type="checkbox"/>	
VOH	expr	ymax(VS("Y"))		<input type="checkbox"/>	<input type="checkbox"/>	
VOL	expr	ymin(VS("Y"))		<input type="checkbox"/>	<input type="checkbox"/>	
d(Vout)	expr	deriv(v("Y" ?result "dc"))		<input type="checkbox"/>	<input type="checkbox"/>	
	expr			<input type="checkbox"/>	<input type="checkbox"/>	
VIL	expr	cross(deriv(v("Y" ?result "dc")) -1 1 "falling" nil nil nil)		<input type="checkbox"/>	<input type="checkbox"/>	
VIH	expr	cross(deriv(v("Y" ?result "dc")) -1 1 "rising" nil nil nil)		<input type="checkbox"/>	<input type="checkbox"/>	
VM	expr	xmin(deriv(v("Y" ?result "dc")) 1)		<input type="checkbox"/>	<input type="checkbox"/>	
TP_LH	expr	riseTime(VT("Y") 0 nil 1 nil 0 50 nil "time")		<input type="checkbox"/>	<input type="checkbox"/>	
TP_HL	expr	fallTime(VT("Y") 1 nil 0 nil 100 50 nil "time")		<input type="checkbox"/>	<input type="checkbox"/>	

Image 13 – Equal rise and fall times

Using our optimal Beta it can be seen that T_{rise} and T_{fall} times are equal. This beta will be used going forward for our inverter.

B. Measurements

The following DC parameters will be measured using our inverter with our $\beta_{opt} = 1.45$

V_{OH} , V_{OL} , V_{IH} , V_{IL} , V_M .

V_{OH} = max output voltage when out logic High (1). Ideally VDD . This can be found by finding the y_{max} of the VTC curve.

V_{OL} = the min output voltage when the inverter is logic Low (0). This can be found by finding the y_{min} of the VTC curve.

V_{IH} = the min input voltage to be considered High(1). This is found when the VTC slope is -1 (falling).

V_{IL} = The max input voltage to be considered Low(0). This is found where the VTC slope is -1 (rising)

V_M = the switching Thereshold Voltage. This is where $Vin = Vout$.

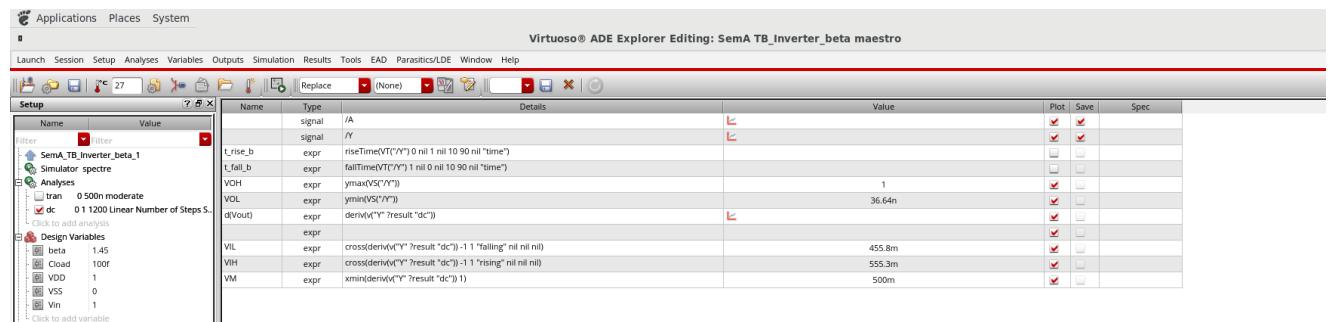


Image 14 – DC Measurements

The following Transient Parameters were measured using our inverter with our optimal beta;

T_{PH} , T_{PLH} , T_{PD} , T_{rise} , T_{fall} .

The following image explains how each time/delay was measured:

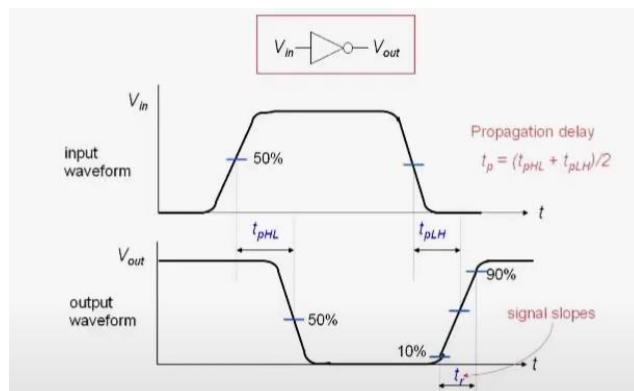


Image 15 - Calculating T_{PHL} , T_{PLH} , TPD

Name	Type	Details	Value	Plot	Save
	signal	/A		<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
	signal	/Y		<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
t_rise_b	expr	riseTime(VT("Y") 0 nil 1 nil 10 90 nil "time")	2.321n	<input checked="" type="checkbox"/>	<input type="checkbox"/>
t_fall_b	expr	fallTime(VT("Y") 1 nil 0 nil 90 10 nil "time")	2.321n	<input checked="" type="checkbox"/>	<input type="checkbox"/>
V0H	expr	ymax(VS("Y"))		<input type="checkbox"/>	<input type="checkbox"/>
V0L	expr	ymin(VS("Y"))		<input type="checkbox"/>	<input type="checkbox"/>
d(Vout)	expr	deriv(v("Y" ?result "dc"))		<input type="checkbox"/>	<input type="checkbox"/>
VIL	expr	cross(deriv(v("Y" ?result "dc"))-1 1 "falling" nil nil nil)		<input type="checkbox"/>	<input type="checkbox"/>
VIH	expr	cross(deriv(v("Y" ?result "dc"))-1 1 "rising" nil nil nil)		<input type="checkbox"/>	<input type="checkbox"/>
VM	expr	xmin(deriv(v("Y" ?result "dc")))		<input type="checkbox"/>	<input type="checkbox"/>
tpHL	expr	delay(?wf1 VT("A") ?value1 0.5 ?edge1 "rising" ?nth1 1 ?td1 0.0 ?tol1 nil ?wf2 VT("Y") ?value2 0.5 ...	1.435n	<input checked="" type="checkbox"/>	<input type="checkbox"/>
tpLH	expr	delay(?wf1 VT("A") ?value1 0.5 ?edge1 "falling" ?nth1 1 ?td1 0.0 ?tol1 nil ?wf2 VT("Y") ?value2 0.5...	1.419n	<input checked="" type="checkbox"/>	<input type="checkbox"/>
tpD	expr	((tpLH + tpHL) / 2)	1.427n	<input checked="" type="checkbox"/>	<input type="checkbox"/>

Image 16 – Transient Time Measurements

Trise and Tfall are the same which was expected. TPLH and TPDLH are also very close which is expected in the symmetrical Inverter.

Next *Cload* is changed until the value for a TPD with a 10% value increase is received.

$$TPD = 1.427\text{ns}$$

$$(1.1) \times TPD = 1.5697\text{ ns}$$

Different values of *Cload* were evaluated using sweep from 100f to 120f with steps of 1f.

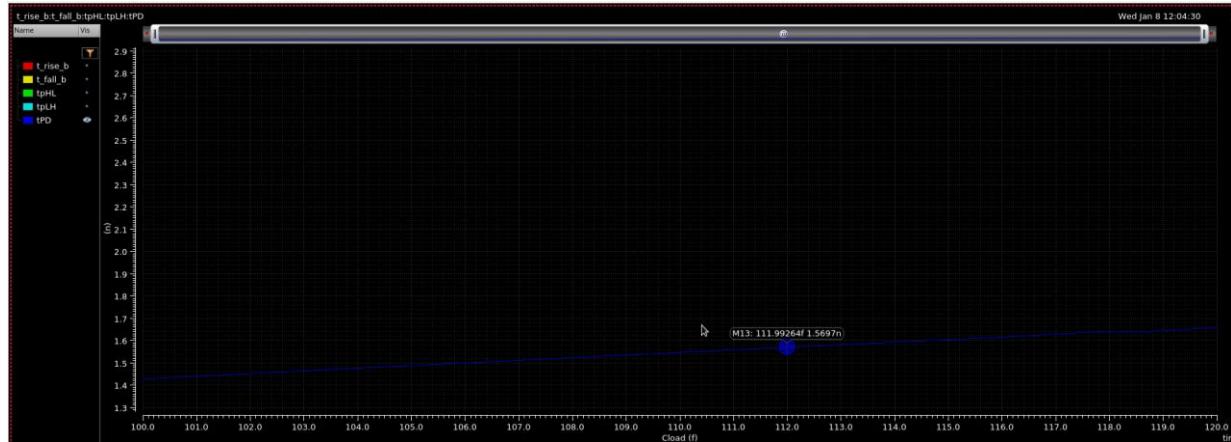


Image 17 – TPD (*Cload*) Graph

The propagation delay (TPD) grows by 10% when *Cload* = 111.99264 fF.

The propagation delay of a CMOS inverter is the time it takes for the output to transition after an input change. The delay depends on the time required to charge and discharge the load capacitance (*Cload*) through the MOSFETs. Therefore, by changing the load capacitance, the propagation delay will also be changed since it will take more time to charge/discharge.

C. Layout

The schematic of the inverter was updated to be: $W_p = 120 \text{ [nm]} \times \beta = 120n \times 1.45 = 174 \text{ [nm]}$.

The schematic automatically updated it to $W_p = 175 \text{ nm}$.

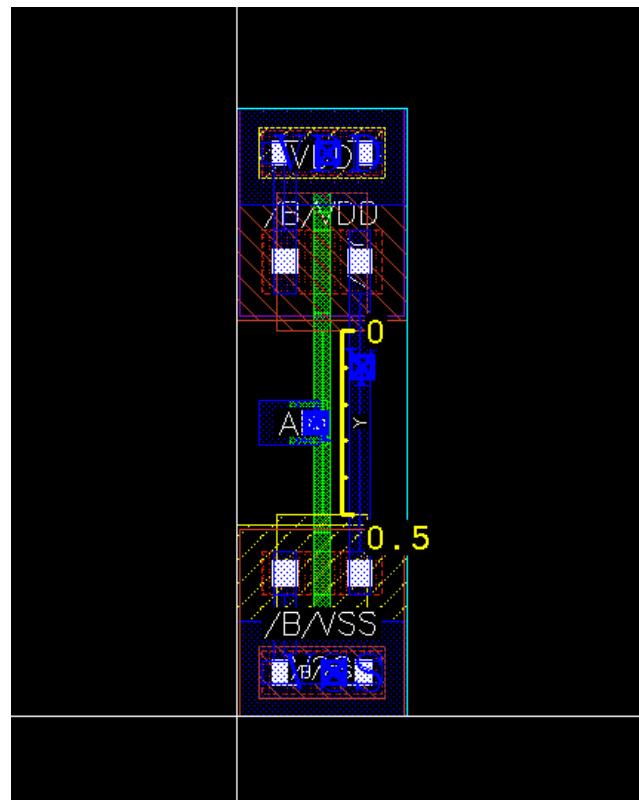


Image 18 - Inverter Layout

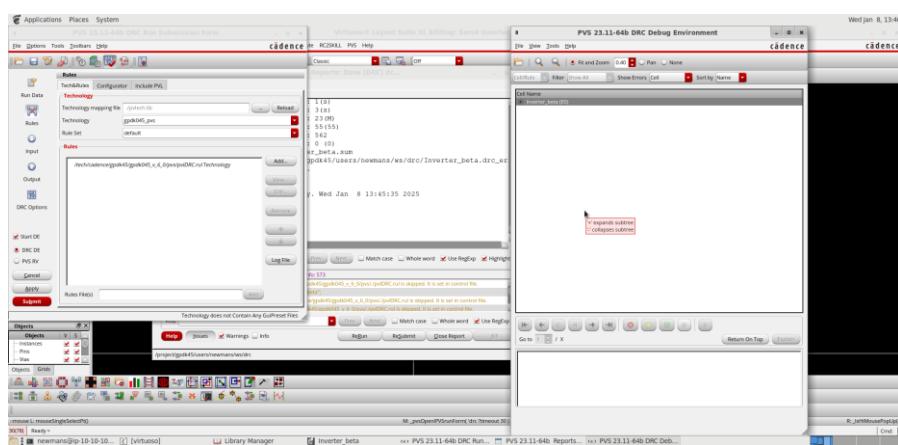


Image 19 - Inverter DRC Check

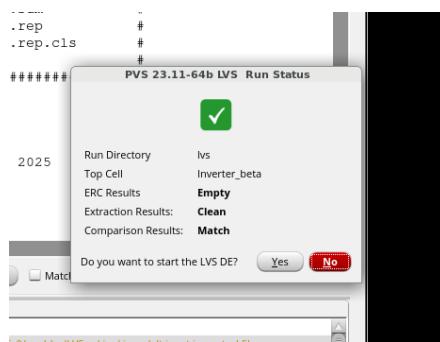


Image 20 - Inverter LVS Check

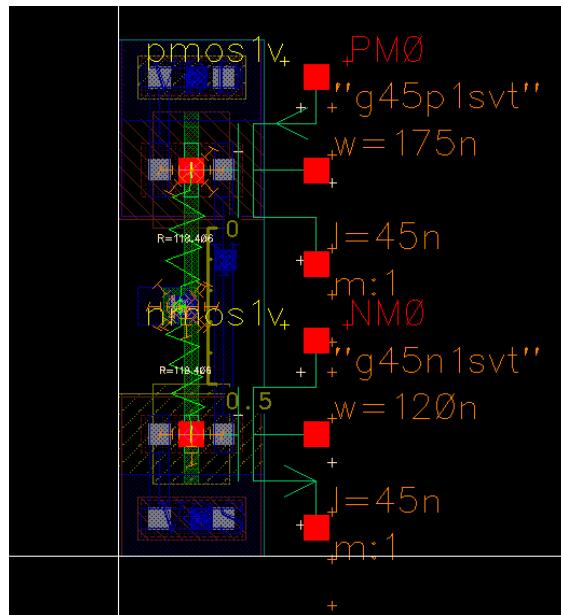


Image 21 - Inverter Layout with Parasitic

After the Patristics were added to the layout, the simulations were run again with the effect of the parasitics.

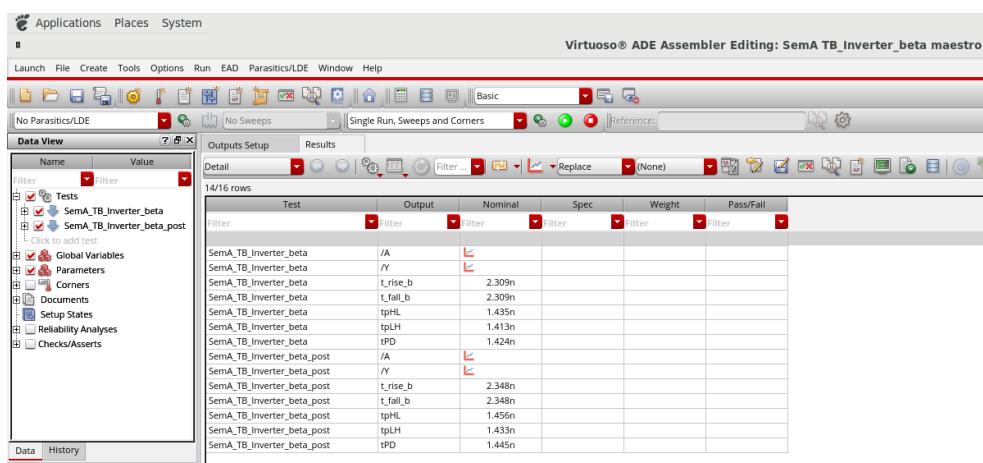


Image 22 - Post Parasitic Transient

T_{pd} (Propagation Delay): Increases significantly

- Delay is dominated by parasitic capacitance (*Cload*)
- $T_{pd} \approx 0.69ReqCload$
- Higher *Cload* → longer charging/discharging time → increased delay.

T_{rise} (Rise Time): Increases

- PMOS has higher resistance than NMOS → *trise* is already slower.
- Parasitic capacitance at the output further slows the charging of *Cload*

T_{fall} (Fall Time): Increases

- NMOS discharge is affected by drain-to-bulk capacitance and wire capacitance.
- If NMOS resistance increases (due to layout or process), *t_{fall}* gets worse.

Result: Slower switching → increased power dissipation and reduced operating speed.

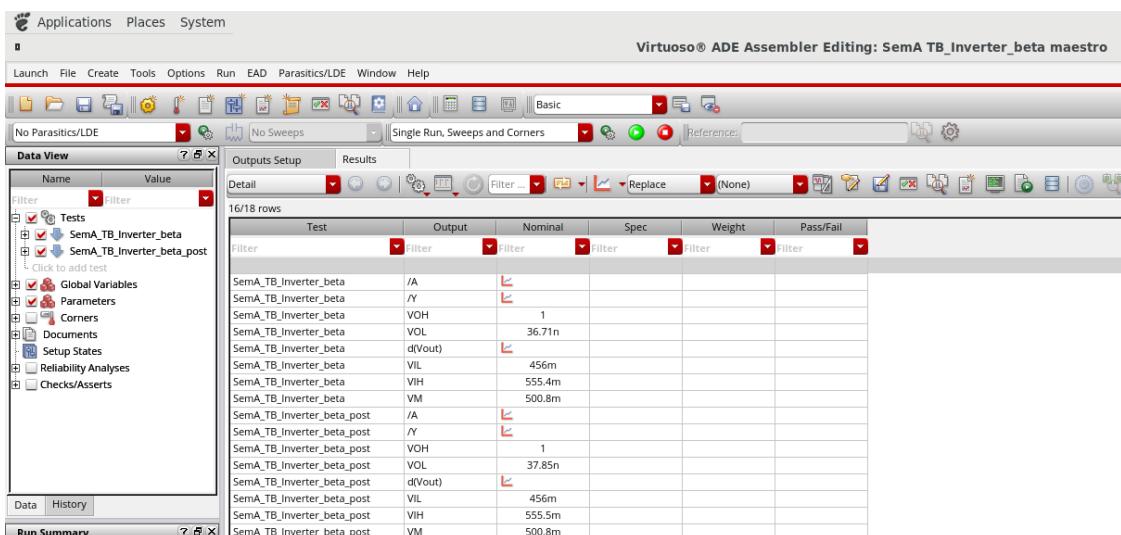


Image 23- Post Parasitic DC Analysis

VOH: Decreases slightly

- Ideally, $VOH = VDD$, but due to parasitic resistance (R_p) in the PMOS other connections, a small voltage drop occurs.
- $VOH \approx VDD - I_{load}R_p$

VOH: Increases slightly

- Ideally, $VOL = 0V$, but parasitic resistance (R_n) in the NMOS and interconnects causes a small voltage rise.

- $V_{OL} \approx I_{load}R_n$

VM:

- Parasitics affect rise/fall asymmetry, shifting VM_V , MVM toward NMOS or PMOS dominance.

VIH: Decreases slightly

- With parasitic capacitances, PMOS pull-up is slower, requiring a higher V_{in} to switch.

VIL: Decreases slightly

- NMOS pull-down is slowed by parasitic capacitance, requiring a lower V_{in} to switch.

Result: Noise margins(NMH , NML) shrink, making the inverter more sensitive to noise.

Question 2 – D Flip-Flop

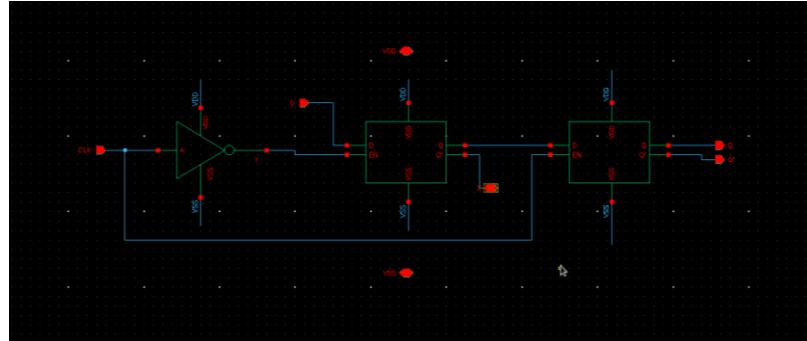


Image 24 - Schematic DFF

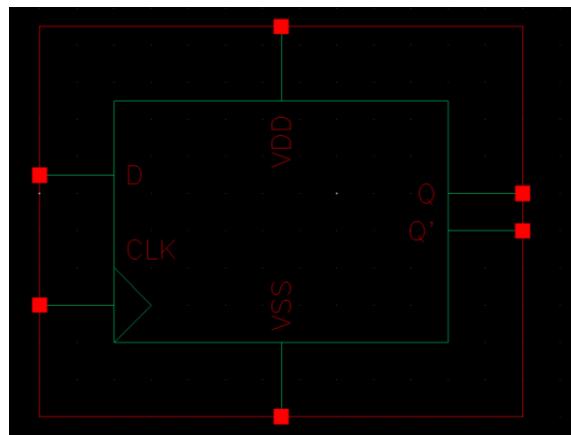


Image 25 – DFF Symbol

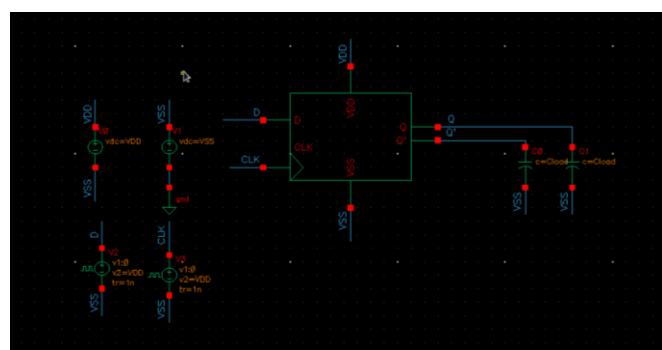


Image 26 - Test Bench Schematic

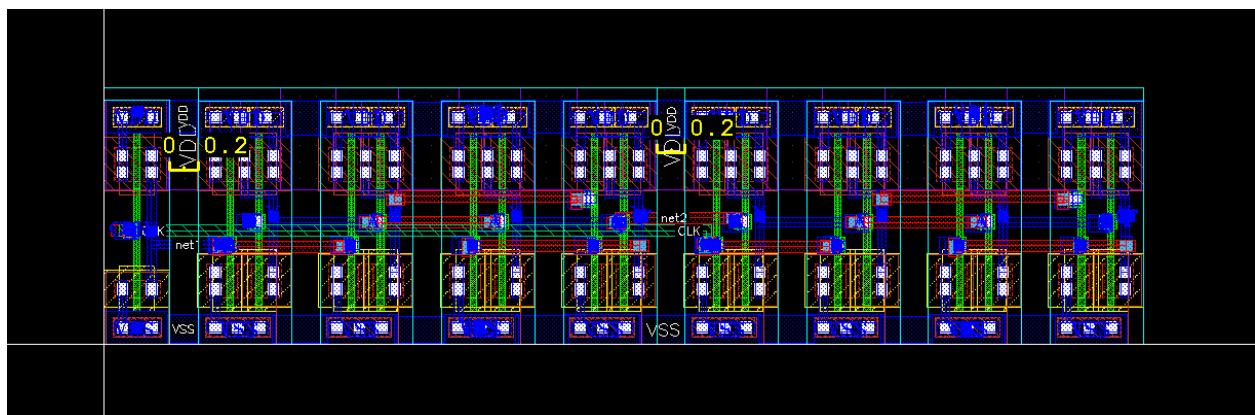


Image 27 - Layout DFF

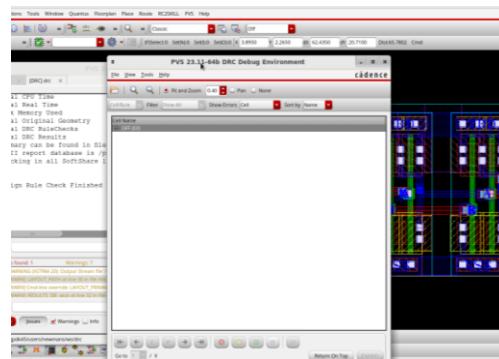


Image 28 – DRC check

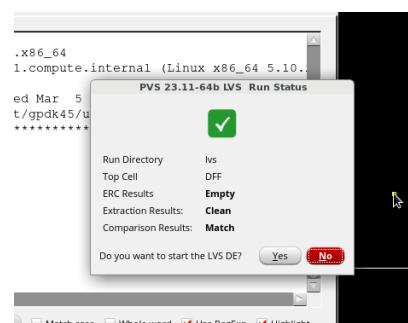


Image 29 – LVS check

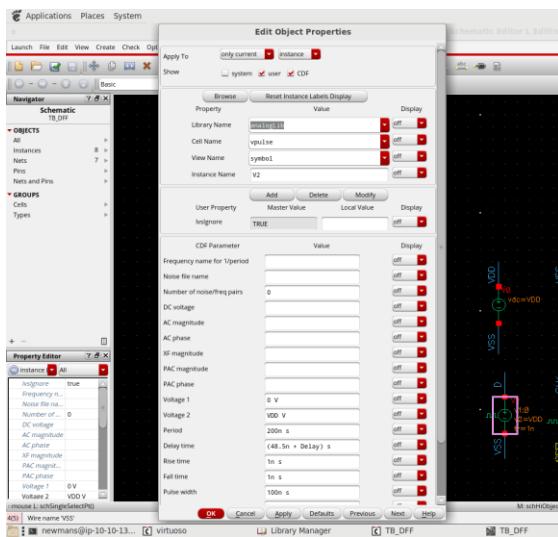


Image 30– Pulse Delay Variable

A test was done to the DFF to show it functions correctly.

$Cload = 12fF$. This corresponds with the last digits of the T.Z (342785912).

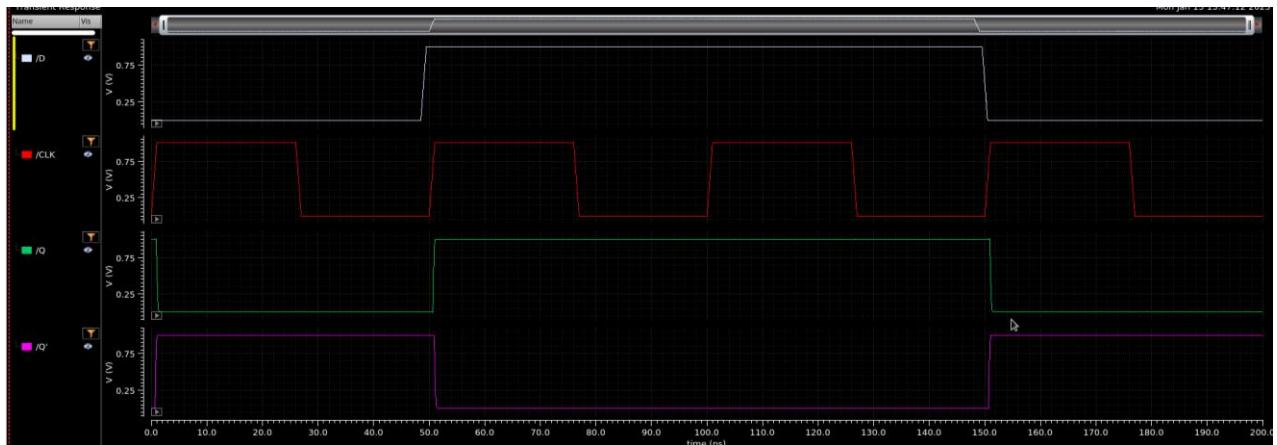


Image 31 - DFF Test Simulation of 200 ns

The simulation shows the correct function of the D-FF. When Data is high and there is a rising edge of CLK single, the output, Q is high. Q remains high until the rising edge of the CLK signal when D is low. Q' is the opposite output of Q.

As a background to the 3 important times of the D-FF see the image below. It shows the D-FF with a changing Delay time in the Data signal.

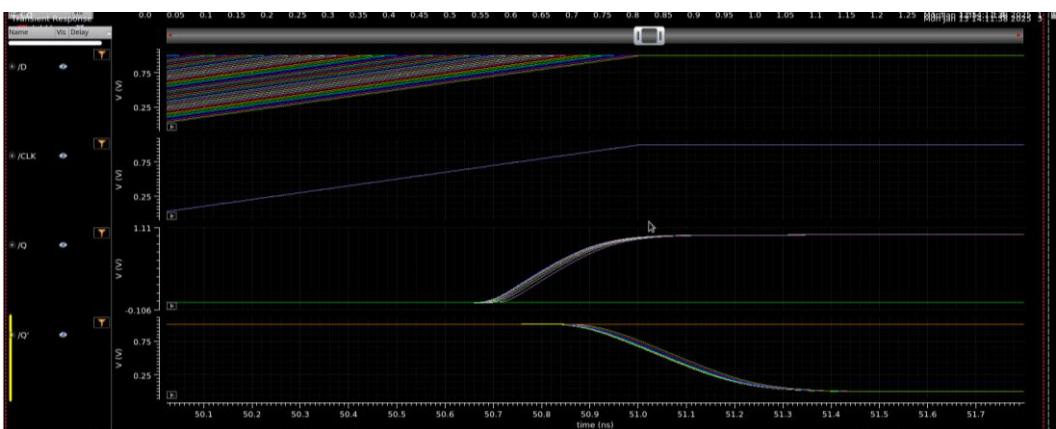


Image 32 – D-FF Delay Variable Simulation

Not every trace can make it high for Q. This is due to some of the issues discussed next. As the incoming Data signal timing changes, the system is able to produce it in the output and sometimes it is not.

There are 3 important times to pay attention to with a D-FF:

T_{CQ} : The time from which the clk rises 50% VDD until the output, Q, reaches the same value 50% VDD (When CLK reaches 50% how long will it then take for Q to reach 50%).

T_{Setup} : How long the information of D (Data) needs to be “ready” before the CLK signal comes. The Data needs to be active or ‘ready’ a certain amount of time prior to the CLK signal, they cannot rise at the same time. If they rise at the same time, or without the D being ‘ready’ then Q will not receive anything. If there are many DFF cascaded and T_{Setup} is incorrect then the system will not work.

T_{Hold} : The minimum time that the data input (D) must remain stable after the clock edge to ensure that the flip-flop correctly latches the data to the output.

$T_{Data to Clock}$: It represents the time difference between when D (data) arrives and the clock edge occurs.

If the system does not meet the required T_{Hold} or T_{Setup} then it may cause issues in the output of the system, as seen in the simulation above.

Using maestro these different times will be measured.

The Delay time of the $Vpulse$ of the test Bench Schematic is set to $Delay\ Time = 48.5n + Delay$.

Delay is defined as a variable which will be defined in the maestro.

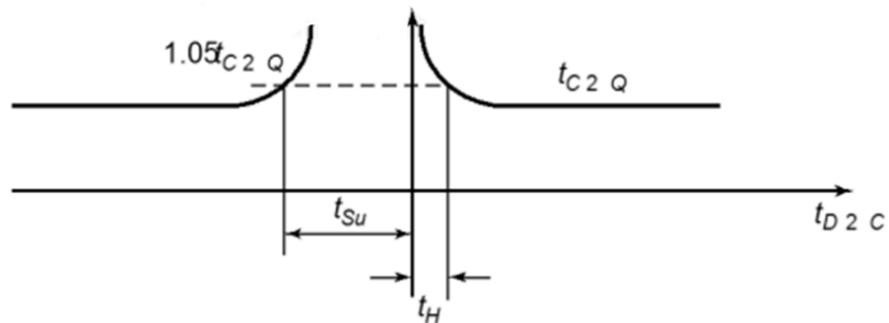


Image 33 - Tsetup, Thold diagram

Measure TCQ:

Use delay function between 2 points. Signal1 = CLK, Signal2=Q, Threshold 1 = Threshold 2 = 0.5, both on the rising edge.

Measure Tsetup

$T_{data_to_clock}$ and TCQ calculations were measured in maestro below:

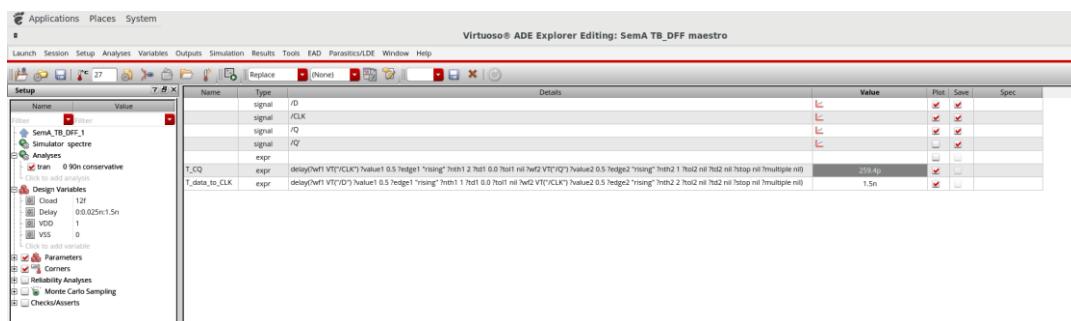


Image 34 - Tsetup, TCQ calculations Maestro

To measure Tsetup, the Delay variable was run from 0 to 1.5ns.

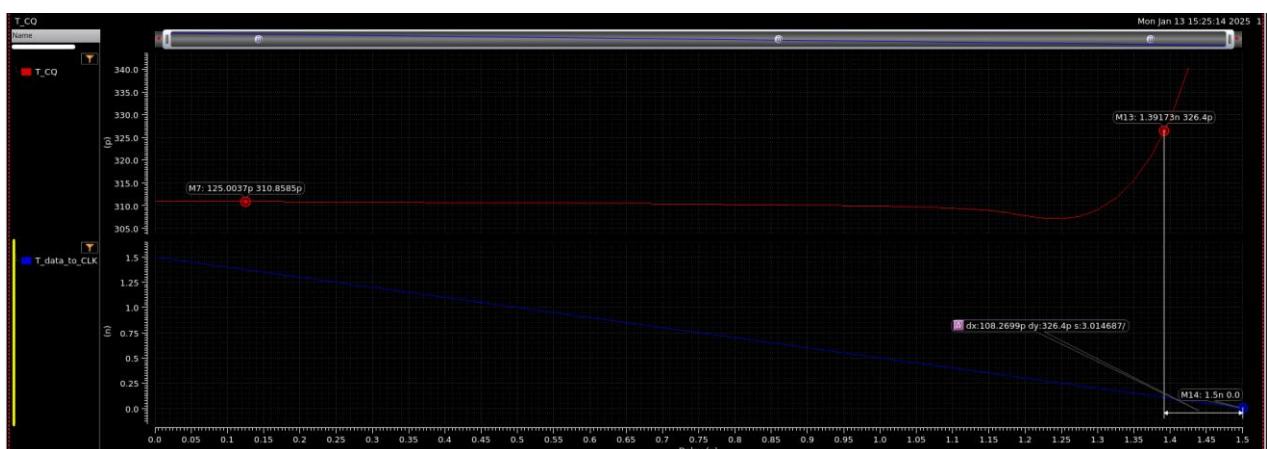


Image 35 - Finding Tsetup as dx

The delay time variable of the system was swept over a range of values. After, simulated the graphs of the TCQ and $T_{data_to_clock}$ were compared in the same graph as a function of the variable delay. The Image above was used as reference. Using a marker, a stable TCQ value was measured $TCQ = 310.8585\text{ps}$. The T_{setup} starts when TCQ rises 5%. After calculation this value to be 326.4ps , this value was marked on the simulation. The T_{setup} value is measured as the Δx (or dx) between $+5\%TCQ$ and the origin of $T_{data_to_clock}$. This origin $(0,0)$ is when $Delay = 1.5n$ is all the way to the right. Past this point TCQ becomes infinite. There is no output value (Q) at this point (eval error) since there was not enough time before the CLK signal that the Data was active high. dx is measured at:

$$T_{setup} = dx = 108.27\text{ps}.$$

The variable Delay is 1.5ns at this point which means are total Delay time is: $Delay = 58.5n + 1.5n = 60\text{ns}$.

Measure Thold:

To find $THold$, The Delay time of the Data pulse was changed to $Delay Time = 50n + Delay$ and $Pulse Width = PW$, also a variable.

Delay was set to 0. The PW variable was swept through initial values to see which values allowed Data to pass to the Output. One an initial range was found; there PW was swept over a smaller range with smaller jumps between values. PW was swept from $0.4n$ to $0.5n$ with jumps of $0.0001n$.

*With permission from the teacher, $Cload$ was made half its current value to $6ff$.

The various times can be seen in the following diagram:

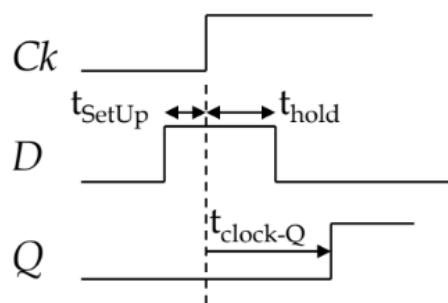


Image 40 – D Flip-Flop Times

To do this, the Pulse Width of the clock was swept through various values. Using the simulation output, the time when the Q was no longer stable was found.

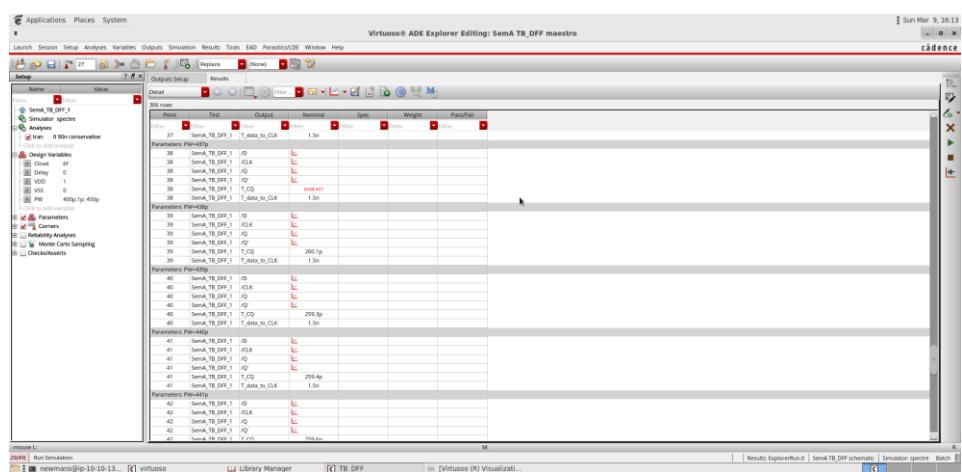


Image 41 – PW Time

Pulse width that is long enough for Q to receive the data from D: PW=438ps. With that band width, a simulation was run. It was evaluated to check how long Data stays stable (falling edge 50%) from the Clock signal rising edge (50%).

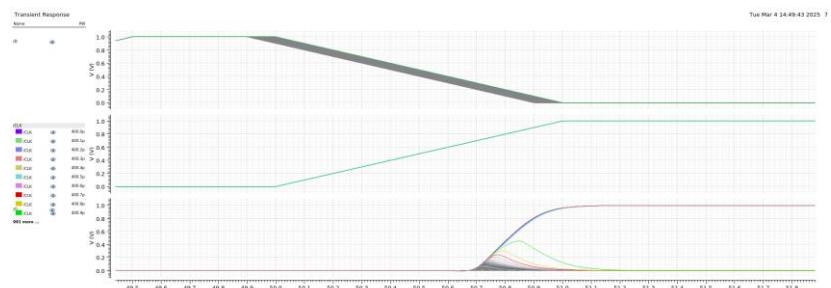


Image 42 – D-FF simulation with different PW values

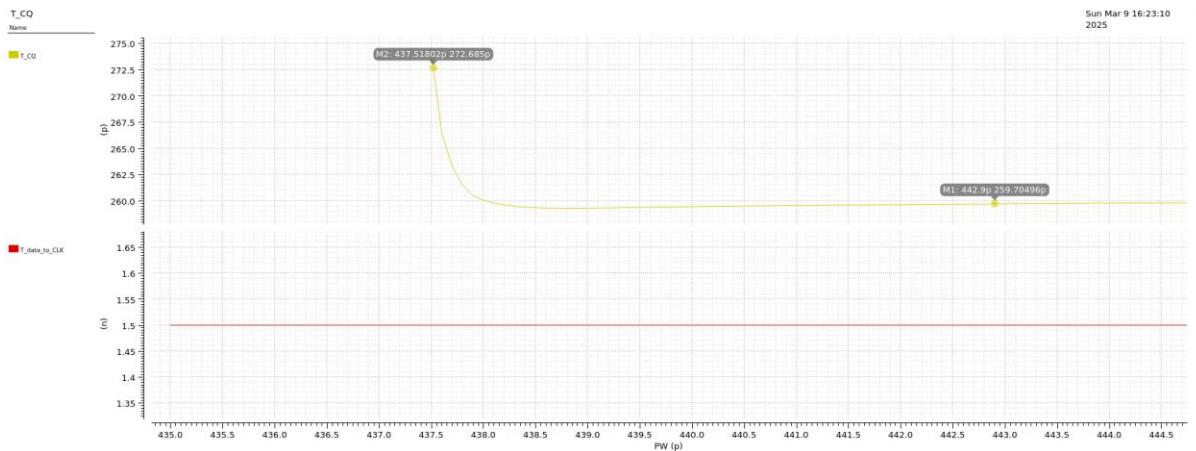


Image 43 – TCQ and Tdata – to_Clock Graph

This graph shows the spike of TCQ when the Flip-Flop becomes stable again. The stable TCQ is at 259.7ps. TCQ+5% is at 272.685ps. Both these values are marked on the graph.

Using the simulation the Thold was measured.

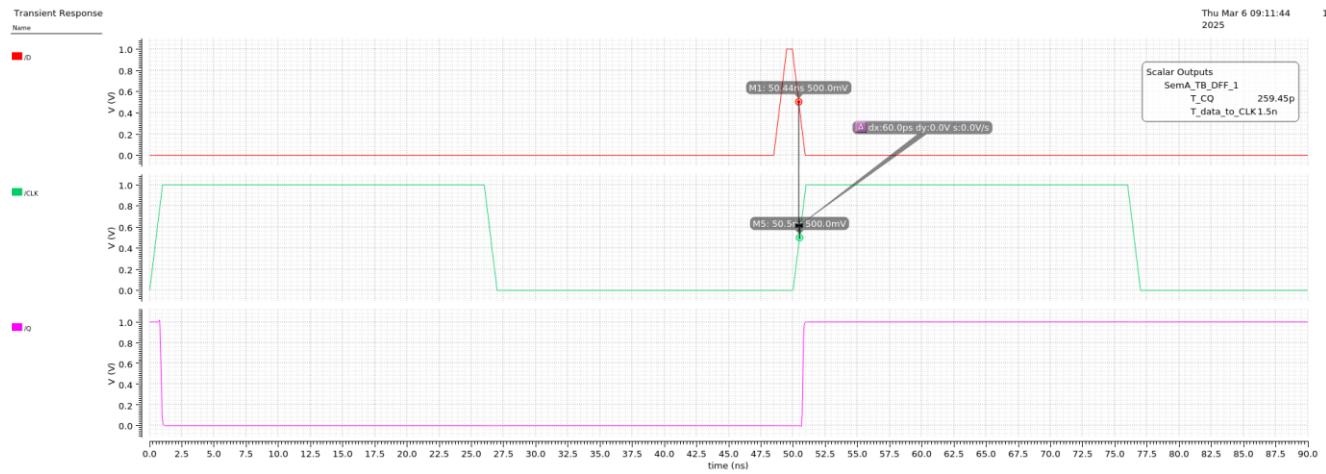


Image 44– Thold

The first point is the last moment when D is stable. The second point is when the clock rising edge happens. Both are at 50% value of the pulse. These two points were marked and the distance between them measured. The time, which can be taken as the Thold is:

Thold = 60ps.

Question 3 – Ring Oscillator

For this question, a Ring Oscillator was built by chaining 3 (an odd number) inverters together in series, with the last one chained to the first. These are the same Symmetric Inverters as were built in question 1.

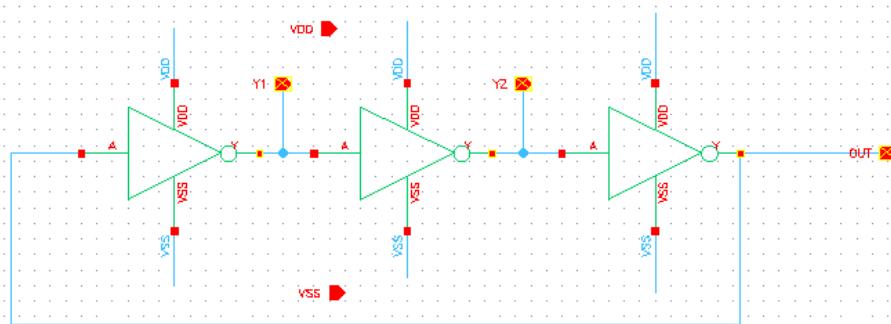


Image 44 – RO Schematic

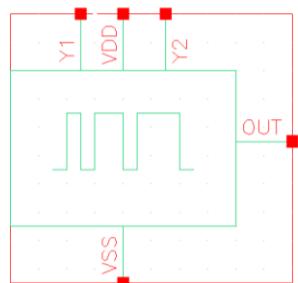


Image 45 – RO Symbol

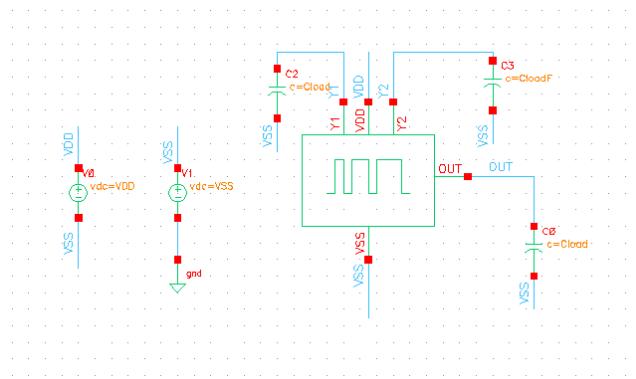


Image 46 – RO TB Schematic

Using the TZ: 324785912:

$$L1 = 1\mu m$$

$$L2 = 10\mu m$$

$$L3 = L1 + L2 \approx 11\mu m$$

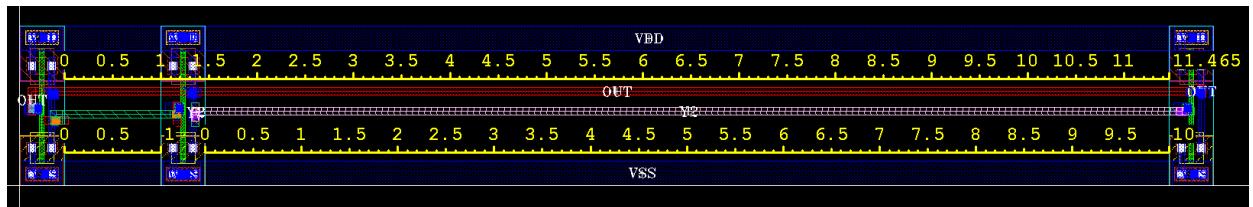


Image 47 – Layout Ring Oscillator

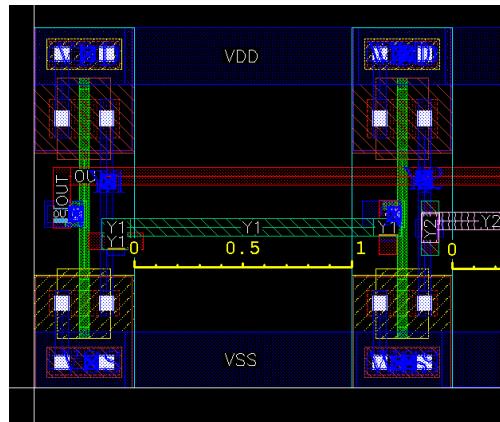


Image 48 – Cell 1 and 2

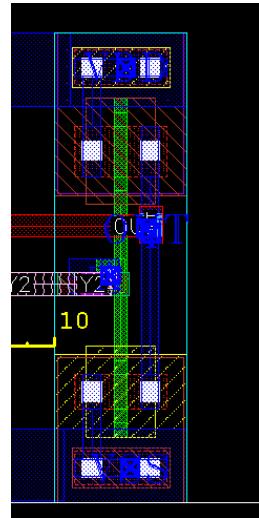


Image 49 – Cell 3

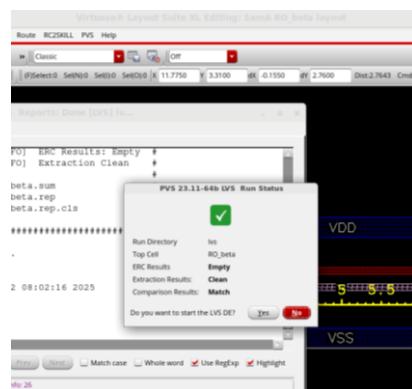


Image 50 – LVS Check RO

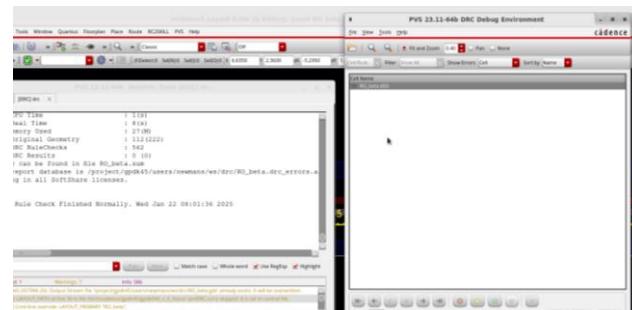


Image 51 – DRC Check RO

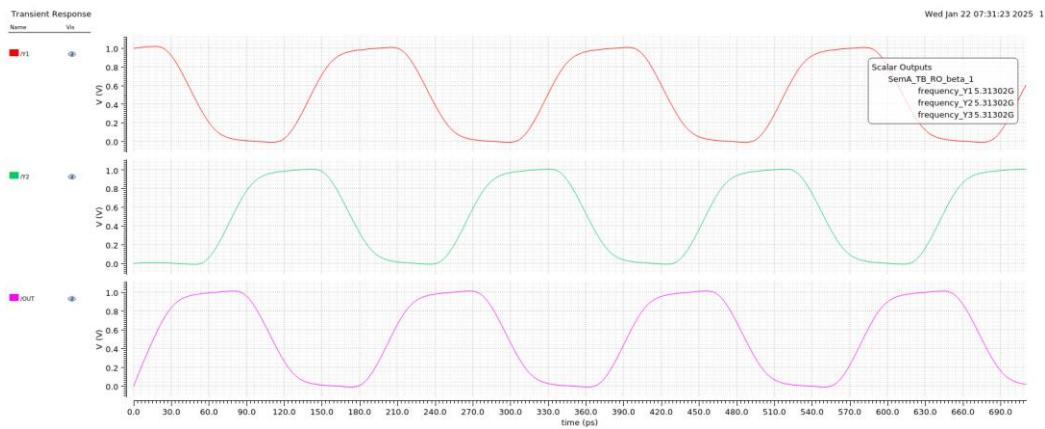


Image 52 – RO Frequencies

Example for calculating TPD Used the following picture. Needed to take edges that were very far along when the RO is stable (took, 101, 102).

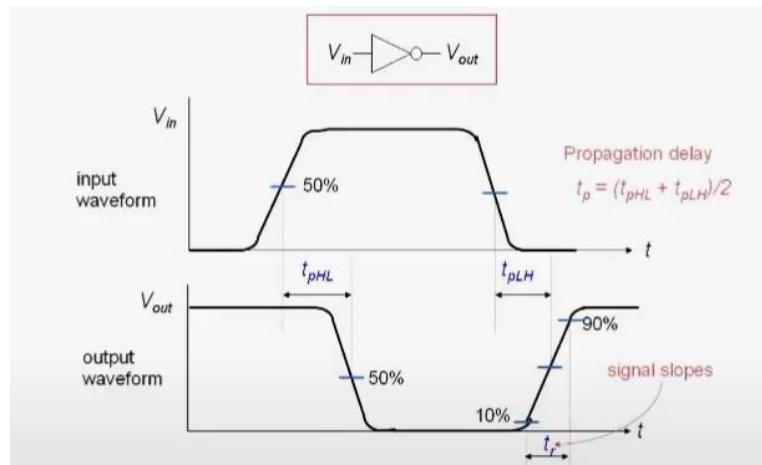


Image 53 – TPD Calculations

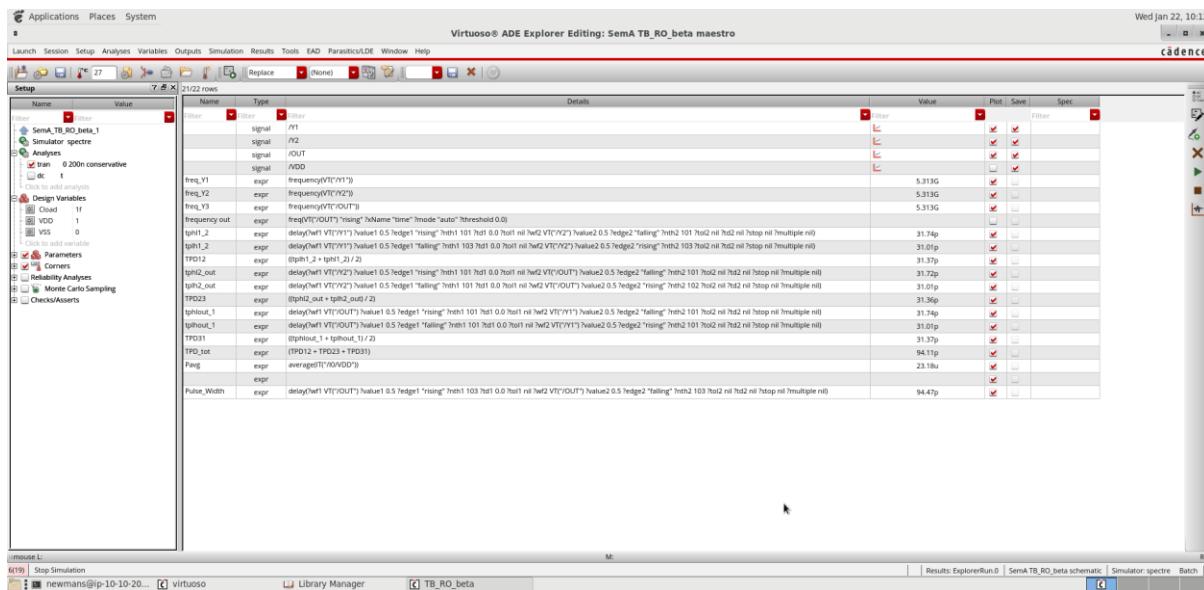


Image 54 – Calculations RO

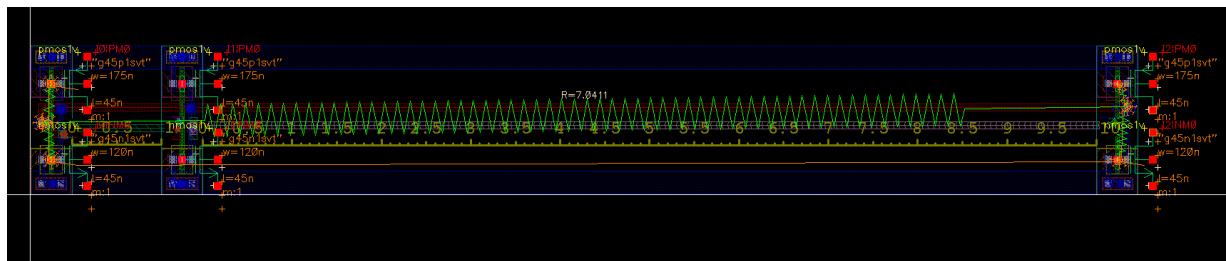


Image 55 – Layout Post Patriстиcs

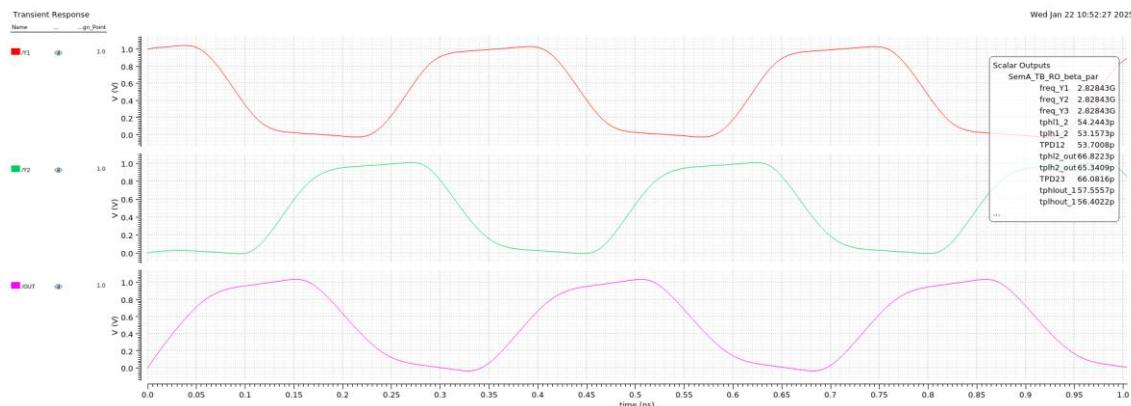


Image 56 - Sim without Patriстиcs

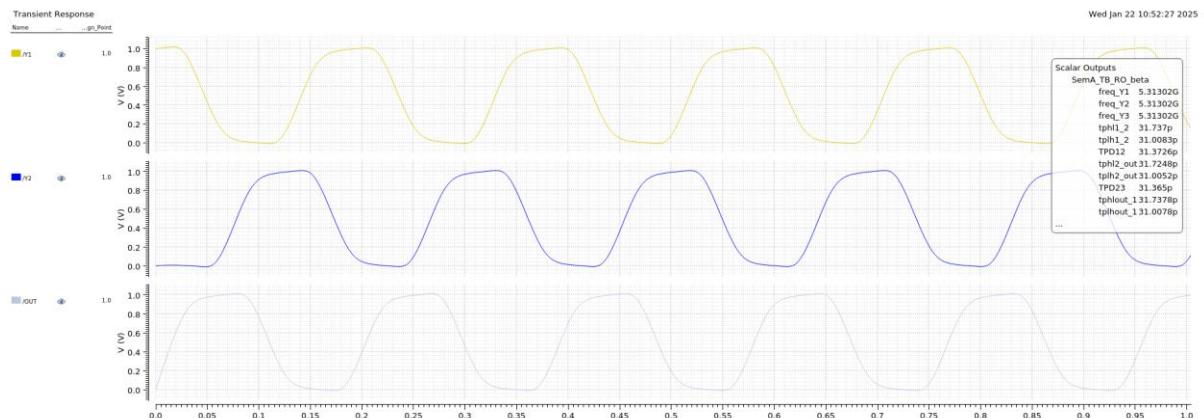


Image 57 - Sim with Patristics

B. Corners:

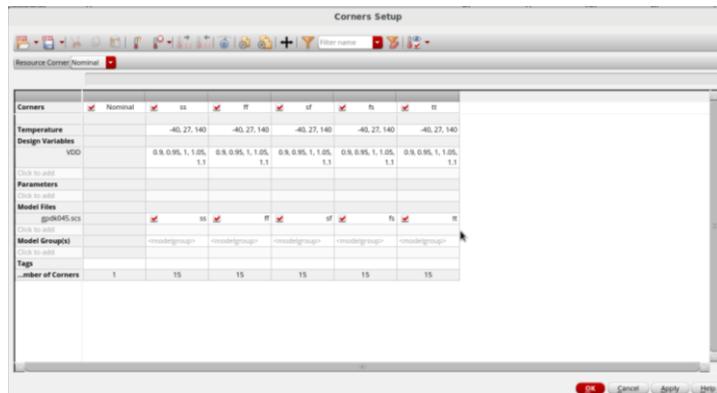


Image 58 – Defining Corners on Maestro

Parameter	Nominal							ss_0							ss_1							ss_2							ss_3							
	VDD	1	900m	900m	900m	950m	950m	950m	950m	950m	950m	950m	950m	950m	950m	950m	950m	950m	950m	950m	950m	950m	950m	950m	950m	950m	950m									
gdk045.scs	tt		ss	ss	ss	ss	ss	ss	ss	ss	ss	ss	ss	ss	ss	ss	ss	ss	ss	ss	ss	ss	ss	ss	ss	ss	ss	ss	ss	ss	ss	ss				
temperature	27		-40	27	140	-40	27	140	-40	27	140	-40	27	140	-40	27	140	-40	27	140	-40	27	140	-40	27	140	-40	27	140	-40	27	140	-40	27	140	
SemA_TB_RO_beta.par	freq_Y1	2.828G		1.014G	5.646G	1.618G	1.343G	1.014G	2.039G	1.674G	1.239G	2.454G																								
SemA_TB_RO_beta.par	freq_Y2	2.828G		1.014G	5.646G	1.618G	1.343G	1.014G	2.039G	1.674G	1.239G	2.454G																								
SemA_TB_RO_beta.par	freq_X1	2.828G		1.014G	5.646G	1.618G	1.343G	1.014G	2.039G	1.674G	1.239G	2.454G																								
SemA_TB_RO_beta.par	qnt1_1	54.34p		29.85p	125.8p	83.45p	101.5p	125.8p	70.71p	87.14p	119.4p	62.18p																								
SemA_TB_RO_beta.par	tpH1_2	53.16p		24.56p	160.4p	100.9p	121.3p	160.4p	76.17p	92.24p	124p	60.3p																								
SemA_TB_RO_beta.par	TPD12	53.7p		27.21p	148.2p	92.15p	111.4p	148.2p	73.44p	89.61p	121.7p	61.24p																								
SemA_TB_RO_beta.par	tpH2_out	66.42p		36.43p	168.2p	104.6p	126.6p	168.2p	88.26p	108.2p	147.2p	77.32p																								
SemA_TB_RO_beta.par	tpH2_out	65.34p		35.34p	170.8p	124.8p	140.9p	170.8p	94.12p	114.4p	157.2p	74.74p																								
SemA_TB_RO_beta.par	TPD23	65.8p		33.39p	185.1p	114.7p	138.3p	185.1p	91.29p	111.1p	150.3p	70.7p																								
SemA_TB_RO_beta.par	tpHout_1	57.56p		31.21p	144.2p	91.1p	109.5p	144.2p	76.95p	93.71p	126.2p	67.39p																								
SemA_TB_RO_beta.par	tpHout_1	56.4p		24.72p	179.7p	113p	135.1p	179.7p	84.01p	102.1p	137.1p	65.49p																								
SemA_TB_RO_beta.par	TPD31	56.98p		27.96p	161.9p	102.1p	122.8p	161.9p	80.48p	97.88p	131.7p	66.44p																								
SemA_TB_RO_beta.par	TPD_tot	176.8p		88.56p	493.3p	305p	372.4p	493.3p	245.2p	298.7p	403.5p	203.7p																								
SemA_TB_RO_beta.par	Pulse	23.14p		17.15p	50.24p	12.03p	9.967p	17.15p	15.95p	13.08p	9.878p	20.15p																								
SemA_TB_RO_beta.par	Pulse_Width	177.4p		92.21p	47.3p	296.7p	357.4p	473p	241.4p	294.1p	397.4p	207p																								

Image 59 – Corners Results

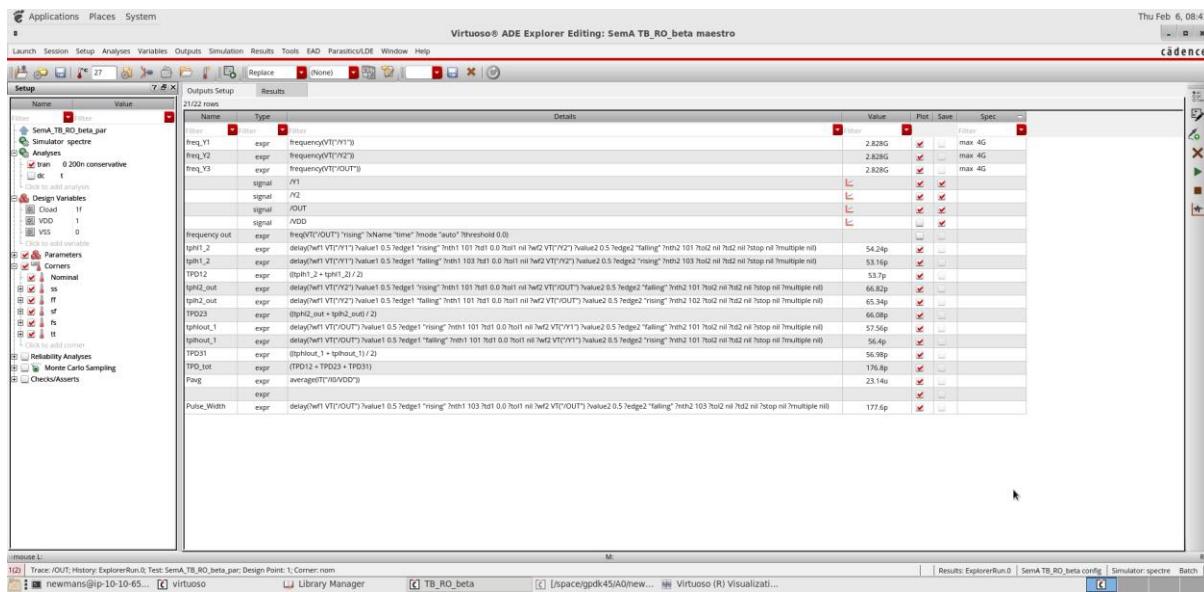


Image 60 – Maestro with Spec fmax = 4 GHz

Table 1 – RO Corners and Spec Results

CORNER	VDD [V]	Temperature[°]	gpdk045.scs	Pass/Fail	Frequency [Hz]	Pavg	TPD [s]	Pulse Width [s]
nom	1	27	tt	pass	2.828G	23.14u	176.8p	177.6p
ff_0	900m	-40	ff	pass	3.725G	27.48u	134.2p	127.5p
ff_1	900m	27	ff	pass	2.933G	21.63u	170.5p	162p
ff_2	900m	140	ff	pass	2.046G	15.09u	244.4p	231.9p
ff_3	950m	-40	ff	near	4.234G	32.85u	118.1p	115.1p
ff_4	950m	27	ff	pass	3.34G	25.92u	149.7p	146.2p
ff_5	950m	140	ff	pass	2.32G	18.02u	215.5p	210.3p
ff_6	1	-40	ff	fail	4.725G	38.45u	105.8p	105.6p
ff_7	1	27	ff	pass	3.737G	30.45u	133.8p	133.9p
ff_8	1	140	ff	pass	2.592G	21.15u	192.9p	193.2p
ff_9	1.05	-40	ff	fail	5.196G	44.25u	96.23p	98.17p
ff_10	1.05	27	ff	near	4.123G	35.17u	121.3p	124.1p
ff_11	1.05	140	ff	pass	2.858G	24.45u	174.9p	179.4p
ff_12	1.1	-40	ff	fail	5.646G	50.24u	88.56p	92.21p
ff_13	1.1	27	ff	fail	4.496G	40.09u	111.2p	116.3p
ff_14	1.1	140	ff	pass	3.119G	27.91u	160.3p	168p
fs_0	900m	-40	fs	pass	2.586G	19.12u	193.3p	181.1p
fs_1	900m	27	fs	pass	2.083G	15.39u	240p	224.5p
fs_2	900m	140	fs	pass	1.506G	11.13u	331.9p	309.1p
fs_3	950m	-40	fs	pass	3.055G	23.75u	163.7p	157p
fs_4	950m	27	fs	pass	2.456G	19.09u	203.6p	195.3p
fs_5	950m	140	fs	pass	1.759G	13.68u	284.2p	272p
fs_6	1	-40	fs	pass	3.51G	28.62u	142.5p	139.7p

fs_7	1	27	fs	pass	2.823G	23.03u	177.1p	173.9p
fs_8	1	140	fs	pass	2.012G	16.43u	248.6p	243.8p
fs_9	1.05	-40	fs	pass	3.947G	33.68u	126.7p	126.8p
fs_10	1.05	27	fs	pass	3.181G	27.17u	157.2p	157.6p
fs_11	1.05	140	fs	pass	2.262G	19.35u	221.1p	221.8p
fs_12	1.1	-40	fs	near	4.368G	38.91u	114.5p	116.8p
fs_13	1.1	27	fs	pass	3.53G	31.49u	141.7p	144.9p
fs_14	1.1	140	fs	pass	2.508G	22.43u	199.3p	204.3p
sf_0	900m	-40	sf	pass	2.441G	18.06u	204.8p	199.8p
sf_1	900m	27	sf	pass	1.96G	14.47u	255.1p	249.1p
sf_2	900m	140	sf	pass	1.414G	10.41u	353.6p	345.5p
sf_3	950m	-40	sf	pass	2.921G	22.75u	171.2p	171.3p
sf_4	950m	27	sf	pass	2.339G	18.19u	213.8p	214.4p
sf_5	950m	140	sf	pass	1.668G	12.95u	299.7p	301p
sf_6	1	-40	sf	pass	3.384G	27.66u	147.8p	151.2p
sf_7	1	27	sf	pass	2.712G	22.14u	184.3p	189.3p
sf_8	1	140	sf	pass	1.923G	15.68u	260p	267.6p
sf_9	1.05	-40	sf	pass	3.828G	32.76u	130.6p	136.4p
sf_10	1.05	27	sf	pass	3.076G	26.3u	162.5p	170.5p
sf_11	1.05	140	sf	pass	2.175G	18.58u	229.9p	242p
sf_12	1.1	-40	sf	near	4.252G	38.02u	117.6p	125.2p
sf_13	1.1	27	sf	pass	3.429G	30.63u	145.8p	156p
sf_14	1.1	140	sf	pass	2.423G	21.64u	206.4p	221.8p
ss_0	900m	-40	ss	pass	1.618G	12.03u	309p	296.7p
ss_1	900m	27	ss	pass	1.343G	9.967u	372.4p	357.4p
ss_2	900m	140	ss	pass	1.014G	7.515u	493.3p	473p
ss_3	950m	-40	ss	pass	2.039G	15.95u	245.2p	241.4p
ss_4	950m	27	ss	pass	1.674G	13.09u	298.7p	294.1p
ss_5	950m	140	ss	pass	1.239G	9.676u	403.5p	397.4p
ss_6	1	-40	ss	pass	2.454G	20.15u	203.7p	205p
ss_7	1	27	ss	pass	2.008G	16.48u	249p	250.9p
ss_8	1	140	ss	pass	1.469G	12.05u	340.4p	343.3p
ss_9	1.05	-40	ss	pass	2.857G	24.56u	175p	179.6p
ss_10	1.05	27	ss	pass	2.338G	20.09u	213.9p	220p
ss_11	1.05	140	ss	pass	1.7G	14.6u	294.1p	303.2p
ss_12	1.1	-40	ss	pass	3.246G	29.14u	154.1p	161p
ss_13	1.1	27	ss	pass	2.661G	23.89u	187.9p	197p
ss_14	1.1	140	ss	pass	1.929G	17.32u	259.1p	272.6p
tt_0	900m	-40	tt	pass	2.589G	19.2u	193.1p	184.8p
tt_1	900m	27	tt	pass	2.084G	15.44u	239.9p	229.6p
tt_2	900m	140	tt	pass	1.503G	11.12u	332.6p	317.8p
tt_3	950m	-40	tt	pass	3.059G	23.86u	163.5p	160.3p
tt_4	950m	27	tt	pass	2.459G	19.17u	203.3p	199.6p
tt_5	950m	140	tt	pass	1.758G	13.7u	284.4p	279.2p

tt_6	1	-40	tt	pass	3.514G	28.75u	142.3p	142.6p
tt_7	1	27	tt	pass	2.828G	23.14u	176.8p	177.6p
tt_8	1	140	tt	pass	2.013G	16.46u	248.4p	249.9p
tt_9	1.05	-40	tt	pass	3.952G	33.84u	126.5p	129.4p
tt_10	1.05	27	tt	pass	3.189G	27.31u	156.8p	160.9p
tt_11	1.05	140	tt	pass	2.265G	19.41u	220.8p	227p
tt_12	1.1	-40	tt	near	4.373G	39.09u	114.4p	119.2p
tt_13	1.1	27	tt	pass	3.54G	31.67u	141.3p	147.9p
tt_14	1.1	140	tt	pass	2.513G	22.51u	198.9p	208.9p

C. Monte Carlo:

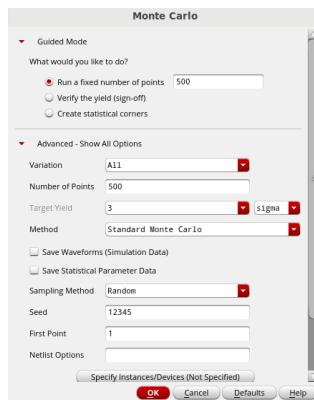


Image 61 - Monte Carlo Setup

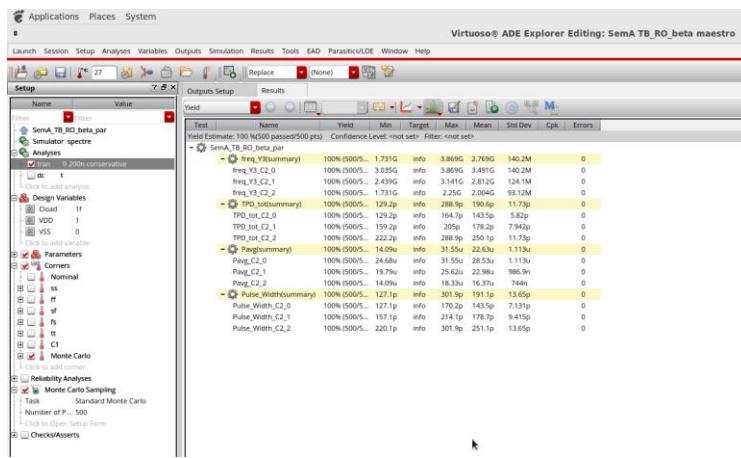


Image 62 – Monte Carlo

Monte Carlo: C is a corner that was set with $VDD=1$ V and with 3 different temperatures; -40, 27, and 120 degrees Celsius.

$C2_0: T = -40$

$C2_1: T = 27$

$C2_2: T = 120$

Parameter	C2_0	C2_1	C2_2
VDD	1	1	1
gpdk045.scs	mc	mc	mc
temperature	-40	27	140

Image 63 – Monte Carlo Corners

The data was then simulated into histograms which are pictured below.

The histogram represents a dataset with 500 samples, showing its distribution shape, spread, and key statistics. The red bars represent the frequency distribution of the data values. The red scatter points show individual data points. The black curve represents the fitted probability density function (PDF), helping us assess how well the data follows a normal distribution. The data seems roughly bell-shaped, suggesting a near-normal distribution.

The Mean – The central value (average) of the dataset.

Standard Deviation – Measures how spread out the values are from the mean. A lower value means data is more concentrated around the mean.

Skewness – Negative skew indicates a slightly longer left tail, meaning a few lower values grad the distribution left.

Each Histogram had 500 data points.

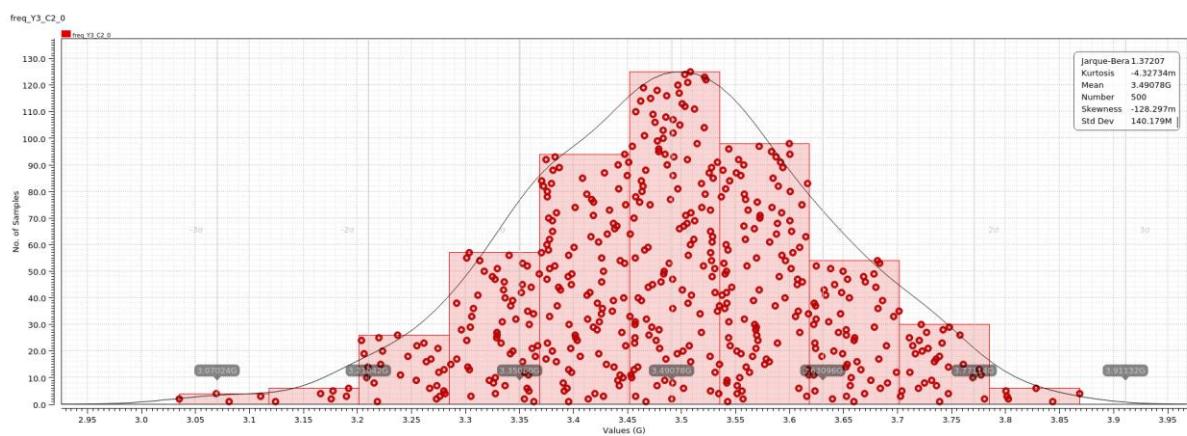


Image 64 - Histogram C2_0 -40 degrees

Results:

Mean: 3.49078G

Skewness: -128.297m

Std Dev: 140.179M

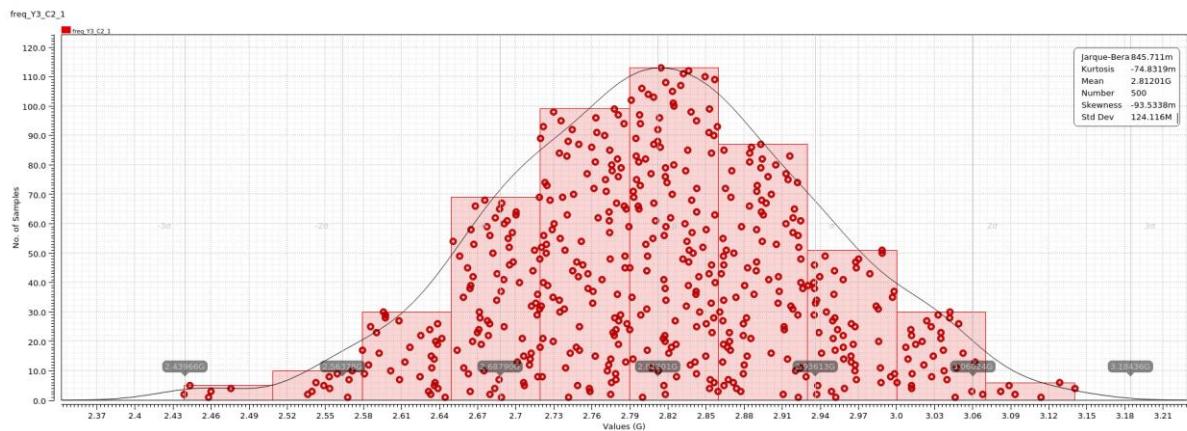


Image 65 - Histogram C2_1 27 degrees

Results:

Mean : 2.81201G

Skewness: -93.5338m

STD: 124.116M

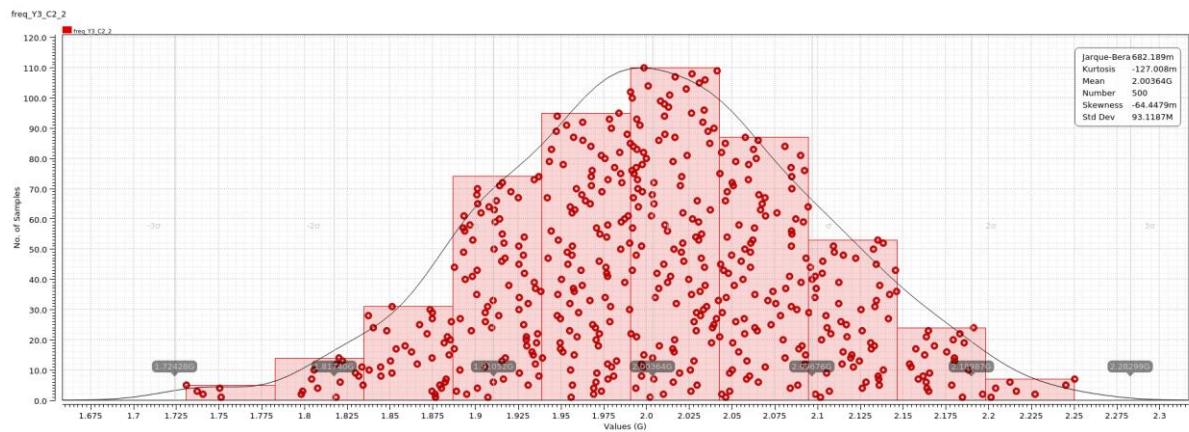


Image 66 - Histogram C2_2 120 degree

Results:

Mean: 2 G

Skewness: - 64.4479m

STD: 93.118M

120 degrees had the lowest STD of them all meaning data is closer to the average. The mean of 120 degrees was also the smallest, and the colder temps had a larger mean. At 27 degrees there was the most skew pulling its histogram to the left.

Amplifier

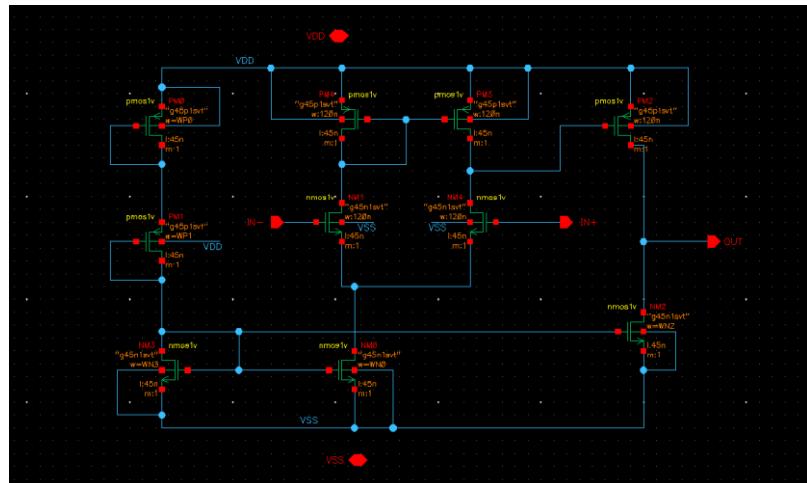


Image 67 - Amplifier – Schematic

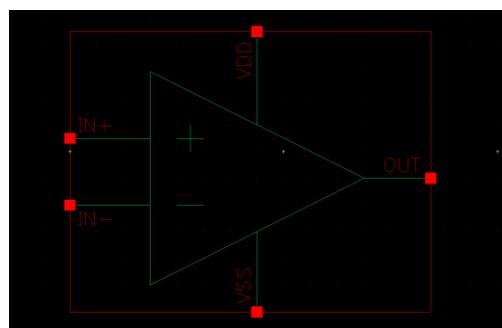


Image 68 – Amplifier Symbol

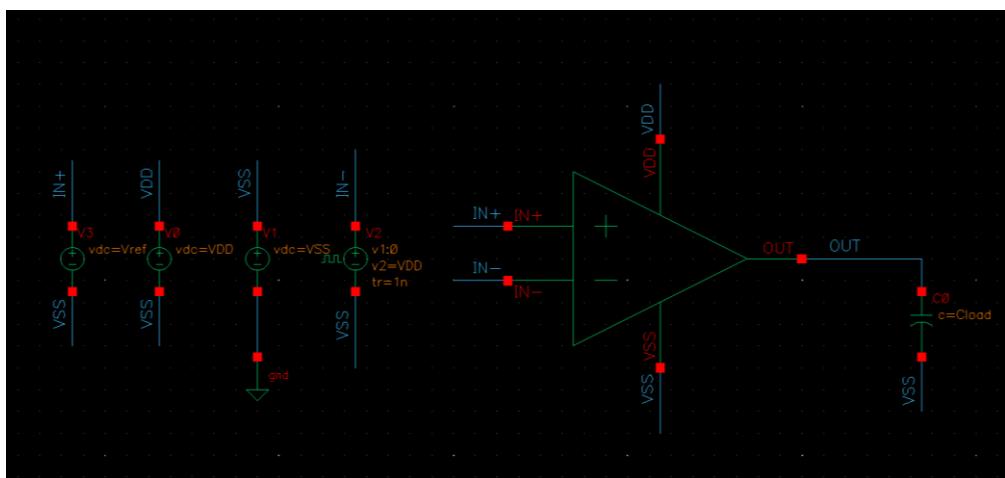


Image 69 – TB Amplifier

$$VDD = 1V$$

$$Cload = 2fF (TZ:342785912)$$

Trise and Tfall equations were added to the maestro.

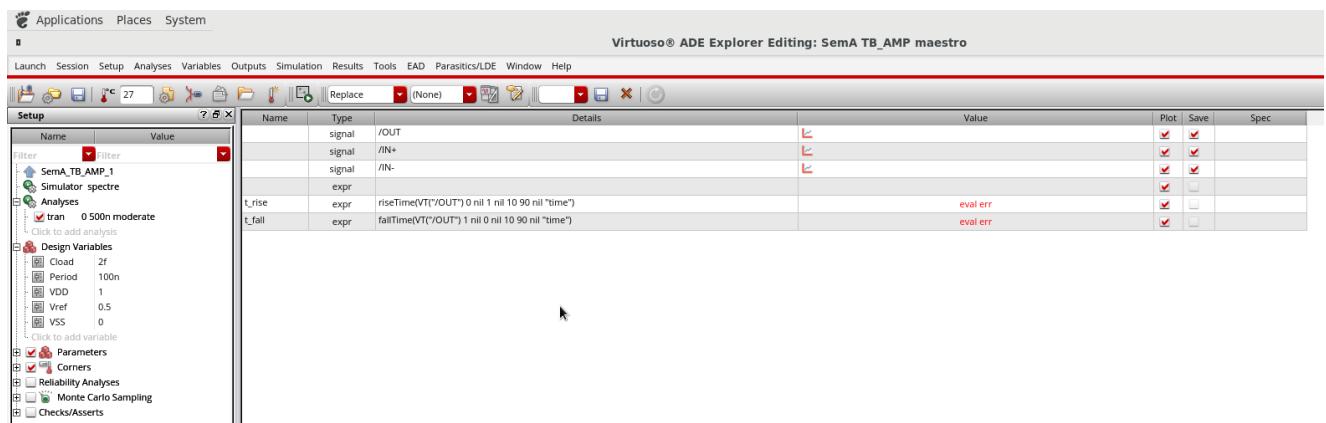


Image - Amplifier Maestro



Image 70 – Amp Simulation

It can be seen from the simulation that the OUT value starts at 1 but does not succeed in getting all the way to 0. There is an offset of 430.325mV.

The Program will not be able to evaluate the trise and tfall properly since the Amp does not reach a value of 0.1V. Additionally, the trise is very fast, but the tfall takes a long time as can be seen in the simulation. This means it does not even fully discharge before the capacitor is charged again to 1.

In order to fix this we will need to lower the frequency. The Period will be changed from 100 ns to 1μs.

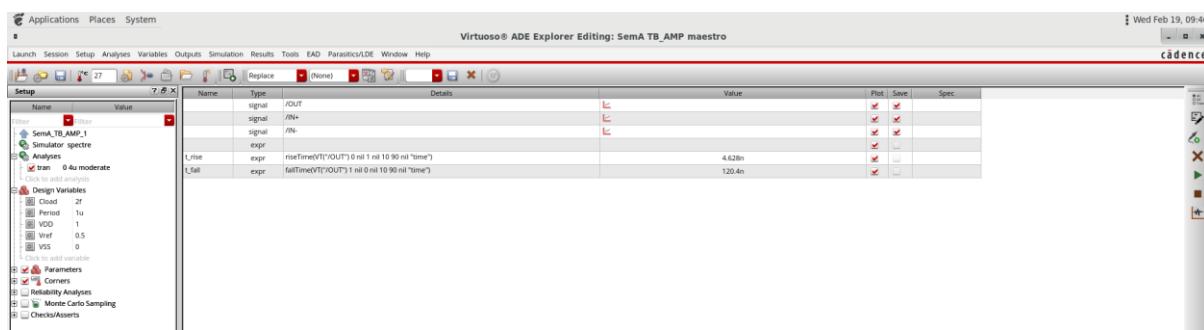


Image 71 – Amp maestro 2

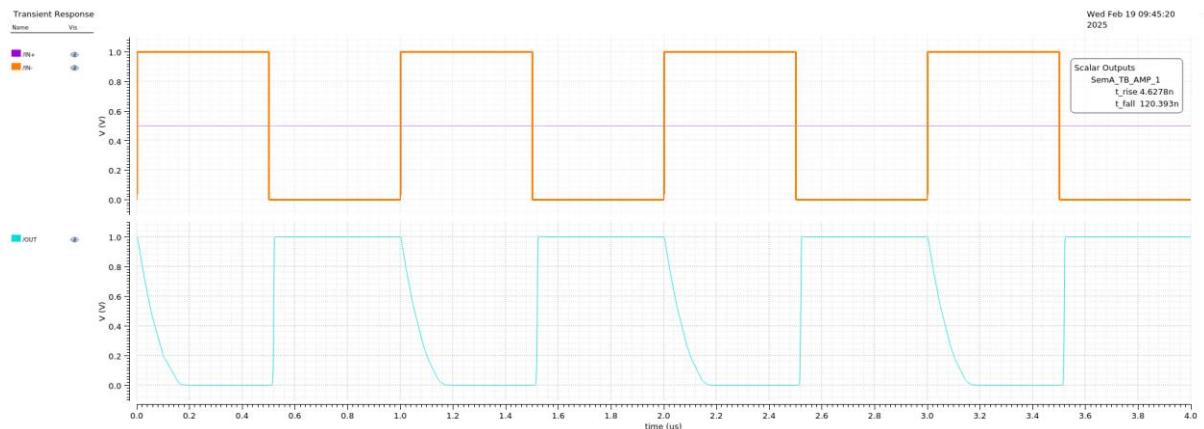


Image 72 – Amp Simulation 2

The Trise and Tfall can be properly measured. Another problem that arises is that the trise and the tfall are not at the same unit size, they are too far apart. This can be seen from both the maestro output and from the simulation graphs. To get a properly working amplifier the trise and tfall need to be within the same unit range.

The goal is to fix this new issue and make the trise and tfall similar sizes.

This will be done by changing the Width size of specific transistors in the circuit.

NM2 is the NMOS transistor directly responsible for pulling the output node down to VSS during the fall time. It's essentially a simple inverter at the output. Increasing its width (W_{N2}) will significantly reduce tfall because it increases the current drive capability of the NMOS pull-down network. The wider W_{N2} is, the stronger the pull-down and the faster the output voltage will fall. Since the effective resistance (R_{eff}) is inversely proportional to the Width, when the width is raised, the R_{eff} falls which allows for stronger current through transistors and a smaller rise/fall time.

At an initial look at the circuit, NM2 seems to be the ideal transistor to change its size. But, as the tfall will fall, at one point the trise will become smaller as well. This will keep the unwanted discrepancy between the rise and fall times. This happens since there are other transistors in the circuit that influence the circuit's rise and fall times.

P2 and P3 form a current mirror. N0 and N1 also form a current mirror. N2 and N3 form a differential pair. P0 and P1 create more resistance from VDD to the discharging transistors, NM2. Therefore, all of the transistor sizes will need to be taken into account and changed to find an ideal tfall and trise times.

The different Widths will be replaced by parameters and swept in the simulation to find the proper ideal values of each.

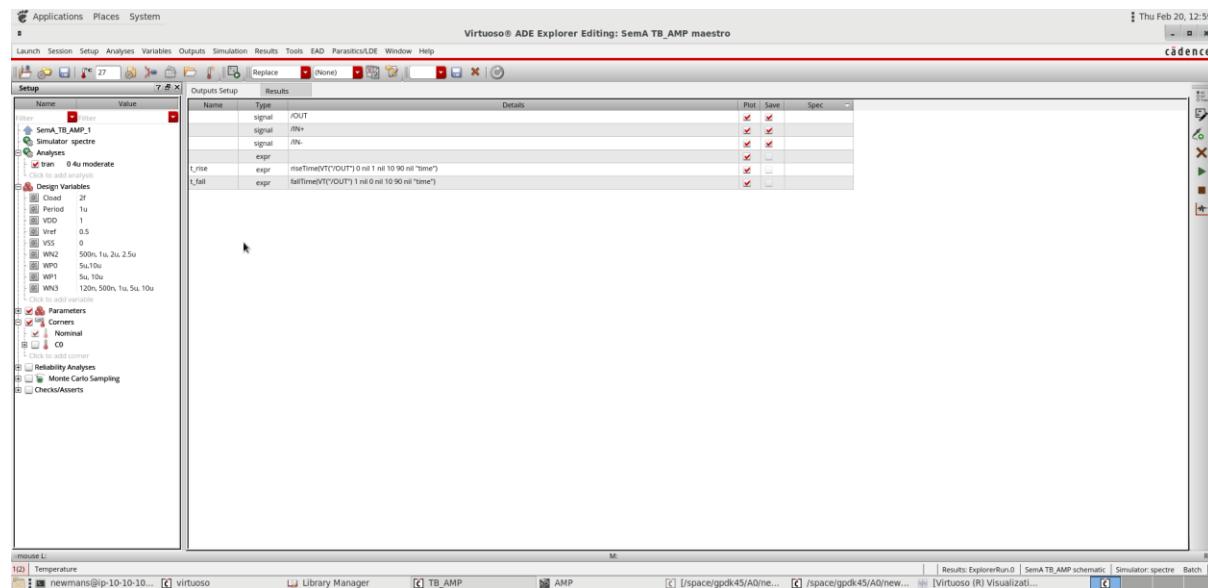


Image 73 – W tests

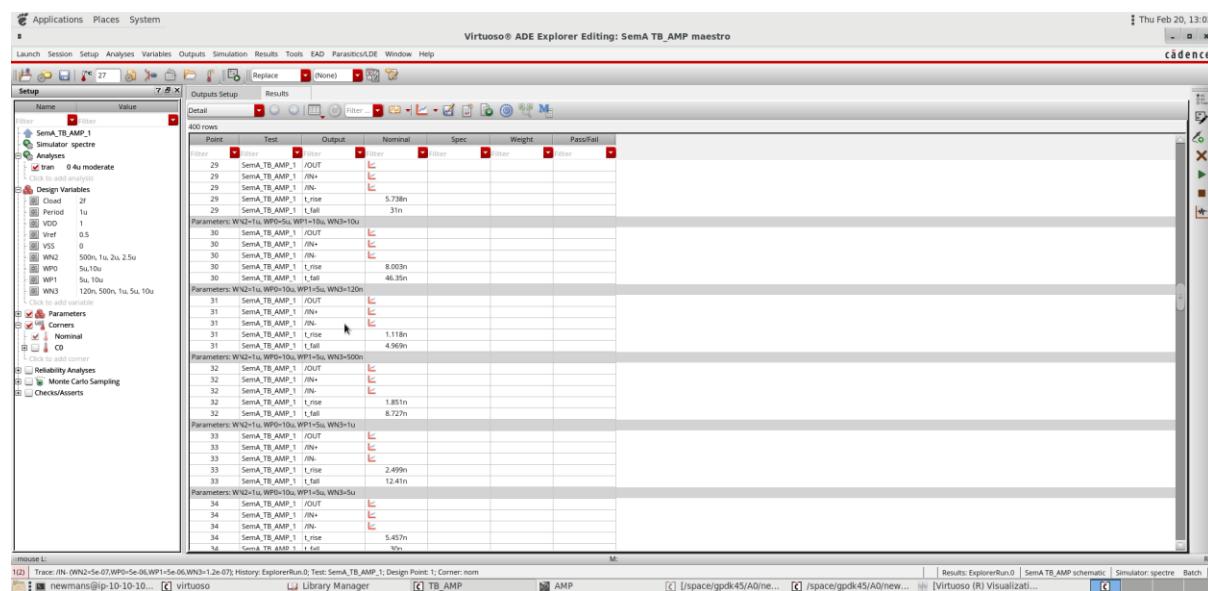


Image 74 – W values sweep

The values for trise and tfall should be close but distinguishable. The values chosen for the circuit will be the following:

$$WN2 = 1\mu m$$

$$WN3 = 120n$$

$$WP0 = 10\mu$$

$$WP1 = 5\mu$$

$$Trise = 1.118ns$$

$$Tfall = 4.969ns$$

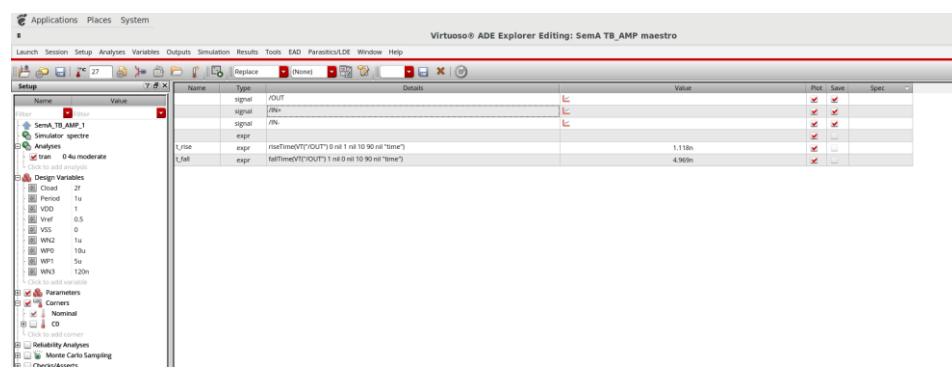


Image 75 – W values shown

When building the layout the transistors cannot exceed over 2μ . Therefore, for the large transistors we will apply fingers. Values were retested when fingers where applied. In the end the following will be used:

$$WN2 = 1\mu \rightarrow 5 \text{ fingers}, WN3 = 120n, WP0 = 2.5\mu \rightarrow 10 \text{ fingers}, WP1 = 240\mu.$$

The gate connection of the fingers is set to bottom for PMOS and top for NMOS.

The result is $trise = 2.141ns, tfall = 7.895ns$.

The parameters were chosen this way in order to make the layout easier to construct. Each Width was updated in the schematic in order to build the Layout.

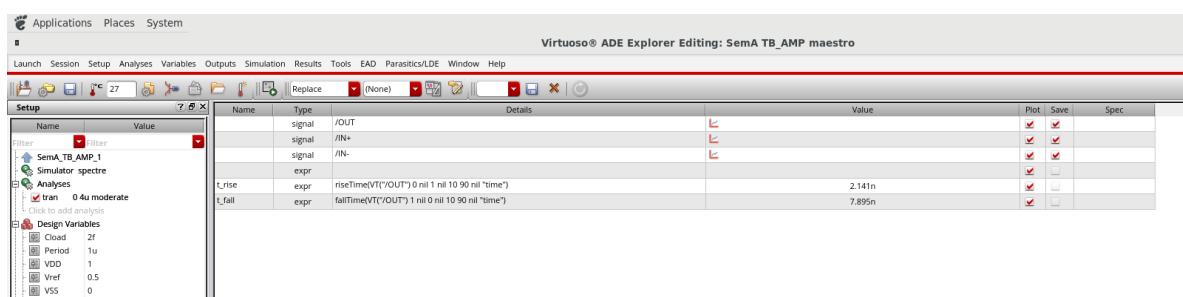


Image 76 – Amp rise/fall times after W

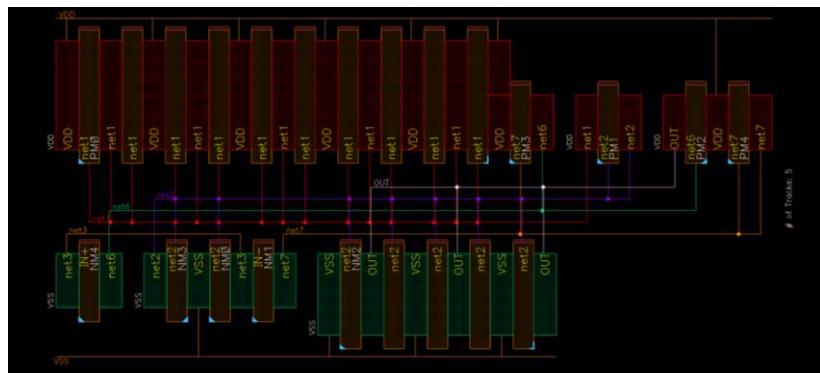


Image 77 – SPD Editing

The transistors were separated for personal preference and the layout was built in Layout XL.

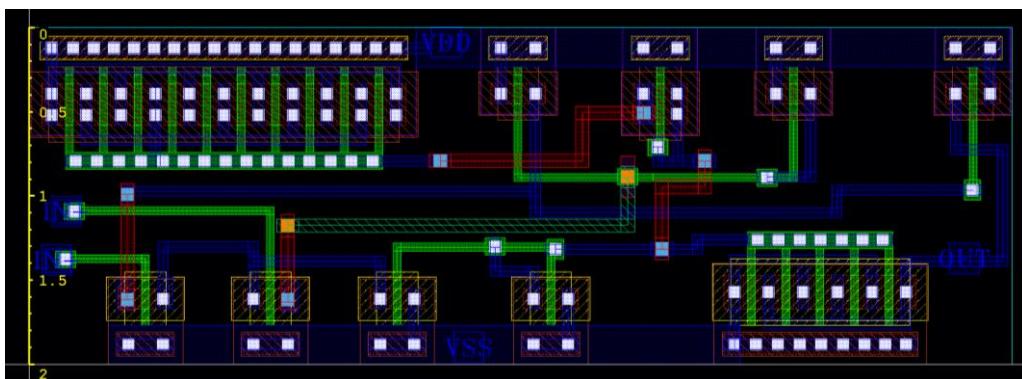


Image 78 – Amplifier Layout

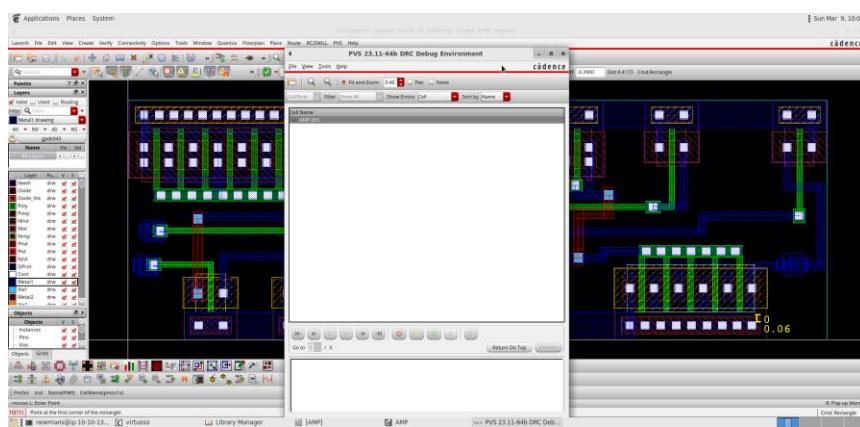


Image 79 – Amp DRC Check

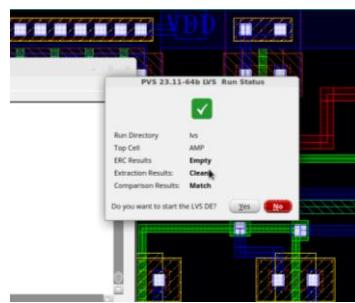


Image 80 – Amp LVS Check

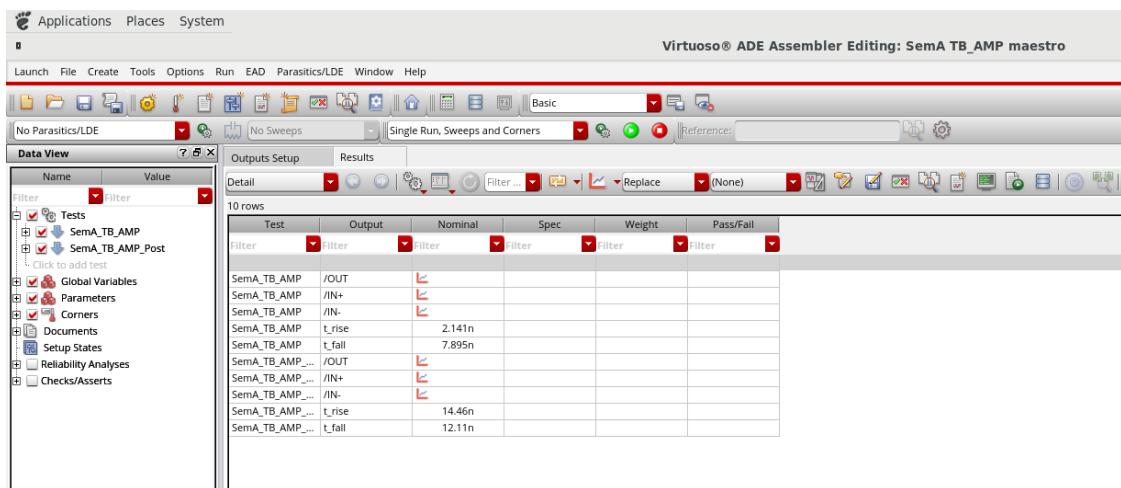


Image 81 – Trise and Tfall Post Parasitics

Due to the added resistance and capacitance $Trise$ and $Tfall$ times grew. Now the $Trise$ is larger than $Tfall$.

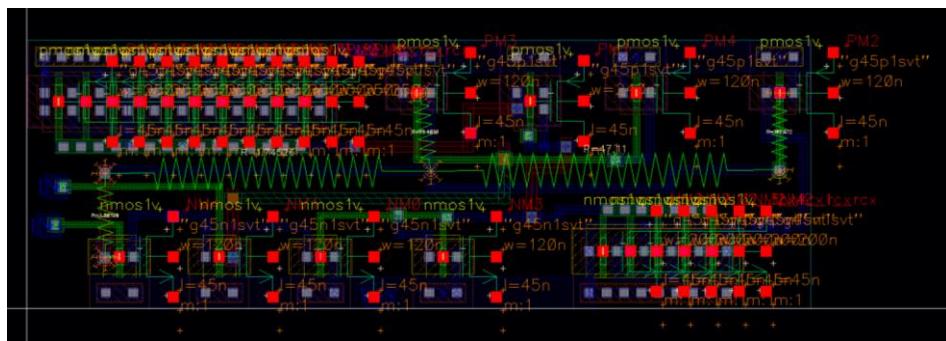


Image 82 – Layout with Parasitics

All the following measurements were done after the Parasitics were added.

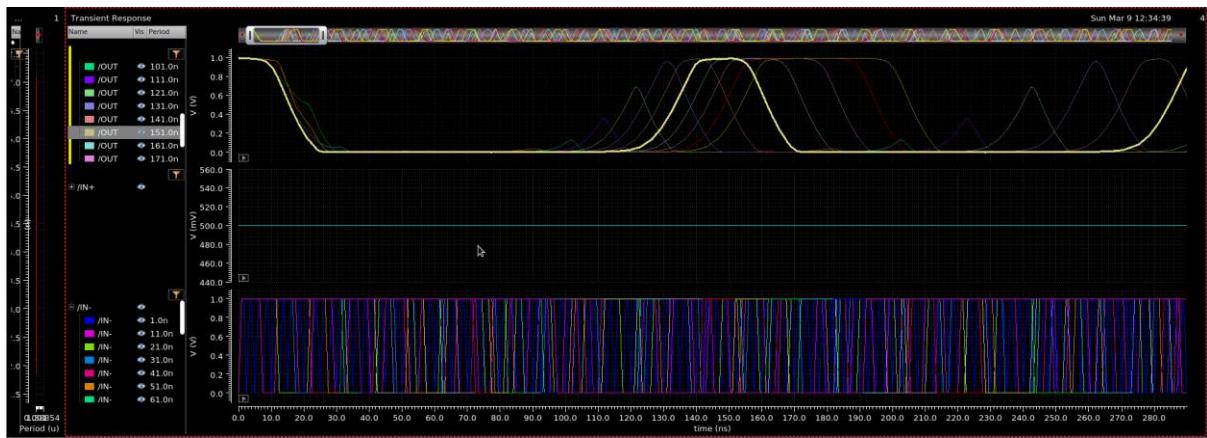


Image 83 – Stability Frequency

To test at what is the maximum frequency that the system can reach before it is no longer stable; the Period was swept from 1n to 200n. The graph from the simulation shows at what point the output was no longer stable and did not reach proper high voltage. This happened when the Period value was 151ns.

$$f_{max} = \frac{1}{151n} = 6.6225 \text{ MHz}$$

Next the system was investigated for stability at different temperatures and frequencies. This was done using corners in the maestro setup.

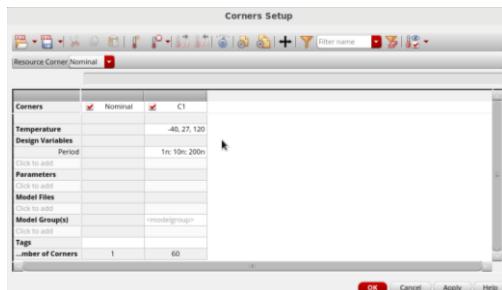


Image 84 – Amp Corner Setup

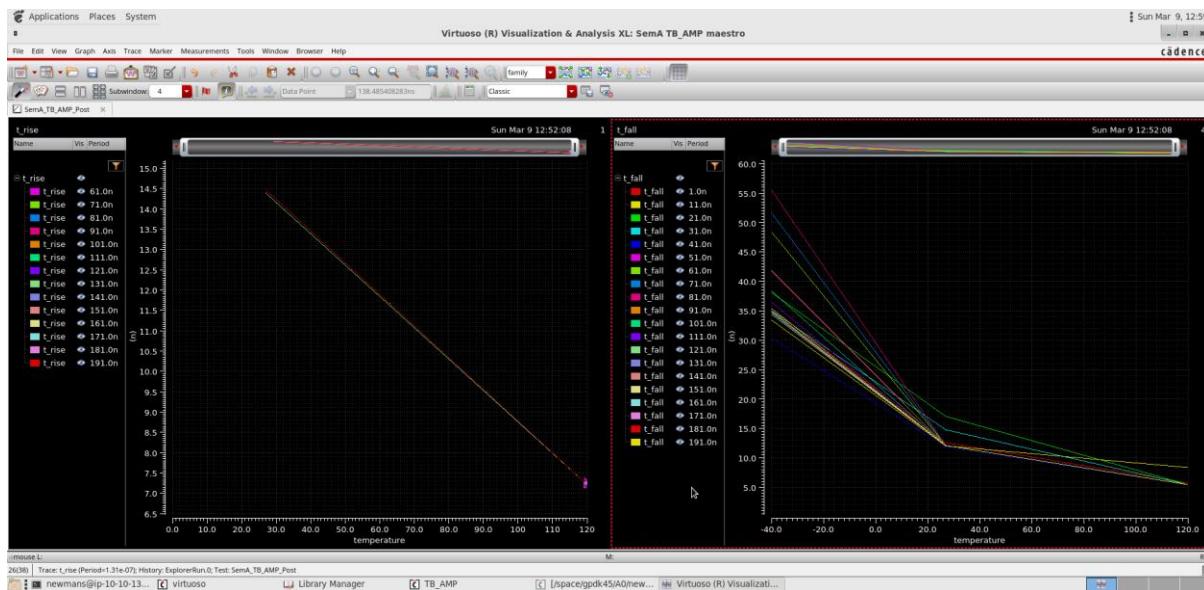


Image 85 – Trise and Tfall Relative to Temperature

The graphs above show how the Trise and Tfall of the Amp change as the temperature of the system changes. The system was tested at 3 different temperatures, -40, 27 and 120. When the temperature was higher, the rise and fall times of the system were faster. The rise time fell linearly with the temperature, but the fall time fell at a lower rate for each change of temperature.

While Trise stayed consistent between each different tested frequency, the Tfall was different at each value. It also did not change in any specific pattern.

The Results have been recorded in the table below;

Table 2 – Amplifier Corners

Period	Temperature	Column1	T_rise	T_fall
151n	27		14.47n	12.11n
1n	-40	eval err	35.43n	
1n	27	eval err	12.6n	
1n	120	eval err	5.756n	
11n	-40	eval err	33.44n	
11n	27	eval err	12.03n	
11n	120	eval err	8.366n	
21n	-40	eval err	38.12n	
21n	27	eval err	17.07n	
21n	120	eval err	5.462n	
31n	-40	eval err	35.04n	
31n	27	eval err	14.78n	
31n	120	eval err	5.462n	
41n	-40	eval err	30.39n	
41n	27	eval err	11.87n	
41n	120	eval err	5.462n	

51n	-40	eval err	41.81n
51n	27	eval err	12.11n
51n	120	eval err	5.462n
61n	-40	eval err	48.43n
61n	27	eval err	12.11n
61n	120	7.302n	5.462n
71n	-40	eval err	51.66n
71n	27	eval err	12.11n
71n	120	7.212n	5.462n
81n	-40	eval err	55.55n
81n	27	eval err	12.11n
81n	120	7.213n	5.462n
91n	-40	eval err	41.92n
91n	27	eval err	12.11n
91n	120	7.213n	5.462n
101n	-40	eval err	38.39n
101n	27	eval err	12.11n
101n	120	7.213n	5.462n
111n	-40	eval err	36.46n
111n	27	eval err	12.11n
111n	120	7.213n	5.462n
121n	-40	eval err	34.41n
121n	27	eval err	12.11n
121n	120	7.213n	5.462n
131n	-40	eval err	34.8n
131n	27	14.39n	12.11n
131n	120	7.213n	5.462n
141n	-40	eval err	34.65n
141n	27	14.47n	12.11n
141n	120	7.213n	5.462n
151n	-40	eval err	34.97n
151n	27	14.47n	12.11n
151n	120	7.213n	5.462n
161n	-40	eval err	35.4n
161n	27	14.47n	12.11n
161n	120	7.213n	5.462n
171n	-40	eval err	35.4n
171n	27	14.47n	12.11n
171n	120	7.214n	5.462n
181n	-40	eval err	35.4n
181n	27	14.47n	12.11n
181n	120	7.213n	5.462n
191n	-40	eval err	35.4n
191n	27	14.47n	12.11n

191n	120	7.213n	5.462n
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When the Amplifier was at -40 degrees, there was never a proper rise time and the Amplifier was not stable. When the temperature was 120 degrees, the system was stable for many runs where it was not at normal 27 degrees. Until a Period of 61ns nothing was stable. According to the table the Amp was stable at 27 degrees *Period = 131ns*. While this seems true, from the graphs above the Amp did not properly reach the high Voltage, so it was not counted as stable when determining the max frequency.