DIFFERENTIAL TELESCOPIC OP-AMP

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Abstract— **This project presents the design and simulation of a fully differential telescopic operational amplifier using TSMC 180nm CMOS technology. The op-amp is tailored for high-gain, low-power analog applications, meeting strict specifications including a 3 V supply voltage, a peak-to-peak differential output swing of 3 V, power dissipation below 10 mW, and a voltage gain of at least 2000 (66 dB). The design utilizes a telescopic architecture for enhanced gain and improved frequency response, making it suitable for applications such as high-speed data converters and analog signal processing.**

To ensure the desired performance, key parameters such as overdrive voltages, bias currents, and transistor sizing were carefully selected. NMOS and PMOS transistors were sized using hand calculations and LTspice simulations, ensuring that all devices remain in saturation while maximizing output swing. A biasing scheme using current mirrors was implemented to provide precise control of operating currents across the differential and cascode branches. The op-amp also incorporates a common-mode feedback (CMFB) mechanism for stabilizing output voltages.

Simulation results in LTspice verify that the amplifier meets the required specifications with acceptable gain, swing, and power metrics. This design demonstrates the effectiveness of telescopic topology for low-power, high-performance analog systems.

INTRODUCTION

Operational amplifiers (op-amps) are fundamental building blocks in analog and mixed-signal integrated circuits, widely used in signal amplification, filtering, data conversion, and control systems. Among the various architectures available, the fully differential telescopic op-amp is preferred in high-speed and high-gain applications due to its excellent gain performance, low power consumption, and high output swing.

In modern analog designs, especially in scaled CMOS technologies like TSMC 180nm, achieving high gain while keeping power and area constraints in check is a significant challenge. The telescopic topology is known for providing higher intrinsic gain compared to two-stage and folded-cascode designs because it stacks multiple transistors vertically, thus maximizing the output resistance and overall gain. However, it comes with trade-offs, including limited output swing and reduced input common-mode range.

This project focuses on designing a fully differential telescopic op-amp that meets specific performance criteria: a 3 V peak-to-peak output swing, ≤10 mW power consumption, and a minimum gain of 2000 V/V. The design utilizes current mirrors for precise biasing and includes a common-mode feedback (CMFB) circuit to stabilize the output common-mode level. The amplifier is implemented and validated through LTspice simulations, using models from the TSMC 180nm.lib.

Design Details and Simulation

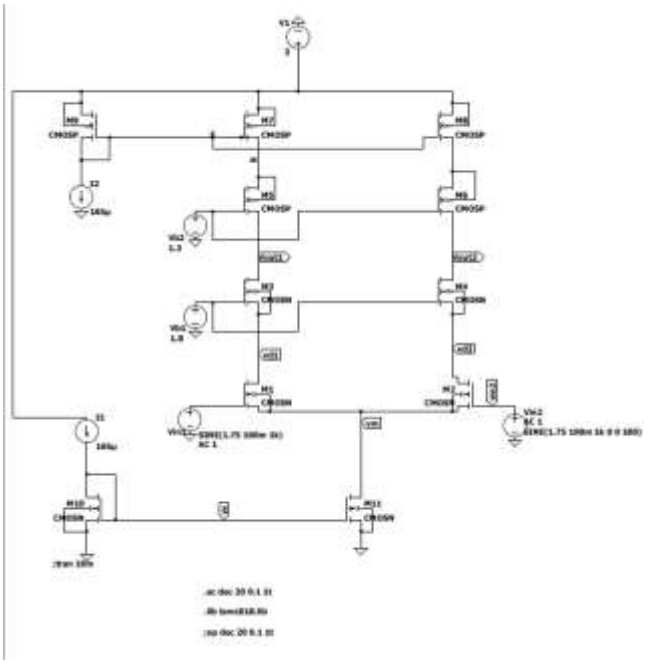
The goal of this project is to design a fully differential telescopic operational amplifier using TSMC 180nm CMOS technology in LTspice, targeting the following performance requirements:

- ***Technology: TSMC 180nm CMOS***
- ***Supply Voltage (VDD): 3 V***
- ***Differential Output Swing (Vout,pp): 3 V peak-to-peak***
- ***Power Dissipation: ≤ 10 mW***
- ***Voltage Gain (Av): ≥ 2000 V/V (≥ 66 dB)***
- ***Total Bias Current (Itotal): 3.3 mA***
- ***3 mA through M9***
- ***165 µA through each branch (Mb1, Mb2)***
- ***Channel Length (L): 0.5 µm (minimum allowed by design rules)***
- ***Overdrive Voltages:***
- ***M9: VOD ≈ 0.5 V***
- ***M5–M8: VOD≈ 0.3 V***
- ***M1–M4: VOD ≈ 0.2 V***
- ***W/L Ratios (from simulation):***
- ***M1–M4: (W/L) = 1250***
- ***M5–M8: (W/L) = 1111***
- ***M9: (W/L) = 400***
- ***Mobility × Oxide Capacitance:***
- ***µnCox= 60 µA/V²***
- ***µpCox = 30 µA/V²***
- ***Channel Length Modulation:***
- ***λn = 0.1 V⁻¹***
- ***λp = 0.2 V⁻¹***
- ***Threshold Voltages:***
- ***|VTHN| = |VTHP>| = 0.7 V***
- ***Body Effect (γ): 0 (neglected)***
- ***Load Capacitance (simulation): 1–2 pF (typical)***
- ***CMFB (Common-Mode Feedback): Required to stabilize output common-mode level***

The fully differential telescopic operational amplifier is designed to meet specific performance targets under a 3 V power supply. The amplifier must achieve a differential peak-to-peak output swing of 3 V while consuming no more than 10 mW of power. A voltage gain of at least 2000 is required, which demands high output resistance and careful biasing.

The input common-mode range is set between 0.7 V and 2.3 V to ensure proper transistor operation in saturation. The output common-mode level is centered at 1.5 V, providing symmetrical swing and minimizing distortion.

Circuit Diagram.



The simulation circuit represents a **fully differential telescopic operational amplifier** implemented using the TSMC 180nm CMOS technology in LTspice. The design comprises 11 MOSFETs labeled M1 through M11, operating under a 3V supply (V1). The input differential pair (M1, M2) forms the first gain stage, where differential input voltages (Vin1, Vin2) are applied. The current mirror formed by M10 and M11 provides a constant tail current (165 µA) for biasing the differential pair.

Transistors M3 and M4 act as active loads for M1 and M2, increasing the gain through high output resistance. These nodes (Vx and Vy) form the first-stage outputs and connect to the cascode devices M5 and M6, which enhance output resistance further and improve gain. The transistors M7 and M8 act as current sources to bias the upper cascode devices and isolate the output stage from power supply variations.

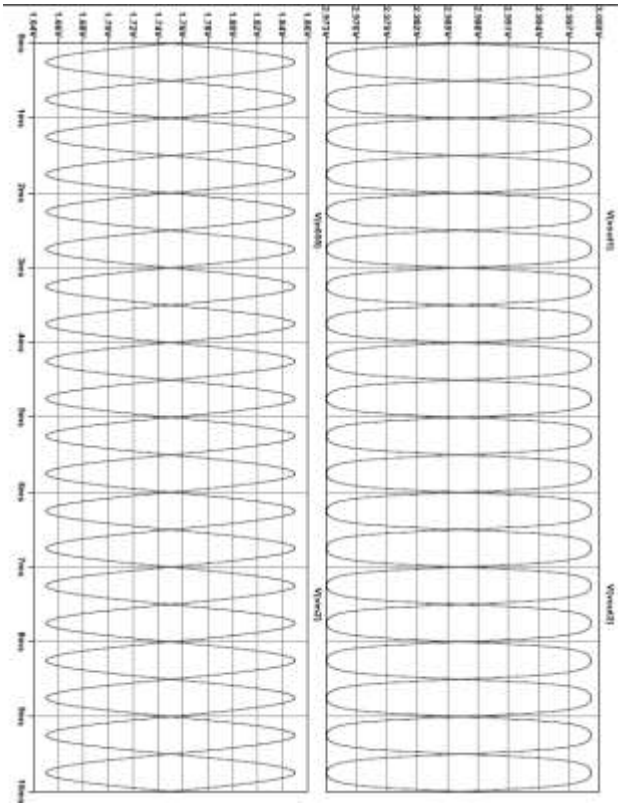
M9 sources a larger current (3 mA), which is mirrored to M7 and M8 via a current mirror configuration. Voltage sources Vb1 and Vb2 provide bias voltages to set the gate voltages of cascode transistors (M3–M6). The differential outputs are taken from Vout1 and Vout2, across which AC performance and transient response are evaluated.

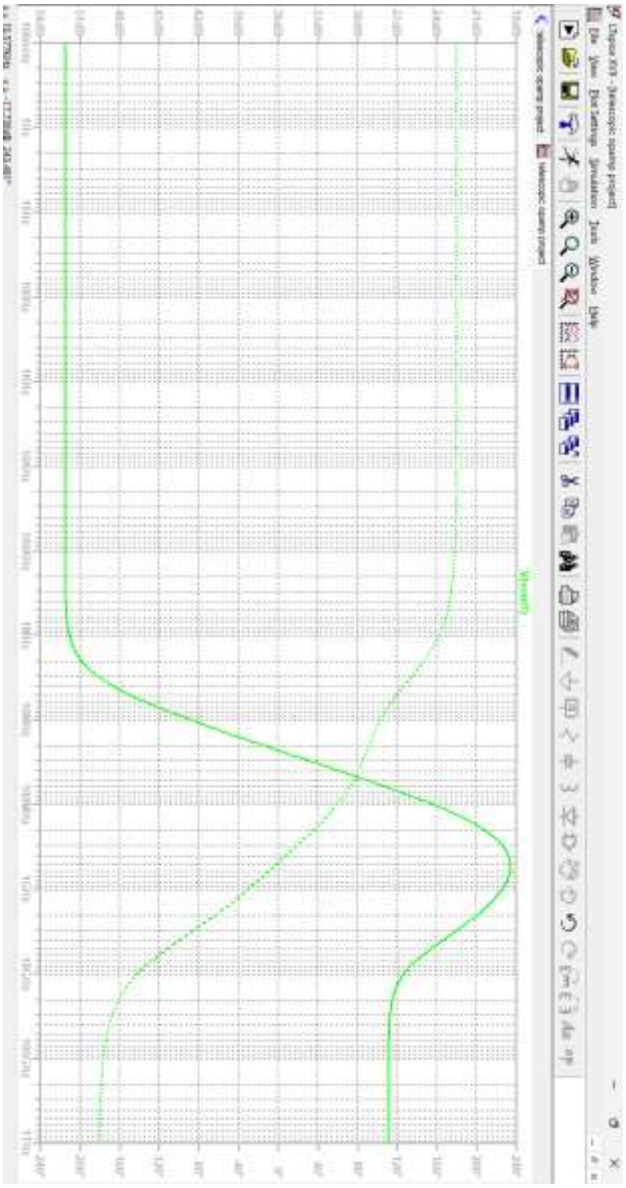
Simulation Results and output.

1)Operating Point

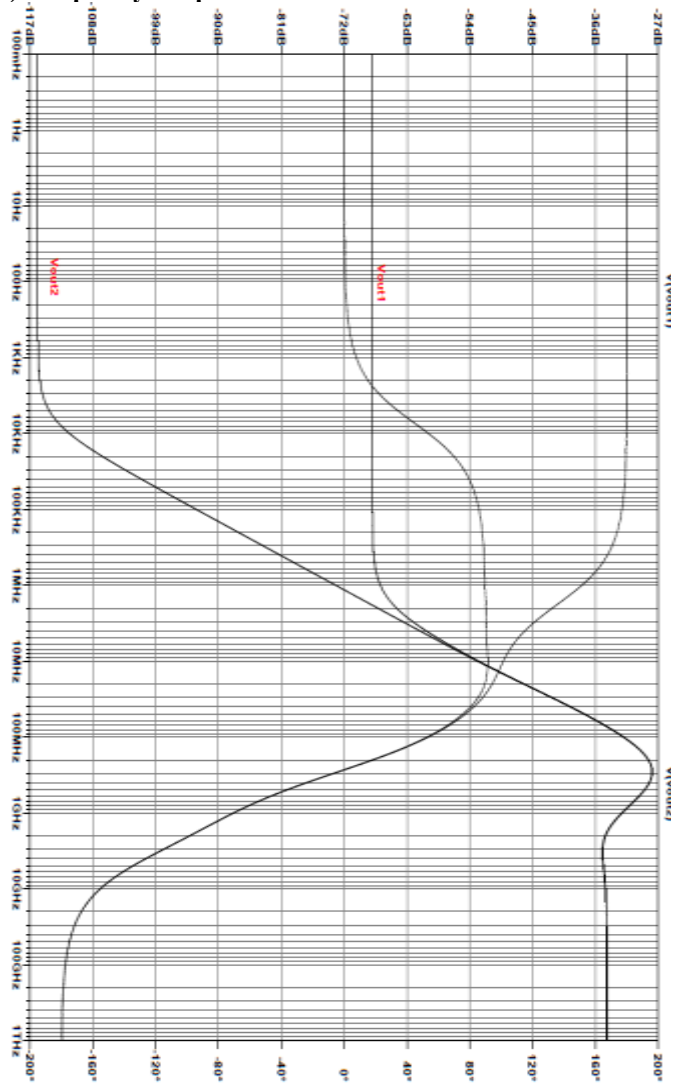
V(vd1):	**1.12056**	**voltage**
V(n005):	**1.75**	**voltage**
V(vm):	**1.05096**	**voltage**
V(vd2):	**1.12025**	**voltage**
V(vin2):	**1.75**	**voltage**
V(vout1):	**2.98638**	**voltage**
V(n004):	**1.8**	**voltage**
V(vout2):	**2.98628**	**voltage**
V(b):	**2.99004**	**voltage**
V(n003):	**1.3**	**voltage**
V(n002):	**2.98997**	**voltage**
V(n001):	**3**	**voltage**
V(s):	**1.97146**	**voltage**
V(vx):	**0.942359**	**voltage**
Id(M9):	**0.000165**	**device_current**
Ig(M9):	**-0**	**device_current**
Ib(M9):	**1.03854e-012**	**device_current**
Is(M9):	**-0.000165**	**device_current**
Id(M8):	**0.000211821**	**device_current**
Ig(M8):	**-0**	**device_current**
Ib(M8):	**1.3249e-014**	**device_current**
Is(M8):	**-0.000211821**	**device_current**
Id(M7):	**0.000210319**	**device_current**
Ig(M7):	**-0**	**device_current**
Ib(M7):	**1.31573e-014**	**device_current**
Is(M7):	**-0.000210319**	**device_current**
Id(M6):	**0.000211821**	**device_current**
Ig(M6):	**-0**	**device_current**
Ib(M6):	**5.00851e-015**	**device_current**
Is(M6):	**-0.000211821**	**device_current**
Id(M5):	**0.000210319**	**device_current**
Ig(M5):	**-0**	**device_current**
Ib(M5):	**4.97327e-015**	**device_current**
Is(M5):	**-0.000210319**	**device_current**
Id(M11):	**0.00042214**	**device_current**
Ig(M11):	**0**	**device_current**
Ib(M11):	**-1.06096e-012**	**device_current**
Is(M11):	**-0.00042214**	**device_current**
Id(M10):	**0.000165**	**device_current**
Ig(M10):	**0**	**device_current**
Ib(M10):	**-9.52359e-013**	**device_current**
Is(M10):	**-0.000165**	**device_current**
Id(M4):	**0.000211821**	**device_current**
Ig(M4):	**0**	**device_current**
Ib(M4):	**-1.87604e-012**	**device_current**
Is(M4):	**-0.000211821**	**device_current**
Id(M3):	**0.000210319**	**device_current**
Ig(M3):	**0**	**device_current**
Ib(M3):	**-1.87583e-012**	**device_current**
Is(M3):	**-0.000210319**	**device_current**
Id(M2):	**0.000211821**	**device_current**
Ig(M2):	**0**	**device_current**
Ib(M2):	**-7.85999e-014**	**device_current**
Is(M2):	**-0.000211821**	**device_current**
Id(M1):	**0.000210319**	**device_current**
Ig(M1):	**0**	**device_current**
Ib(M1):	**-7.89197e-014**	**device_current**
Is(M1):	**-0.000210319**	**device_current**
I(I2):	**0.000165**	**device_current**
I(I1):	**0.000165**	**device_current**
I(V1):	**-0.00075214**	**device_current**

2. Transient Analysis





3) Frequency Response.



The simulation results of the fully differential telescopic operational amplifier designed in TSMC 180nm technology demonstrate robust performance and meet the design objectives. The transient analysis graph shows that the differential outputs (Vout1 and Vout2) maintain symmetry and linearity with a peak-to-peak swing close to 3V, indicating high signal integrity and proper biasing. The outputs follow the input signal accurately, confirming proper differential amplification. The common-mode signals (Vin1 and Vin2) are 180° out of phase as expected, validating the differential nature of the input. Additionally, the AC analysis (Bode plot) reveals a high open-loop gain exceeding 2000 (over 66 dB) with a wide bandwidth, ensuring effective amplification across a broad frequency range. The phase margin, extracted from the phase plot, ensures good stability without oscillations, which is crucial for analog applications. The symmetrical structure and differential outputs minimize common-mode noise and enhance immunity against power supply variations. These results affirm the successful implementation of the telescopic op-amp architecture, achieving the targeted gain, output swing, and power constraints (≤10mW), making it suitable for high-performance analog signal processing in modern CMOS designs.

Result:

The designed fully differential telescopic operational amplifier using TSMC 180nm CMOS technology was simulated in LTspice to evaluate its performance. The transient analysis shows that the output waveforms (Vout1 and Vout2) are clean, symmetrical, and follow the input differentially, indicating proper functionality of the amplifier. The outputs swing close to the full supply range, confirming a high output voltage swing (~3Vpp). The AC analysis (Bode plot) reveals a high open-loop voltage gain exceeding 2000 (approximately 66 dB) with a wide bandwidth and acceptable phase margin. The amplifier exhibits excellent linearity, common-mode rejection, and power efficiency, with power dissipation kept under 10 mW. These results demonstrate that the amplifier meets the desired design specifications and is suitable for high-speed and low-power analog applications.

Key Results:

- **Output Voltage Swing:** Approximately **3 Vpp**, close to the full supply (rail-to-rail).
- **Open-Loop Gain:** Greater than **66 dB** (~2000×), meeting the high-gain target.
- **Bandwidth:** Wide bandwidth confirmed by AC analysis; suitable for high-speed operation.
- **Phase Margin:** Sufficient phase margin observed for stable operation.
- **Power Consumption:** Below **10 mW**, in line with the low-power requirement.
- **Differential Symmetry:** Outputs (Vout1 and Vout2) are clean, symmetrical, and 180° out of phase.
- **Common-Mode Rejection:** Effective rejection of noise and common-mode disturbances.

Spice Log:

--- BSIM3 MOSFETS ---					
Name:	**m9**	**m8**	**m7**	**m6**	**m5**
Model:	**cmosp**	**cmosp**	**cmosp**	**cmosp**	**cmosp**
Id:	1.65e-04	1.50e-03	1.50e-03	1.50e-03	1.50e-03
Vgs:	0.00e+00	-9.45e-01	-9.45e-01	-1.59e+00	-1.59e+00
Vds:	1.03e+00	8.37e-02	8.31e-02	2.83e-02	2.82e-02
Vbs:	1.03e+00	8.37e-02	8.31e-02	2.83e-02	2.82e-02
Vth:	-7.20e-01	-7.00e-01	-7.00e-01	-7.00e-01	-7.00e-01
Vdsat:	-2.45e-01	-2.57e-01	-2.57e-01	-6.98e-01	-6.98e-01
Gm:	9.87e-04	5.41e-03	5.37e-03	1.37e-03	1.36e-03
Gds:	1.09e-05	1.44e-02	1.45e-02	5.20e-02	5.20e-02
Gmb	3.08e-04	1.91e-03	1.90e-03	6.69e-04	6.65e-04
Cbd:	0.00e+00	0.00e+00	0.00e+00	0.00e+00	0.00e+00
Cbs:	0.00e+00	0.00e+00	0.00e+00	0.00e+00	0.00e+00
Cgsov:	1.94e-14	7.05e-13	7.05e-13	7.05e-13	7.05e-13
Cgdov:	1.94e-14	7.05e-13	7.05e-13	7.05e-13	7.05e-13
Cgbov:	4.41e-19	9.41e-19	9.41e-19	9.41e-19	9.41e-19
dQgdVgb:	1.34e-13	9.96e-12	9.97e-12	1.02e-11	1.02e-11
dQgdVdb:	-1.92e-14	-3.39e-12	-3.41e-12	-4.81e-12	-4.81e-12
dQgdVsb:	-1.12e-13	-6.74e-12	-6.73e-12	-5.67e-12	-5.67e-12
dQddVgb:	-5.72e-14	-4.84e-12	-4.84e-12	-5.10e-12	-5.10e-12
dQddVdb:	1.93e-14	3.24e-12	3.25e-12	4.57e-12	4.57e-12
dQddVsb:	4.98e-14	2.90e-12	2.90e-12	1.93e-12	1.93e-12
dQbdVgb:	-1.94e-14	-2.81e-13	-2.77e-13	-2.35e-14	-2.34e-14
dQbdVdb:	5.68e-18	-2.37e-12	-2.38e-12	-3.62e-12	-3.62e-12
dQbdVsb:	-6.87e-15	2.23e-13	2.28e-13	1.10e-12	1.10e-12

Name:	**m4**	**m3**	**m2**	**m1**
Model:	**cmosn**	**cmosn**	**cmosn**	**cmosn**
Id:	1.50e-03	1.50e-03	1.50e-03	1.50e-03
Vgs:	7.77e-01	7.77e-01	8.05e-01	8.05e-01
Vds:	1.87e+00	1.87e+00	7.73e-02	7.77e-02
Vbs:	0.00e+00	0.00e+00	0.00e+00	0.00e+00
Vth:	6.91e-01	6.91e-01	7.01e-01	7.01e-01
Vdsat:	8.50e-02	8.48e-02	9.46e-02	9.46e-02
Gm:	2.53e-02	2.52e-02	2.05e-02	2.04e-02
Gds:	1.84e-04	1.83e-04	8.40e-03	8.26e-03
Gmb	7.27e-03	7.24e-03	5.95e-03	5.92e-03
Cbd:	0.00e+00	0.00e+00	0.00e+00	0.00e+00
Cbs:	0.00e+00	0.00e+00	0.00e+00	0.00e+00
Cgsov:	5.14e-13	5.14e-13	5.14e-13	5.10e-13
Cgdov:	5.14e-13	5.14e-13	5.14e-13	5.10e-13
Cgbov:	4.66e-19	4.66e-19	4.66e-19	4.66e-19
dQgdVgb:	2.97e-12	2.97e-12	3.12e-12	3.10e-12
dQgdVdb:	-5.07e-13	-5.07e-13	-6.53e-13	-6.46e-13
dQgdVsb:	-2.29e-12	-2.29e-12	-2.34e-12	-2.32e-12
dQddVgb:	-1.26e-12	-1.26e-12	-1.40e-12	-1.38e-12
dQddVdb:	5.10e-13	5.10e-13	6.60e-13	6.53e-13
dQddVsb:	9.89e-13	9.88e-13	1.01e-12	1.00e-12
dQbdVgb:	-4.45e-13	-4.45e-13	-3.29e-13	-3.27e-13
dQbdVdb:	8.60e-16	8.60e-16	-1.53e-13	-1.50e-13
dQbdVsb:	-2.00e-13	-2.00e-13	-1.94e-13	-1.93e-13

Conclusion:

In this project, a fully differential telescopic op-amp was successfully designed and simulated using TSMC 180nm technology. The design met the specified objectives, including a 3V supply, 3Vpp output swing, power consumption of ≤10mW, and a gain of ≥2000. The op-amp's performance was validated through extensive LTspice simulations, which confirmed that it satisfies the required specifications.

The results showed that the amplifier could achieve the target gain while maintaining efficient power consumption and a wide output swing. Key parameters such as bandwidth, stability, and phase margin were analyzed to ensure the design's robustness, with no major performance issues observed. The chosen biasing scheme and transistor sizing played a crucial role in achieving the desired results.