Verilog Assignment 7 Part 3

Group Number: 23

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We used the ALU and register bank designed in the previous assignments and integrated it in our top module. Inside top module, we built a FSM for taking in input value, which takes in the register address, lower 16 bits and upper 16 bits in separate steps from the user through the FPGA pins. We built another FSM to take in the instruction which is encoded in 16 bits and one FSM for displaying the value of the register which takes the address of the register whose value is to be displayed and displays the lower and upper sixteen bits in separate steps.

Instruction encoding:

Opcode(4 bits)	Destination(4 bits)	Source 1(4 bits)	Source 2(4 bits)

Example:

Instruction encoding of add $r2,$r1,$r0

0000 0010 0001 0000