Verilog Assignment 6
Team Number 23

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First, we created 1 single port for memory. Inside the top module, we copied the templates of the port from the respective veo file. We wrote the code for the register bank. We then created a 2-bit opcode and used if else for the 4 cases: storing into memory, moving from register to memory, moving from memory to register and displaying value stored in memory and assigned appropriate values to the variables in the templates.

Example:

1) Opcode=0 (store data to memory), value=10 and memory address=0
2) Opcode=2 (transfer from memory to register), register address=1, memory address=0
3) Opcode=1 (transfer from register to memory), register address=1, memory address=1
4) Opcode=3 (display value stored in memory), memory address=1, output=10 (value stored in memory address)