Group 23
Team Members:
Sampreeth R S (21CS30038)
Yash Kumar (21CS30059)

Verilog Assignment 4

We have used cla, complementor, subtractor and right shift modules from the previous assignment and made some changes to them.
We have divided the final 16 bits output into two 8- bit numbers out1 and out2.
We have used a decoder module to see if the case is a 00,11 or 01 or 10 case as per Booth's algorithm.
Depending on the case, we make sumenable or difenable equal to 0 or 1 and make shiftenable equal to 1 for each counter value from 8 to 1.
We terminate these operations when the counter becomes 0.