Verilog Assignment 5

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In this assignment, we have calculated the value of y=x/255 for any 32-bit x, without using any multiplier or divider.

To input 32 bits of x with only 16 switches on the FPGA board, we have used reset button to first load lower 16 bits and then another reset button to load upper 16 bits and show the output on the LEDs.

Also, the output is of 24 bits so first lower 16 bits are displayed with one reset button and pressing another reset button, we get the upper 8 bits of the output.

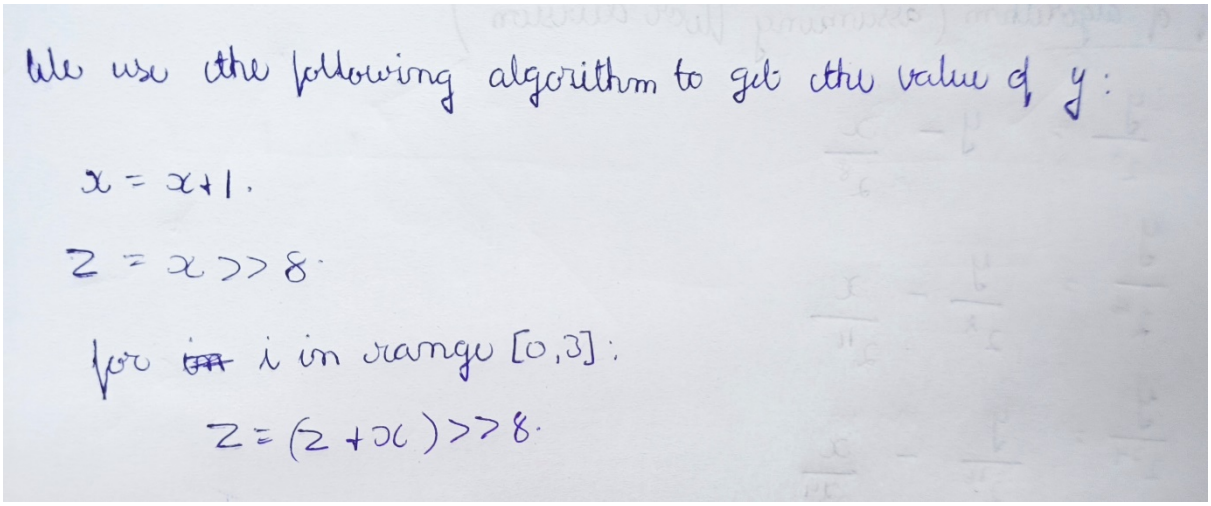
We first carried out our simulation with the algorithm given in the class which works only with values of x which are multiples of 255. We then implemented another algorithm, which works for all values of x and gives floor of x/255 as the answer.

Example:

(x=8796458, (in binary) 00000000100001100 011100100101010,

Y=x/255=34495, (in binary) 00000000 1000011010111111)

To carry out our algorithm, we have used carry lookahead adder (allowed by professor) and right shift modules. The algorithm is given in the picture below:



Proof of algorithm (assuming floor division)

$$\frac{y}{2^8} = y - \frac{x}{2^8}$$

$$\frac{y}{2^{16}} = \frac{y}{2^8} - \frac{x}{2^{16}}$$

$$\frac{y}{2^{24}} = \frac{y}{2^{16}} - \frac{x}{2^{24}}$$

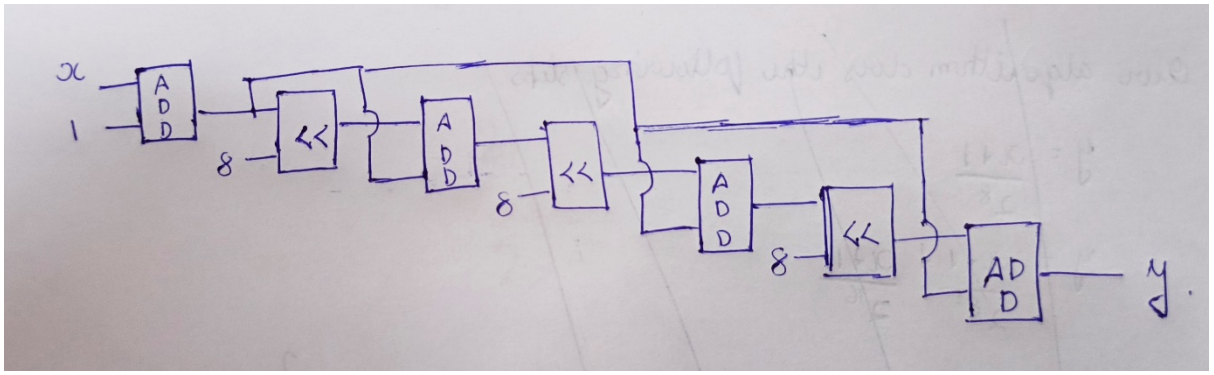
$$\frac{y}{2^{32}} = \frac{y}{2^{24}} - \frac{x}{2^{32}}$$

for 24 bits y.

Adding all,

$$y = x \gg 8 + x \gg 16 + x \gg 24 + x \gg 32.$$

Our algorithm calculates this value. (x+1 is used to allow for floor division).



Lower 16 bits output of y obtained on the FPGA board (10000110101111):