Verilog Assignment 3
Group Number: 23
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We have designed total 11 modules (other than the testbench):

1. cla (Carry lookahead adder): This takes two 8 bits numbers and adds them to give their 8 bit sum and carry out.
2. complementor: To find 2s complement of in2.
3. subtractor: To calculate in1-in2. Used cla with in1 and complement of in2.
4. select (display): To reroute in1 as output.
5. leftshift: To provide in1<<1 as output. Used cla to provide (in1+in1) as output.
6. rightshift: To provide in1>>1 as output.
7. and_op: To provide AND of in1 and in2 in the output.
8. not_op: To provide NOT of in1 in output.
9. or_op: To provide OR of in1 and in2 in the output.
10. my_decoder: To convert 3 bit select input to 8 bit enable output.
11. top_module: To provide output as per the select line by first calling decoder and then calling other modules using each bit of enable.