UNIVERSITÉ Concordia UNIVERSITY
GINA CODY
SCHOOL OF ENGINEERING
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Chapter 1

Part I

Computer Abstractions and Technology

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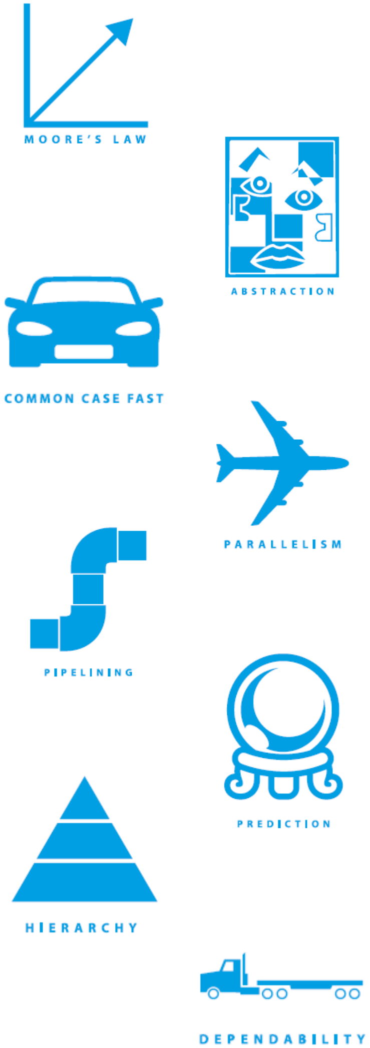
COEN: 316

[Based on Figures from *Computer Organization and Design*: *The Hardware/Software Interface* Patterson & Hennessy, 5th ed. © 2014 Elsevier Inc.
&
Computer Organization and Architecture: *Designing for Performance* William Stallings, 8th ed. © 2010 Pearson Education Inc.]

Department of Electrical & Computer Engineering (ECE)

Eight Great Ideas

- Design for ***Moore's Law***
- Use ***abstraction*** to simplify design
- Make the ***common case fast***
- Performance *via* ***parallelism***
- Performance *via* ***pipelining***
- Performance *via* ***prediction***
- ***Hierarchy*** of memories
- ***Dependability*** *via* redundancy



Eight Great Ideas: Example

- Match the following ideas from other fields to those from computer architecture
  - Assembly lines in automobile manufacturing

    Performance via Pipelining
  - Suspension bridge cables

    Dependability via Redundancy
  - Aircraft and marine navigation systems that incorporate wind information

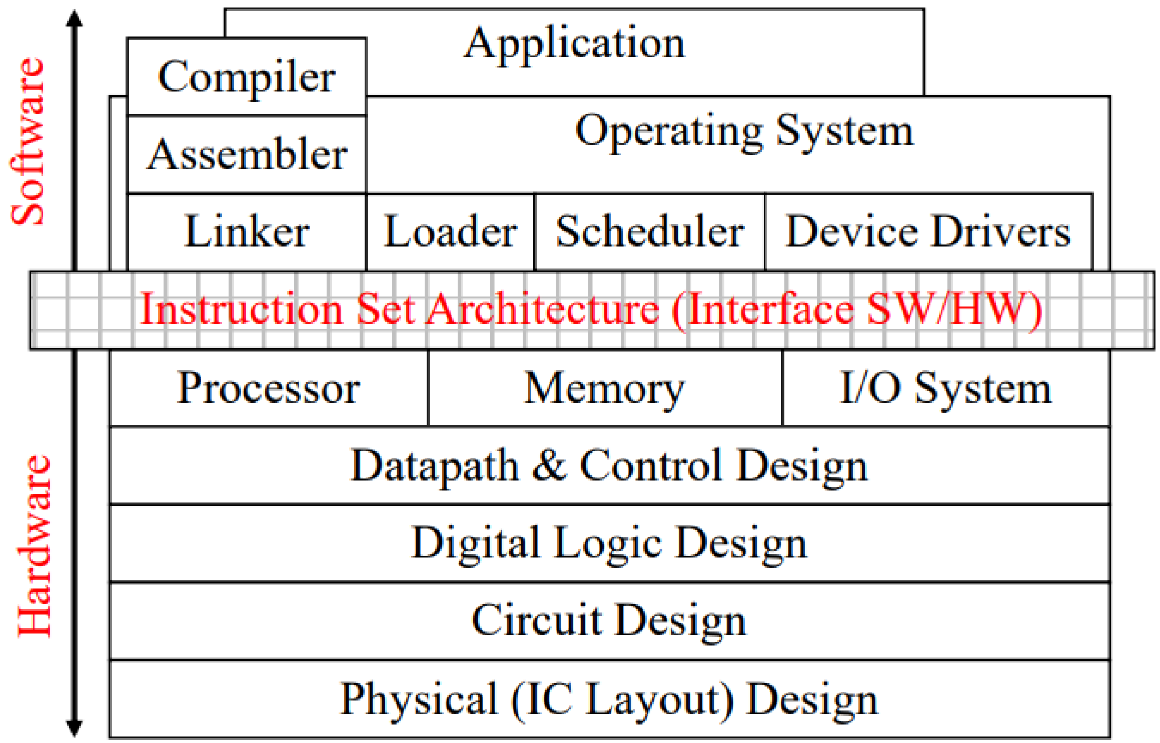
    Performance via Prediction
  - Express elevators in buildings

    Make the Common Case Fast
  - Library reserve desk

    Hierarchy of Memories
  - Adding electromagnetic aircraft catapults, allowed by the increased power generation offered by the new reactor technology

    Design for Moore’s Law

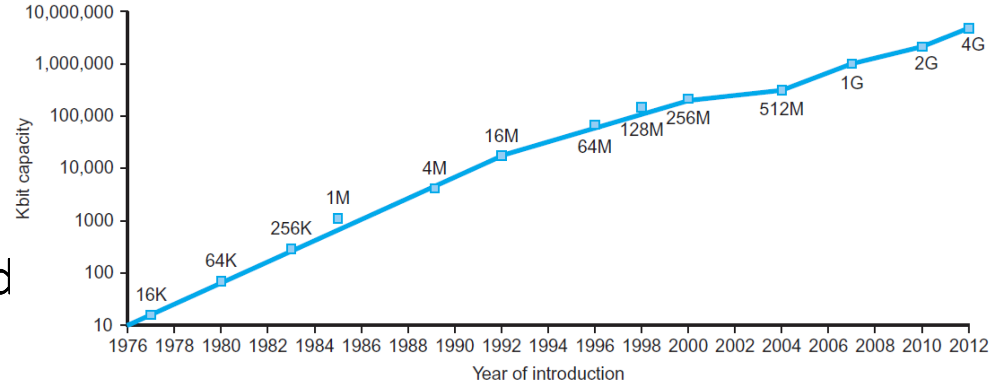
Abstractions



- Abstraction helps us deal with complexity (hide lower-level details)
- Instruction set architecture (ISA) (the hardware/software interface)
- Implementation (the details underlying and interface)

Technology Trends

- Electronics technology continues to evolve
  - Increased capacity and performance
  - Reduced cost



DRAM capacity

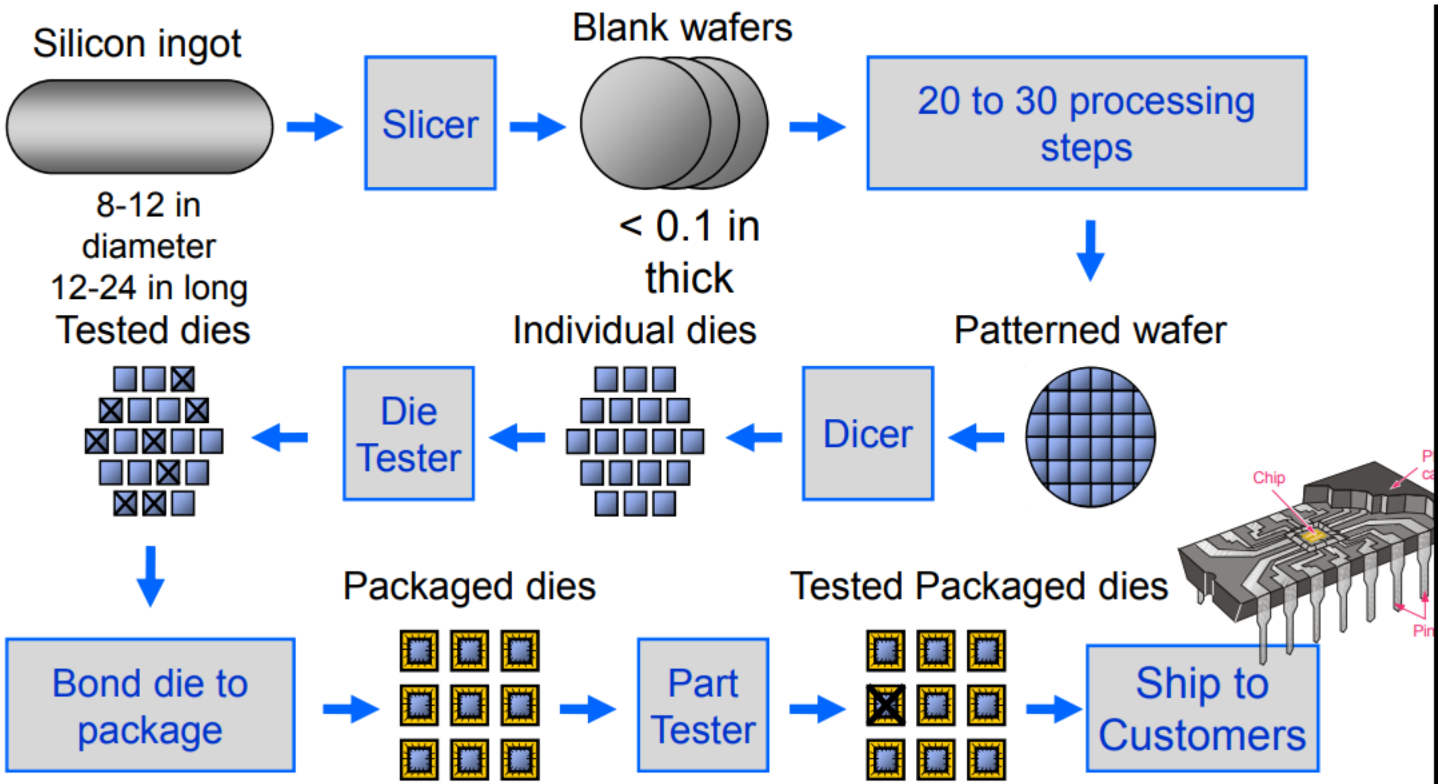
Year	Technology	Relative performance/cost
1951	Vacuum tube	1
1965	Transistor	35
1975	Integrated circuit (IC)	900
1995	Very large scale IC (VLSI)	2,400,000
2013	Ultra large scale IC	250,000,000,000

Semiconductor Technology

- Silicon
  - Semiconductors
- Add materials to transform properties
  - Conductors
  - Insulators
  - Switch

Manufacturing ICs

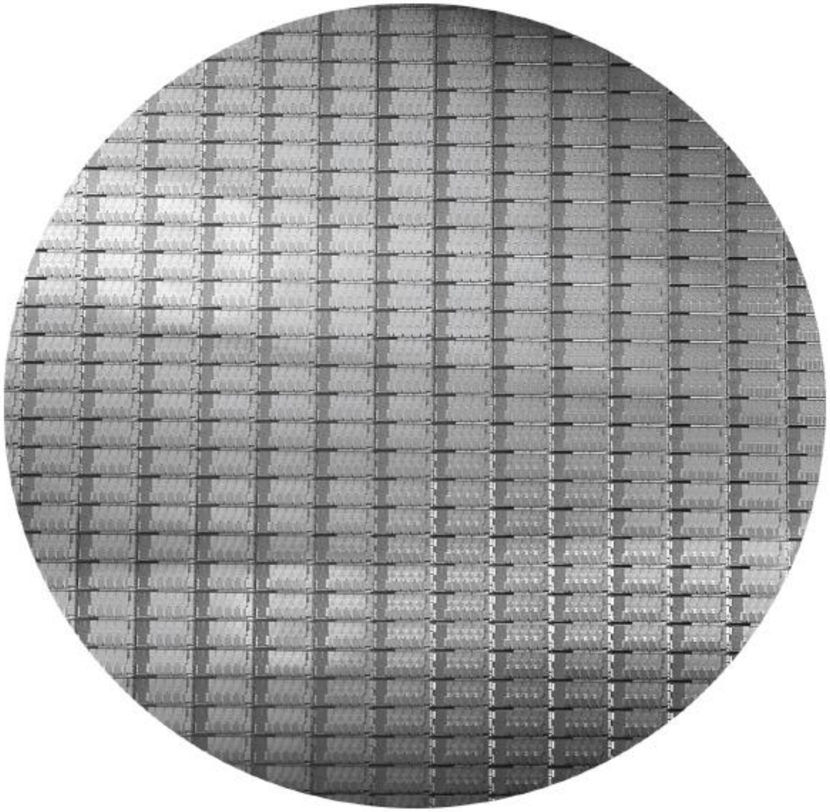
https://www.youtube.com/watch?v=aWVywhzuHnQ



- Yield: proportion of working dies per wafer

Intel Core i7 Wafer

- 300mm wafer, 280 chips, 32nm technology
- Each chip is 20.7 × 10.5 mm



Integrated Circuit Cost

$$\text{Cost per die} = \frac{\text{Cost per wafer}}{\text{Dies per wafer} \times \text{Yield}}$$

$$\text{Dies per wafer} \approx \text{Wafer area}/\text{Die area}$$

$$\text{Yield} = \frac{1}{(1+(\text{Defects per area} \times \text{Die area}/2))^2}$$

- Nonlinear relation to area and defect rate
  - Wafer cost and area are fixed
  - Defect rate determined by manufacturing process
  - Die area determined by architecture and circuit design
  - Dramatic decrease in yield with larger dies

Integrated Circuit Cost: Example (1/2)

- The table below shows manufacturing data for two processors, A and B
  - Find the yield for each processor
  - Find the cost per die for each processor

	Wafer diameter	Dies per Wafer	Defects per Unit area	Cost Per Wafer
A	15 cm	84	0.020 defects/cm^2	12
B	20 cm	100	0.031 defects/cm^2	15

Integrated Circuit Cost: Example (2/2)

- Solution

$$\text{Die\_area}_{15cm} = \text{Wafer\_area/Dies\_per\_wafer} = 3.14 * 7.5^2 / 84 = 2.10\,\text{cm}^2$$

$$\text{Yield}_{15cm} = 1/(1 + (0.020 * 2.10/2))^2 = 0.9593$$

$$\text{Die\_area}_{20cm} = \text{Wafer\_area/Dies\_per\_wafer} = 3.14 * 10^2 / 100 = 3.14\,\text{cm}^2$$

$$\text{Yield}_{20cm} = 1/(1 + (0.031 * 3.14/2))^2 = 0.9093$$

$$\text{Cost\_per\_die}_{15cm} = 12/(84 * 0.9593) = 0.1489$$

$$\text{Cost\_per\_die}_{20cm} = 15/(100 * 0.9093) = 0.1650$$

Summary

- Cost/performance is improving
  - Due to underlying technology development
- Hierarchical layers of abstraction
  - In both hardware and software