 <b>Integrated Solutions Technology, Inc.</b>	<b>Title</b>  <b>IST3032 Specification</b>  240 High Voltage Common STN Driver	文件編號 DOC#	版次 Rev
		IST-RD-0004	<b>005</b>
		生效日期 Effective Date : 3/19/2008	

# Specification

Written by Department	Written by / Date	Approved by QRA Manager	Issued by D.C.C.
Research & Development	Martin Chen 3/19/2008	Bonnie Lee 3/19/2008	Allan Haung 3/19/2008


Controlled by DCC

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文件變更履歷頁

Document Change History

版次 Rev.	變更項次 Change Items#	變更內容簡述 Change Description	變更依據文件號碼 ECN #	生效日期 Eff. Date
001	-	New Release		Jun./19/'01
002		P2: correct block diagram P4: correct VEO item P7: V0=2.7 to 5.5V-> 2.6 to 4.5V P9: correct timing chart P10: modify notes1,3	E10010008	10/23/2001
003		P13: PAD CONFIGURATION P14: COG Align Key Coordinate P15-P20:PAD CENTER OORDINATES	E01020011	1/28/2002
004		P10:Current consumption (1)LCC1:TBD =>typ/max = 10/40uA (2)LCC2:TBD =>typ/max = 20/50uA (3)ILCD:TBD=>typ/max = 20/50uA P13: Add pin101 to pin105	E03040003	3/25/2004
005		P6: Application Example x1 to x240→x240 to x1	E03080004	3/19/2008
接續頁 CONTINUATION --- <input type="checkbox"/> 是 YES; <input checked="" type="checkbox"/> 否 NO				



## High - Voltage 240 - Channel Common Driver for Dot - Matrix STN LCD

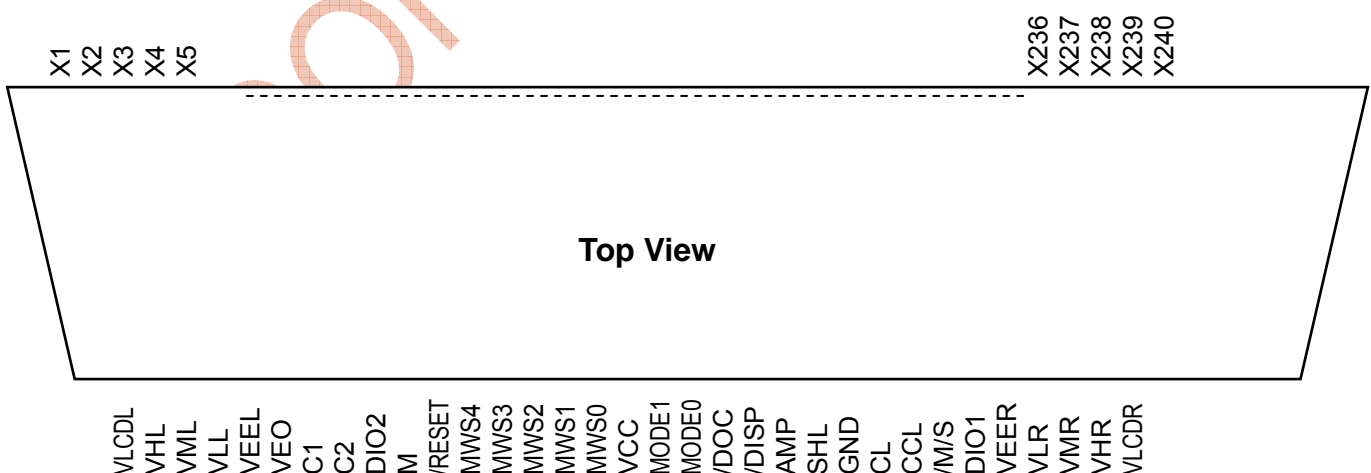
### Description

The IST3032 is a 240-channel common driver which drives a dot matrix STN liquid – crystal panel. By changing the mode, this can be applied to 240-and 200- and 160- channel output. Through the use of a 40V high-voltage CMOS process technology, a high-voltage drive of +20 V and –20 V, centering on VM is possible. -20 V is generated from max +20 V with built-in switching circuit and external capacity. 3 V is used for logic drive. This device is used together with the segment driver IST3031.

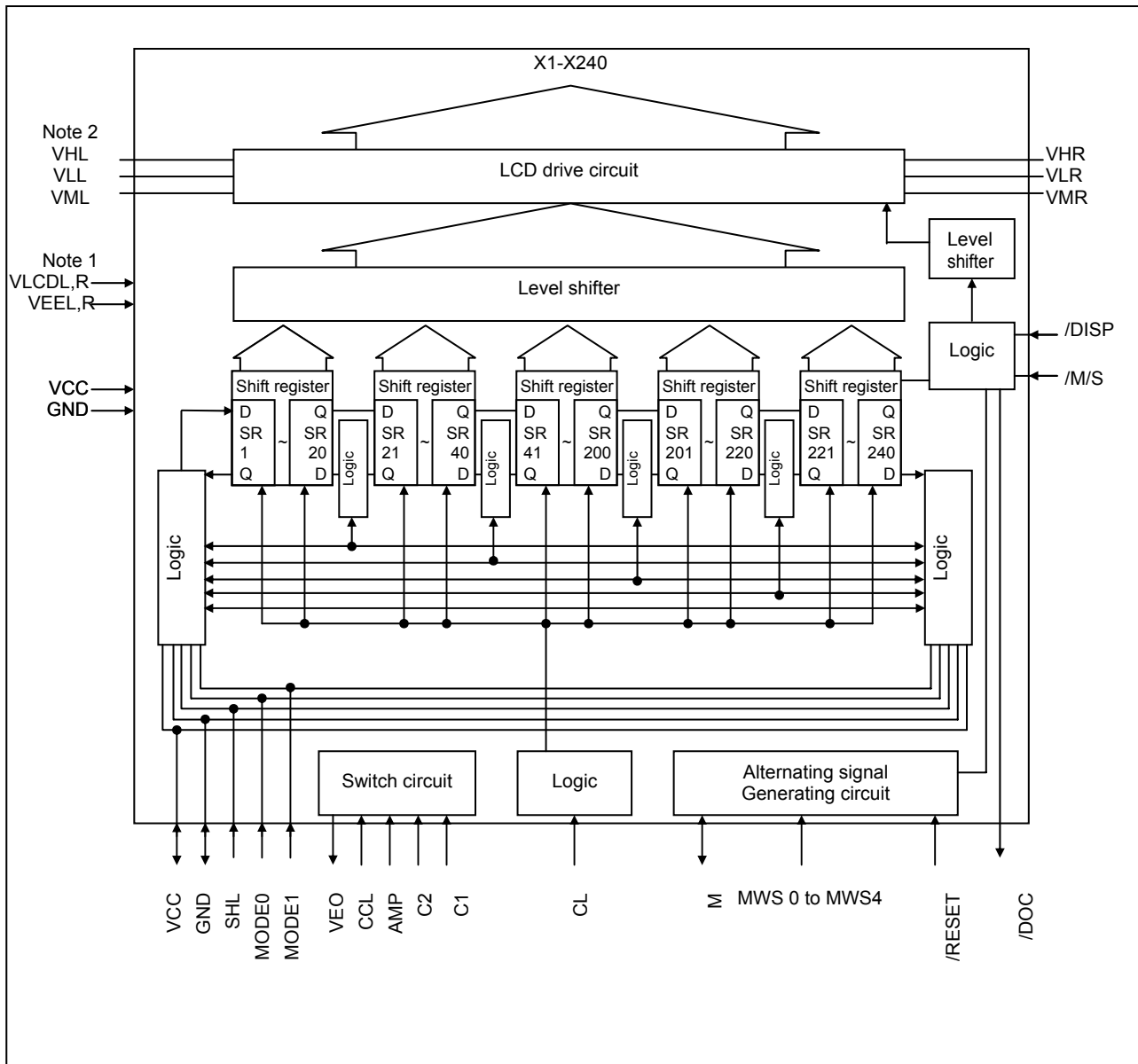
### Features

- Display duty: Up to 1 / 240
- LCD drive voltage: 40 V max
- Built-in switching circuit (to generate –20V)
- Number of LCD drive circuit: 240
- Operating voltage: 2.5 to 5.5 V
- Intermediate voltage I/F
- Built-in alternating signal generation circuit
- Pin programmable
- Output mode change: 240-output mode  
200-output mode  
160-output mode
- Built-in display-off function
- Flex TCP

### Pin Arrangement



Note: The shape above does not indicate the actual outline.



\*1 VLCDL and VLCDR, and VEEL and VEER are internally connected.

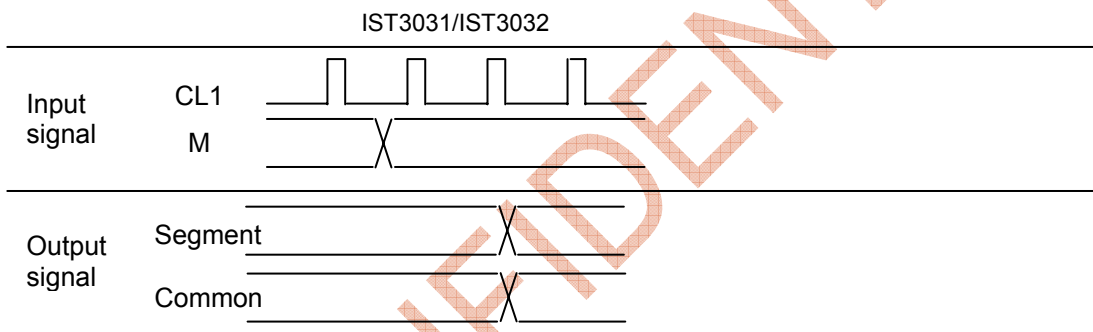
\*2 VHL and VHR, VLL and VLR, and VML and VMR are internally connected.



### Internal Block Diagram

1. LCD drive circuit  
This circuit selects and outputs the three level signals for the LCD drive. By a combination of the data in the shift register and M, either VH, VL, or VM is selected and transmitted to the output circuit.
2. Level shifter  
This boosts a 5V signal to a high-voltage signal for LCD drive.
3. Shift register  
This is a 240-bit bi-directional shift register circuit. The first line marker signal output from the DIO1 pin and DIO2 pin is sequentially shifted by shift clock CL. The shift direction is determined by the SHL pin.
4. Alternating signal generating circuit  
This circuit generates an alternating signal, M signal for LCD display. To suppress cross-talk, the signal is alternated in a unit from several lines to several tens of lines. By connecting MWS0 to MWS4 pins to Vcc or GND, the desired number of signals can be alternated. When alternating signals are externally input, all pins, MWS0 to MWS4 are connected to GND.

### HIGH VOLTAGE driver timing





## Pin Functions

Classification	Symbol	Connected to	I / O	Functions																																																													
Power supply	VLCDL, R VEEL, R VCC GND	Power supply	-	VLCDL, R – VEEL, R : Power supply for LCD drive VLCDL, R : Power supply for switch circuit VCC – GND : Power supply for logic circuit																																																													
	VHL, R VLL, R VML, R	Power supply	Input	Power supply for LCD drive level VHL, R : selected level ; Set to the same voltage as VLCDL, R. VLL, R : selected level ; set to the same voltage as VEEL, R. VML, R : Non-selected level and Power supply for switch circuit																																																													
	VEO	VEEL, R	output	When using built-in switching circuit and generate VEE, VEO pin should be connect to VEEL, R pins. VM voltage is point of reference. VLCD – voltage is reversed and output as VEE. If built-in switching circuit is not used, don't connect any lines to this pin.																																																													
	C1, C2	Capacitance	-	External capacitance should be connected when using the switch circuit for generate VEE. If built-in switching circuit is not used, don't connect any lines to this pin.																																																													
Control signal	CL	MPU	Input	Shift clock input data is shifted at the falling edge of shift clock, CL of the shift register.																																																													
	M	Extension driver or MPU	I/O	Inputs or outputs the alternating current for LCD drive output.																																																													
	MWS0 MWS1 MWS2 MWS3 MWS4	-	Input	<div>This pin specifies the cycle of the alternating signal, M signal in the unit of the number of lines. The number of lines, which is an integer from 2 to 31, is specified as follows. Usually, specify the number of lines within a range from 10 to 31. When the IST3032 is driven by an external alternating signal, specify the number of lines as zero.</div> <table><thead><tr><th>Number of lines</th><th>MWS 4</th><th>MWS 3</th><th>MWS 2</th><th>MWS 1</th><th>MWS 0</th><th>Line alternating waveform</th><th>M-pin status</th></tr></thead><tbody><tr><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>-</td><td>Input</td></tr><tr><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>Prohibited</td><td rowspan="4">Output</td></tr><tr><td>2</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>2 lines alternated</td></tr><tr><td>3</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td>3 lines alternated</td></tr><tr><td>⋮</td><td>⋮</td><td>⋮</td><td>⋮</td><td>⋮</td><td>⋮</td><td>⋮</td></tr><tr><td>31</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>31 lines alternated</td><td></td></tr><tr><td colspan="8">1 = "Vcc", 0 = "GND"</td></tr></tbody></table>	Number of lines	MWS 4	MWS 3	MWS 2	MWS 1	MWS 0	Line alternating waveform	M-pin status	0	0	0	0	0	0	-	Input	1	0	0	0	0	1	Prohibited	Output	2	0	0	0	1	0	2 lines alternated	3	0	0	0	1	1	3 lines alternated	⋮	⋮	⋮	⋮	⋮	⋮	⋮	31	1	1	1	1	1	31 lines alternated		1 = "Vcc", 0 = "GND"							
	Number of lines	MWS 4	MWS 3	MWS 2	MWS 1	MWS 0	Line alternating waveform	M-pin status																																																									
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	1	0	0	0	0	1	Prohibited	Output																																																									
	2	0	0	0	1	0	2 lines alternated																																																										
	3	0	0	0	1	1	3 lines alternated																																																										
	⋮	⋮	⋮	⋮	⋮	⋮	⋮																																																										
	31	1	1	1	1	1	31 lines alternated																																																										
1 = "Vcc", 0 = "GND"																																																																	
MODE0 MODE1	-	Input	<div>Switch terminals for the number of LCD drive output pins</div> <table><thead><tr><th>MODE 0</th><th>MODE 1</th><th>Shift direction</th></tr></thead><tbody><tr><td>"H"</td><td>"H"</td><td>240-output (X1,X2,X3.....X238,X239,X240)</td></tr><tr><td>"H"</td><td>"L"</td><td>200-output (X21,X22,X23.....X218,X219,X220)</td></tr><tr><td>"L"</td><td>"H"</td><td>160-output (X41,X42,X43.....X198,X199,X200)</td></tr><tr><td>"L"</td><td>"L"</td><td>Prohibited</td></tr></tbody></table>	MODE 0	MODE 1	Shift direction	"H"	"H"	240-output (X1,X2,X3.....X238,X239,X240)	"H"	"L"	200-output (X21,X22,X23.....X218,X219,X220)	"L"	"H"	160-output (X41,X42,X43.....X198,X199,X200)	"L"	"L"	Prohibited																																															
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"L"	"L"	Prohibited																																																															
DIO1 DIO2	Extension driver or MPU	I/O	<div>Serial data input/output pin; input/output pins for sift register</div> <table><thead><tr><th>SHL</th><th>DIO1</th><th>DIO2</th></tr></thead><tbody><tr><td>"H" level</td><td>serial output pin</td><td>serial input pin</td></tr><tr><td>"L" level</td><td>serial input pin</td><td>serial output pin</td></tr></tbody></table>	SHL	DIO1	DIO2	"H" level	serial output pin	serial input pin	"L" level	serial input pin	serial output pin																																																					
SHL	DIO1	DIO2																																																															
"H" level	serial output pin	serial input pin																																																															
"L" level	serial input pin	serial output pin																																																															
CCL	MPU	Input	Built-in switching circuit clock input. When using built-in switching circuit and generating VEE, this pin connect CL pin. If built-in switching circuit is not used, CCL must be fixed to GND																																																														
AMP	VCC Or GND	Input	Built-in switching circuit on-off control When using built-in switching circuit, this pin must be fixed to VCC. If built-in switching circuit is not used, this pin must be fixed to GND																																																														

## Pin Functions (cont)

Classification	Symbol	Connected to	I / O	Functions
Control signal	/RESET	MPU or VCC	Input	Setting this pin to GND initializes the alternating signal (M signa) circuit. A VCC level RESET is nomally used.
	/DISP	MPU	Input	Setting this pin to GND sets LCD drive output X1 to X240 to the VM level.
	/M/S	-	Input	Controls the display-off function. And display-off signal output from /DOC pin
				/M/S                      /DISP pin state and functions
				"H"level                  When /DISP is low level. X1-240 set VM level "L"level                  Until 16 times serial data is input into DIO, X1-X240 set VM level.
	/DOC	-	Output	/M/S                      /DOC
				"H"level                  When /DISP is low level, output low level When /DISP is high level, output high level
				Until 16 times serial data is input, output low level /DISP DIO1,2 /DOC
				When using M/S is low level, /DOC pin should be connected to SEG LSI Dispoff control pin.
	SHL	-	Input	This pin switches shift register directions.
				SHL   MODE0   MODE1                      Shift direction
				Right shift
				"H"level                  "H"                  "H"                  DIO2→SR1→.....→SR240→DIO1
				"H"level                  "H"                  "L"                  DIO2→SR21→.....→SR220→DIO1
				"L"level                  "L"                  "H"                  DIO2→SR41→.....→SR220→DIO1
				Left shift
				"H"level                  "H"                  "H"                  DIO1→SR240→.....→SR1→DIO2
				"H"level                  "H"                  "L"                  DIO1→SR220→.....→SR21→DIO2
				"L"level                  "L"                  "H"                  DIO1→SR200→.....→SR41→DIO2
				SR1, SR2...SR240 correspond to X1, X2...X240. Note: The 40 or 80 pins invalidated at the 200-output or 160-output mode output the non-selected level synchronized with M signal; These pins should be used open.
LCD drive output	X1 to X240	LCD	Output	LCD drive output By a combination of the display data and the M signal, when /DISP is set to Vcc, either VH, VL, or VM is selected and transmitted to the output circuit.  

Note: Configuring the LCD panel using the IST3032 when using the select SEGMENT driver.  
The select SEGMENT driver.

SEGMENT	Select
IST3031(320OUT)	<input type="radio"/>

## Application Example

Figure 1 shows an application example of 320 x 3(color) x 240 dot Quarter VGA Size STN color panel.

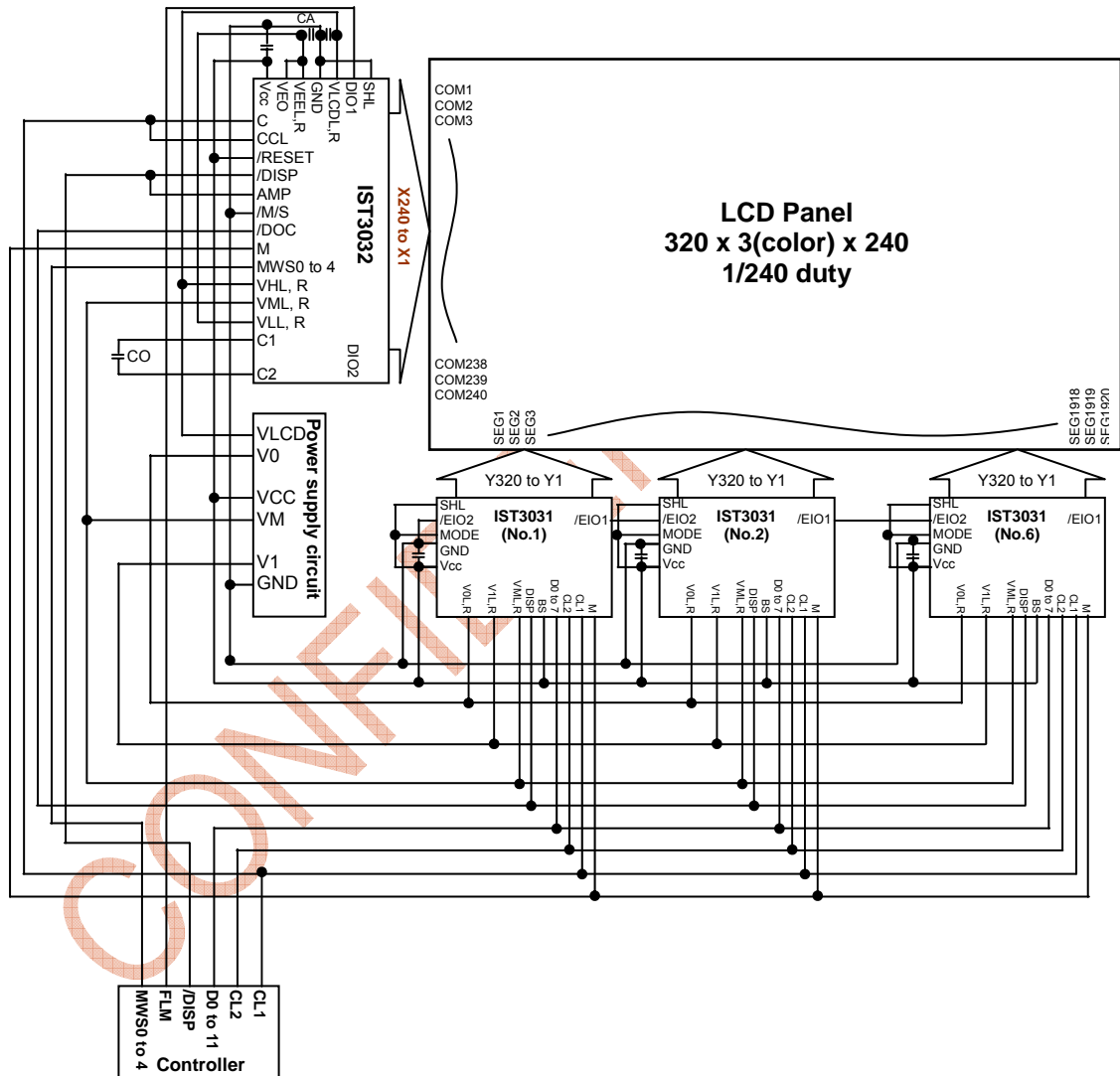
This panel consist on IST3032 x 1 piece and IST3031 x 3 pieces.

IST3032 generate M signal and D<sub>OC</sub> signal. M signal pin is connected M signal pin of IST3031

and DOC signal pin is connected DISP signal pin of IST3031

IST3032 is able to generates minus voltage by external capacitor, CO.

VEO pin is connected VEE pin VL pin.



### Figure 1 Application Example

Note:

1. When designing the board, connect a capacitor near the IC to stabilize power supply. Use two capacitors of about 0.1  $\mu\text{F}$  for each IC, between Vcc and GND, V0 and GND, VLCD and GND, and VEE and GND.
2. In addition, for the power supply circuit, connect a capacitor of several  $\mu\text{F}$  or several tens of  $\mu\text{F}$  between the drive power supply and level power supply in the period between when the liquid-crystal drive power supply is turned on and when it is turned off.
3. when using external capacitor, CO to generate VEE, connect a capacitor of several  $\mu\text{F}$  or several tens of  $\mu\text{F}$  between the VEE and GND.





## Power Supply Circuit Example

### Figure 2 Shows power supply circuits example

By using 3 level power supply output DC-DC converter, LCD power supply circuit is established without minus voltage power supply.

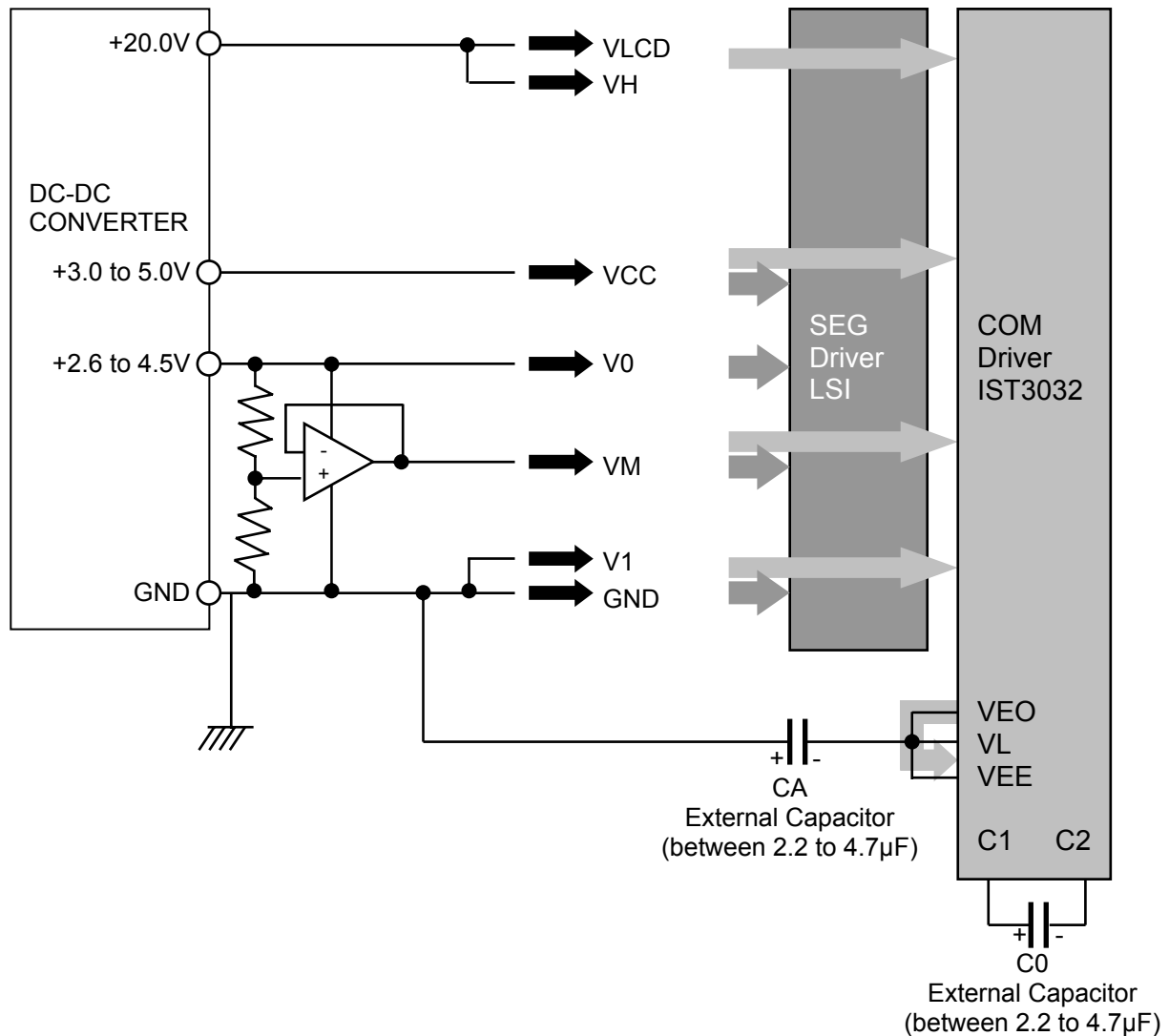



Figure 2 Power Supply Circuits Example

**Absolute Maximum Ratings**

Items		Symbol	Ratings	Unit	Note
Power supply voltage	Logic circuit	VCC	-0.3 to +7.0	V	*1, *8
	LCD drive circuit	VLCD	-0.3 to +25.0	V	*1, *3, *8
		VEE	-20.0 to +0.3	V	*1, *4, *8
Input voltage (1)		VT1	-0.3 to VCC +0.3	V	*1, *2
Input voltage (2)		VH	-0.3 to VLCD	V	*1, *5, *8
Input voltage (3)		VL	-0.3 to +VEE	V	*1, *6, *8
Input voltage (4)		VM	-0.3 to +5.0	V	*1, *7, *8
Operating temperature		Topr	-30 to +75	°C	
Storage temperature		Tstg	-55 to +110	 °C	

Note: If the LSI is used beyond the above maximum ratings, it may be permanently damaged.

It should always be used within its specified operating range for normal operation to prevent malfunction or degraded reliability.

\*1 The reference point is GND (0V).

\*2 Applies to DIO1, /DISP, SHL, M, NWS0, NWS1, NWS2, NWS3, NWS4, /RESET, MODE0, MODE1, CL, /M/S, AMP, CCL, DIO2\*3 Applies to VLCDL, R pin.

\*4 Applies to VHL, R pin.

\*5 Applies to VEEL, R pin.

\*6 Applies to VLL, R pin.

\*7 Applicable to VML, R pins.

(Caution)

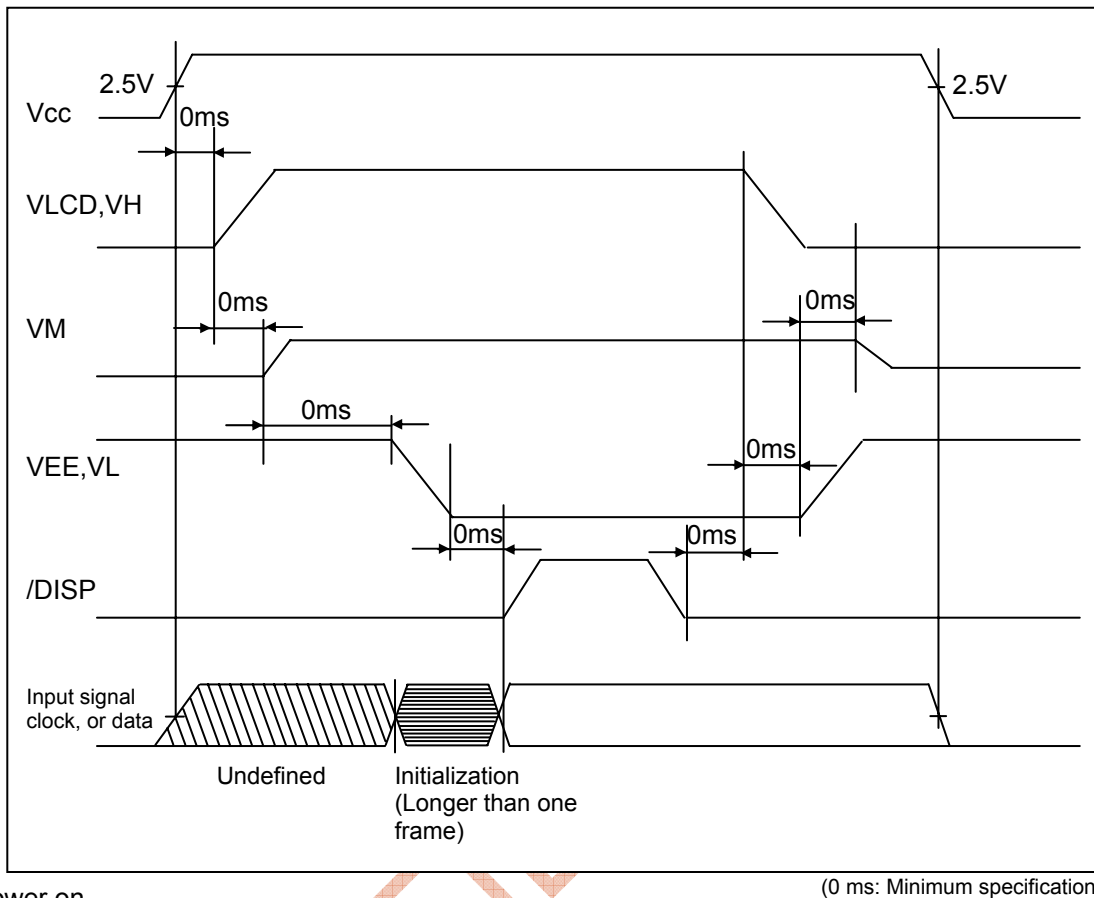
Operating the LSI in excess of the absolute maximum rating will result in permanent damage.

Use the LSI observing electrical characteristic conditions in normal operation. Exceeding the conditions will cause malfunctions or will affect LSI reliability.

\*8 Follow the sequence of activation and inactivation for the following power supplies and signals.

And this sequence should be applied when using built-in switching circuit.

If the sequence is not followed, it may cause LSI malfunction, permanent damage, or adverse effects.



## 8.1 Power on

- (1) Turn on the power supply in the order of GND-VCC, GND-VLCD (VH), and VM. VM-VEE is generated automatically. In this case, input GND to the /DISP pin.
- (2) The LCD level forcibly outputs the VM level by the DISPOFF function.
- (3) The DISPOFF function has a priority even if input signal distortion occurs immediately after VCC input.
- (4) Then input the predetermined signals to initialize the driver registers. In this case, assure a period for more than one frame.
- (5) Preparation for normal display is thus completed. Cancel the DISPOFF function by setting the /DISP pin to VCC. At this point, the levels of VEE (VL), VLCD (VH) and VM must have reached the predetermined respective voltage.

## 8.2 Shut down

As a rule, shut down should be in the opposite order that is used for power on.

- (1) Set the /DISP pin to GND.
- (2) At first shut off the LCD power supply GND-VLCD (VH). At the same time VM-VEE (VL) automatically get to VM level. Next shut off the VM.
- (3) Set VCC and the input signal to GND.

At this point, VEE (VL), VLCD (VH) and VM pin input must completely drop to 0 V.

Since the DISPOFF function is inactivated when the VCC level drops to GND, the LCD output may output a level other than VM. Therefore, an incorrect display may appear at shut down or power on.



## Electrical Characteristics

DC Characteristics 1 (VCC= 2.5 to 5.5V, GND = 0V, VLCD - VEE = 15 to 40V, Ta = -30 to +75°C)

Item	Symbol	Applicable Pins	min.	typ.	max	Unit	Conditions	Notes
Input high level voltage	ViH	DIO1,/DISP,SHL,M,/M/S,MWS 0 to 4,RESET,CL,MODE0,MODE1,/DOC,AMP,CCL,DIO2	0.7xVCC	-	VCC	V		
Input low level voltage	ViL		0	-	0.3xVCC	V		
Output high level voltage	VOH	M,/DOC,DIO1,DIO2	VCC-0.4	-	-	V	IOH=-0.4mA	
Output low level voltage	VOL	M,/DOC,DIO1,DIO2	-	-	0.4	V	IOL=0.4mA	
On resistance between Vi-Xj	RON	X1 to Y240, V pin	-	0.7	2.0	KΩ	ION=150μA	*1
Input leak current (1)	LiL1	DIO1,/DISP,SHL,M,/M/S,MWS 0 to 4,/RESET,CL,MODE0,MODE1,/DOC,AMP,CCL,DIO2	-5	-	5	μA	VIN=VCC to GND	
Input leak current (2)	LiL2	VH,VL,VM,C1,C2	-25	-	25	μA		
Current consumption (1)	LCC1	VCC	-	10	40	μA	VCC=3.3V,VLCD-VEE=40V fCL=19.2kHz,fM=1.5kHz	
Current consumption (2)	LCC2	VCC	-	20	50	μA	VCC=5.0V,VLCD-VEE=40V fCL=19.2kHz,fM=1.5kHz	
Current consumption (2)	ILCD	CLCD	-	25	50	μA	VCC=3.3V,VLCD-VEE=40V fCL=19.2kHz,fM=1.5kHz	*2

\*1 Indicates the resistance between one of the pins X1-X240 and one of the voltage supply pins VH, VL, or VM, When load current is applied to the X pin; defined under the following conditions:

VLCD=VH=22.75V, VEE=VL=-17.25V, VM=2.75V, and GND=0V.

VH, VL, and VM voltage must be within VLCD-VM ≥ VH-VM =21.5 to 7.5V

VEE-VM ≤ VL-VM=-21.5 to -7.5V, 6.0 ≥ VM ≥ -0.3V, and VH > VM > VL.

\*2 Input and output currents are excluded. When a CMOS input is left floating, excess current flows from the power supply through the input circuit. To avoid this, ViH and ViL must be held at VCC and GND, respectively.

\*3 The voltage relationship of each signal is as follows:

Segment voltage	Segment waveform	Common waveform	Common voltage
VH (22.75 V)			VH (22.75 V)
V0 (4.5 V)			V0 (4.5 V)
VM (2.75 V)			VM (2.75 V)
V1(1.0V)			V1(1.0V)
			VL (-17.25V)



	Normal display period	Off-display period	Normal display period	Off-display period	
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AC characteristics (Common driver timing 1):(VCC = 2.5 to 5.5V, GND =V0, VLCD-VEE = 15 to 40V, Ta = -30 to +75°C)

Item	Symbol	Pin Name	Min	Max	Unit	Note
Clock cycle time	tCYC	CL	400	-	ns	
CL high-level width	tCWH	CL	25	-	ns	
CL low-level width	tCWL	CL	370	-	ns	
CL rising time	tr	CL	-	30	ns	
CL falling time	tf	CL	-	30	ns	
Data set-up time	tDS	DIO1, DIO2, CL	100	-	ns	
Data hold time	tDH	DIO1, DIO2, CL	10	-	ns	
Data output delay time	tDD	DIO1, DIO2, CL	-	150	ns	*1
M output delay time	tMD	M, CL	-	150	ns	*1
M setup time	tMS	M, CL	20	-	ns	
M hold time	tMH	M, CL	20	-	ns	
DOC delay time 1	tDOC1	/DISP, /DOC	-	300	ns	*2
DOC delay time 2	tDOC2	DIO1,DIO2,/DOC	-	300	ns	*2

AC characteristics (Common driver timing 2):(VCC = 2.5 to 4.5V, GND =V0, VLCD-VEE = 40V, Ta = -30 to +75°C)

Item	Symbol	Pin Name	Min	Max	Unit	Note
Output delay time 1	tpd1	X(n), M	-	1.2	μs	*2

AC characteristics (Common driver timing 3):(VCC = 4.5 to 5.5V, GND =V0, VLCD-VEE = 40V, Ta = -30 to +75°C)

Item	Symbol	Pin Name	Min	Max	Unit	Note
Output delay time 1	tpd1	X(n), M	-	0.7	μs	*2

Notes: \*1. Defined by connecting the load circuit shown in figure 4

\*2. Defined by connecting the load circuit shown in figure 4

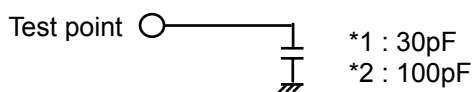
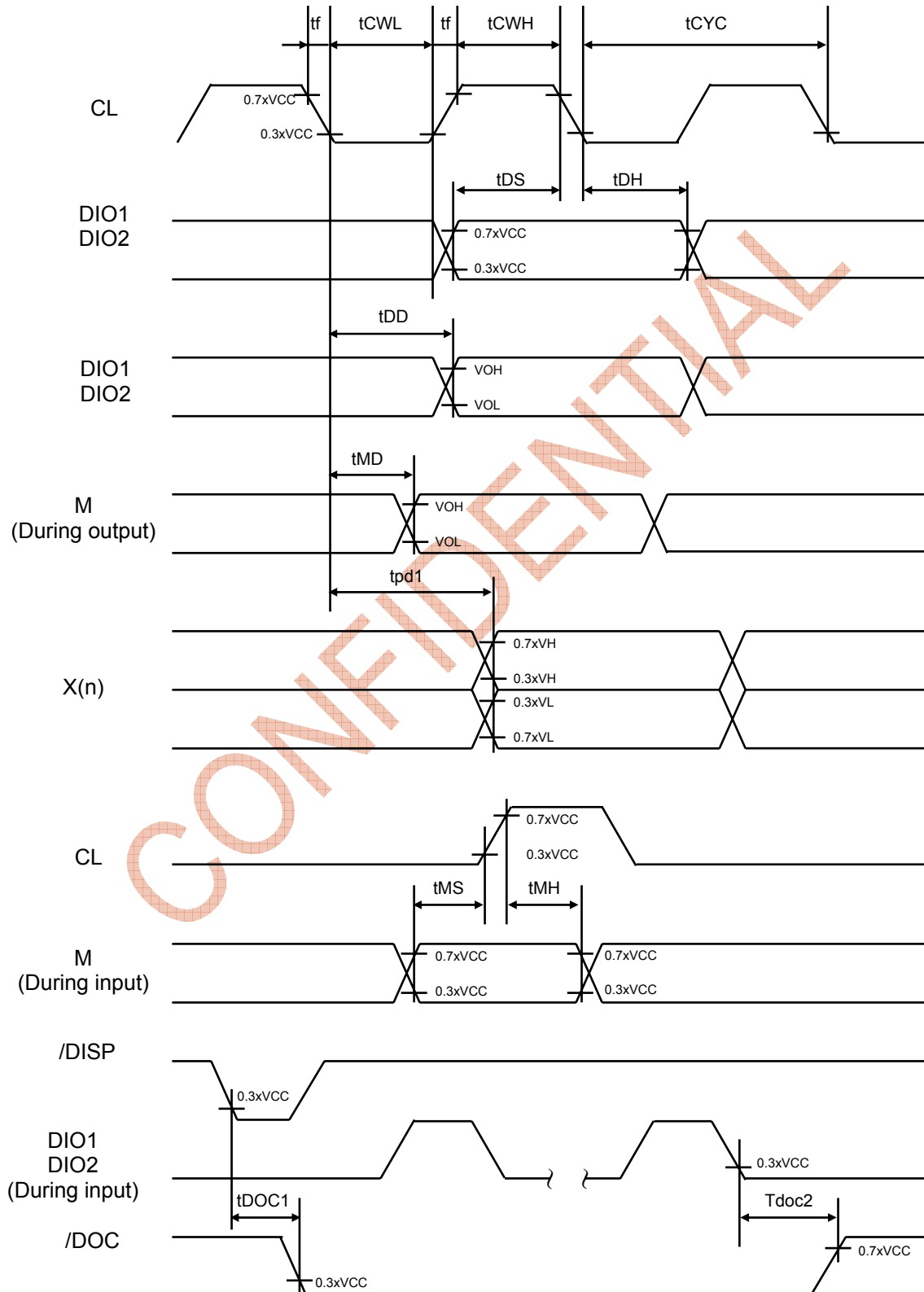
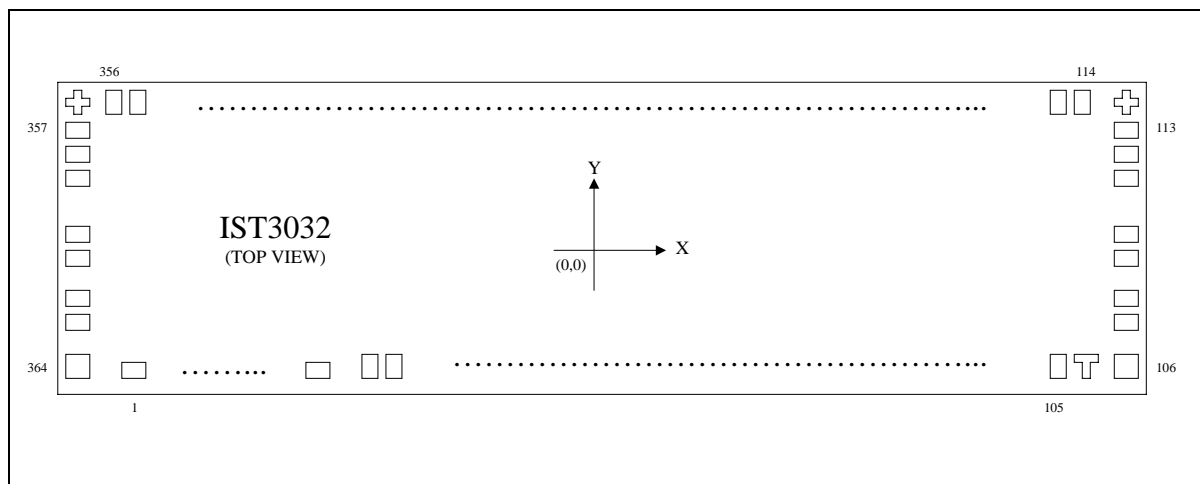


Figure 4 Load circuit





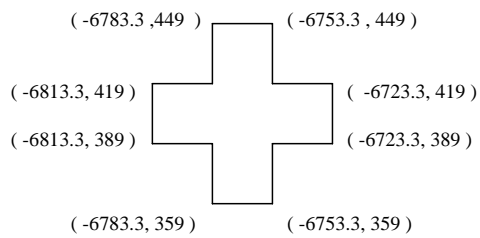
## PAD CONFIGURATION :



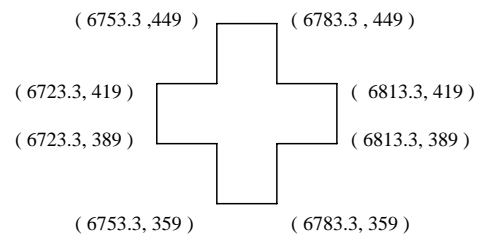


## COG Align Key Coordinate :

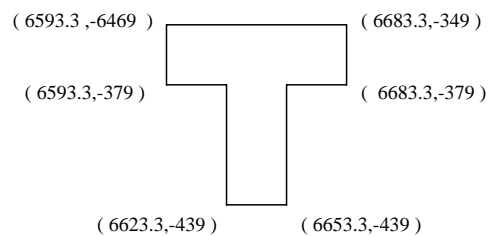
Left-Top



Right-Top



Right-Down





**PAD CENTER COORDINATES :****Table 2 : Pad Center Coordinates****Unit : um**

PAD NO	PAD NAME	COORDINATES		PAD NO	PAD NAME	COORDINATES	
		X	Y			X	Y
1	DUMMY	-6607.8	-420	31	VEO	-3447.6	-400
2	DUMMY	-6502.8	-420	32	C1	-3260.4	-400
3	DUMMY	-6397.8	-420	33	C1	-3200.4	-400
4	DUMMY	-6292.8	-420	34	C2	-3003.5	-400
5	DUMMY	-6187.8	-420	35	C2	-2943.5	-400
6	DUMMY	-6082.8	-420	36	DUMMY	-2723.5	-400
7	DUMMY	-5977.8	-420	37	DUMMY	-2663.5	-400
8	DUMMY	-5872.8	-420	38	DUMMY	-2515.5	-400
9	DUMMY	-5767.8	-420	39	DUMMY	-2455.5	-400
10	DUMMY	-5662.8	-420	40	GNDC	-2340	-400
11	DUMMY	-5557.8	-420	41	DIO2	-2127.5	-400
12	DUMMY	-5452.8	-420	42	DIO2	-2067.5	-400
13	DUMMY	-5347.8	-420	43	M	-1887.9	-400
14	DUMMY	-5242.8	-420	44	M	-1827.9	-400
15	DUMMY	-5137.8	-420	45	RESETB	-1631.7	-400
16	DUMMY	-5032.8	-420	46	RESETB	-1571.7	-400
17	DUMMY	-4927.8	-420	47	GNDC	-1432.4	-400
18	DUMMY	-4822.8	-420	48	MWS4	-1219.9	-400
19	DUMMY	-4717.8	-420	49	MWS4	-1159.9	-400
20	DUMMY	-4612.8	-420	50	GNDC	-1020.6	-400
21	DUMMY	-4507.8	-420	51	VDDC	-851.7	-400
22	DUMMY	-4402.8	-420	52	MWS3	-634	-400
23	DUMMY	-4297.8	-420	53	MWS3	-574	-400
24	DUMMY	-4192.8	-420	54	GNDC	-434.7	-400
25	DUMMY	-4087.8	-420	55	VDDC	-265.8	-400
26	DUMMY	-3982.8	-420	56	MWS2	-48.1	-400
27	DUMMY	-3877.8	-420	57	MWS2	11.9	-400
28	DUMMY	-3772.8	-420	58	GNDC	151.2	-400
29	DUMMY	-3667.8	-420	59	VDDC	320.1	-400
30	VEO	-3507.6	-400	60	MWS1	537.8	-400



Table 2 : Pad Center Coordinates ( Continued )

Unit : um

PAD NO	PAD NAME	COORDINATES		PAD NO	PAD NAME	COORDINATES	
		X	Y			X	Y
61	MWS1	597.8	-400	96	VDDC	5637	-400
62	GNDC	737.1	-400	97	DIO1	5789.6	-400
63	VDDC	906	-400	98	DIO1	5849.6	-400
64	MWS0	1128.5	-400	99	VDDC	5993.9	-400
65	MWS0	1188.5	-400	100	GNDC	6161.6	-400
66	GNDC	1327.8	-400	101	DUMMY	6315	-400
67	VDD	1496.7	-400	102	DUMMY	6375	-400
68	VDD	1670.8	-400	103	DUMMY	6435	-400
69	VDD	1844.9	-400	104	DUMMY	6495	-400
70	MODE1	2062.6	-400	105	DUMMY	6555	-400
71	MODE1	2122.6	-400	106	DUMMY	6774.3	-408
72	GNDC	2261.9	-400	107	VEER	6774.3	-250.4
73	MODE0	2474.4	-400	108	VLR	6774.3	-190.4
74	MODE0	2534.4	-400	109	VMR	6774.3	-60.6
75	VDDC	2678.7	-400	110	VMR	6774.3	-0.6
76	DOCB	2896.4	-400	111	VHR	6774.3	201.7
77	DOCB	2956.4	-400	112	VLCDR	6774.3	261.7
78	DISPOFFB	3144.3	-400	113	DUMMY	6774.3	321.7
79	DISPOFFB	3204.3	-400	114	DUMMY	6637.8	410
80	GNDC	3343.6	-400	115	X240	6582.8	410
81	AMP	3556.1	-400	116	X239	6527.8	410
82	AMP	3616.1	-400	117	X238	6472.8	410
83	VDDC	3760.4	-400	118	X237	6417.8	410
84	SHL	3978.1	-400	119	X236	6362.8	410
85	SHL	4038.1	-400	120	X235	6307.8	410
86	GND	4177.4	-400	121	X234	6252.8	410
87	GND	4336.4	-400	122	X233	6197.8	410
88	GND	4495.5	-400	123	X232	6142.8	410
89	CL	4708	-400	124	X231	6087.8	410
90	CL	4768	-400	125	X230	6032.8	410
91	CCL	4955.9	-400	126	X229	5977.8	410
92	CCL	5015.9	-400	127	X228	5922.8	410
93	GNDC	5220.1	-400	128	X227	5867.8	410
94	/M/S	5367.6	-400	129	X226	5812.8	410
95	/M/S	5427.6	-400	130	X225	5757.8	410



Table 2 : Pad Center Coordinates ( Continued )

Unit : um

PAD NO	PAD NAME	COORDINATES		PAD NO	PAD NAME	COORDINATES	
		X	Y			X	Y
131	X224	5702.8	410	166	X189	3777.8	410
132	X223	5647.8	410	167	X188	3722.8	410
133	X222	5592.8	410	168	X187	3667.8	410
134	X221	5537.8	410	169	X186	3612.8	410
135	X220	5482.8	410	170	X185	3557.8	410
136	X219	5427.8	410	171	X184	3502.8	410
137	X218	5372.8	410	172	X183	3447.8	410
138	X217	5317.8	410	173	X182	3392.8	410
139	X216	5262.8	410	174	X181	3337.8	410
140	X215	5207.8	410	175	X180	3282.8	410
141	X214	5152.8	410	176	X179	3227.8	410
142	X213	5097.8	410	177	X178	3172.8	410
143	X212	5042.8	410	178	X177	3117.8	410
144	X211	4987.8	410	179	X176	3062.8	410
145	X210	4932.8	410	180	X175	3007.8	410
146	X209	4877.8	410	181	X174	2952.8	410
147	X208	4822.8	410	182	X173	2897.8	410
148	X207	4767.8	410	183	X172	2842.8	410
149	X206	4712.8	410	184	X171	2787.8	410
150	X205	4657.8	410	185	X170	2732.8	410
151	X204	4602.8	410	186	X169	2677.8	410
152	X203	4547.8	410	187	X168	2622.8	410
153	X202	4492.8	410	188	X167	2567.8	410
154	X201	4437.8	410	189	X166	2512.8	410
155	X200	4382.8	410	190	X165	2457.8	410
156	X199	4327.8	410	191	X164	2402.8	410
157	X198	4272.8	410	192	X163	2347.8	410
158	X197	4217.8	410	193	X162	2292.8	410
159	X196	4162.8	410	194	X161	2237.8	410
160	X195	4107.8	410	195	X160	2182.8	410
161	X194	4052.8	410	196	X159	2127.8	410
162	X193	3997.8	410	197	X158	2072.8	410
163	X192	3942.8	410	198	X157	2017.8	410
164	X191	3887.8	410	199	X156	1962.8	410
165	X190	3832.8	410	200	X155	1907.8	410



Table 2 : Pad Center Coordinates ( Continued )

Unit : um

PAD NO	PAD NAME	COORDINATES		PAD NO	PAD NAME	COORDINATES	
		X	Y			X	Y
201	X154	1852.8	410	236	X119	-72.2	410
202	X153	1797.8	410	237	X118	-127.2	410
203	X152	1742.8	410	238	X117	-182.2	410
204	X151	1687.8	410	239	X116	-237.2	410
205	X150	1632.8	410	240	X115	-292.2	410
206	X149	1577.8	410	241	X114	-347.2	410
207	X148	1522.8	410	242	X113	-402.2	410
208	X147	1467.8	410	243	X112	-457.2	410
209	X146	1412.8	410	244	X111	-512.2	410
210	X145	1357.8	410	245	X110	-567.2	410
211	X144	1302.8	410	246	X109	-622.2	410
212	X143	1247.8	410	247	X108	-677.2	410
213	X142	1192.8	410	248	X107	-732.2	410
214	X141	1137.8	410	249	X106	-787.2	410
215	X140	1082.8	410	250	X105	-842.2	410
216	X139	1027.8	410	251	X104	-897.2	410
217	X138	972.8	410	252	X103	-952.2	410
218	X137	917.8	410	253	X102	-1007.2	410
219	X136	862.8	410	254	X101	-1062.2	410
220	X135	807.8	410	255	X100	-1117.2	410
221	X134	752.8	410	256	X99	-1172.2	410
222	X133	697.8	410	257	X98	-1227.2	410
223	X132	642.8	410	258	X97	-1282.2	410
224	X131	587.8	410	259	X96	-1337.2	410
225	X130	532.8	410	260	X95	-1392.2	410
226	X129	477.8	410	261	X94	-1447.2	410
227	X128	422.8	410	262	X93	-1502.2	410
228	X127	367.8	410	263	X92	-1557.2	410
229	X126	312.8	410	264	X91	-1612.2	410
230	X125	257.8	410	265	X90	-1667.2	410
231	X124	202.8	410	266	X89	-1722.2	410
232	X123	147.8	410	267	X88	-1777.2	410
233	X122	92.8	410	268	X87	-1832.2	410
234	X121	37.8	410	269	X86	-1887.2	410
235	X120	-17.2	410	270	X85	-1942.2	410



Table 2 : Pad Center Coordinates ( Continued )

Unit : um

PAD NO	PAD NAME	COORDINATES		PAD NO	PAD NAME	COORDINATES	
		X	Y			X	Y
271	X84	-1997.2	410	306	X49	-3922.2	410
272	X83	-2052.2	410	307	X48	-3977.2	410
273	X82	-2107.2	410	308	X47	-4032.2	410
274	X81	-2162.2	410	309	X46	-4087.2	410
275	X80	-2217.2	410	310	X45	-4142.2	410
276	X79	-2272.2	410	311	X44	-4197.2	410
277	X78	-2327.2	410	312	X43	-4252.2	410
278	X77	-2382.2	410	313	X42	-4307.2	410
279	X76	-2437.2	410	314	X41	-4362.2	410
280	X75	-2492.2	410	315	X40	-4417.2	410
281	X74	-2547.2	410	316	X39	-4472.2	410
282	X73	-2602.2	410	317	X38	-4527.2	410
283	X72	-2657.2	410	318	X37	-4582.2	410
284	X71	-2712.2	410	319	X36	-4637.2	410
285	X70	-2767.2	410	320	X35	-4692.2	410
286	X69	-2822.2	410	321	X34	-4747.2	410
287	X68	-2877.2	410	322	X33	-4802.2	410
288	X67	-2932.2	410	323	X32	-4857.2	410
289	X66	-2987.2	410	324	X31	-4912.2	410
290	X65	-3042.2	410	325	X30	-4967.2	410
291	X64	-3097.2	410	326	X29	-5022.2	410
292	X63	-3152.2	410	327	X28	-5077.2	410
293	X62	-3207.2	410	328	X27	-5132.2	410
294	X61	-3262.2	410	329	X26	-5187.2	410
295	X60	-3317.2	410	330	X25	-5242.2	410
296	X59	-3372.2	410	331	X24	-5297.2	410
297	X58	-3427.2	410	332	X23	-5352.2	410
298	X57	-3482.2	410	333	X22	-5407.2	410
299	X56	-3537.2	410	334	X21	-5462.2	410
300	X55	-3592.2	410	335	X20	-5517.2	410
301	X54	-3647.2	410	336	X19	-5572.2	410
302	X53	-3702.2	410	337	X18	-5627.2	410
303	X52	-3757.2	410	338	X17	-5682.2	410
304	X51	-3812.2	410	339	X16	-5737.2	410
305	X50	-3867.2	410	340	X15	-5792.2	410

**Table 2 : Pad Center Coordinates ( Continued )****Unit : um**

<b>PAD NO</b>	<b>PAD NAME</b>	<b>COORDINATES</b>		<b>PAD NO</b>	<b>PAD NAME</b>	<b>COORDINATES</b>	
		<b>X</b>	<b>Y</b>			<b>X</b>	<b>Y</b>
341	X14	-5847.2	410	353	X2	-6507.2	410
342	X13	-5902.2	410	354	X1	-6562.2	410
343	X12	-5957.2	410	355	DUMMY	-6617.2	410
344	X11	-6012.2	410	356	DUMMY	-6672.2	410
345	X10	-6067.2	410	357	DUMMY	-6774.3	321.7
346	X9	-6122.2	410	358	VLCDL	-6774.3	261.7
347	X8	-6177.2	410	359	VHL	-6774.3	201.7
348	X7	-6232.2	410	360	VML	-6774.3	-0.6
349	X6	-6287.2	410	361	VML	-6774.3	-60.6
350	X5	-6342.2	410	362	VLL	-6774.3	-190.4
351	X4	-6397.2	410	363	VEEL	-6774.3	-250.4
352	X3	-6452.2	410	364	DUMMY	-6774.25	-407.8