5 GHz Complementary Source-Coupled LC Tank Oscillator

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***Abstract*—This report describes the design steps that led to the implementation of an LC tank oscillator operating at 5 GHz, with a 1 V peak-to-peak output voltage.**

I. Introduction

This work addresses the design of a source-coupled LC tank oscillator implemented in IHP SiGe 0.25 µm technology, operating at 5 GHz with a 1 V peak-to-peak output voltage. The circuit is intended as a reference signal generator for applications in the 5G New Radio band n79.

Circuit simulations were carried out using Keysight ADS. All active and passive components were dimensioned by first neglecting non-idealities and subsequently accounting for them. A comprehensive comparison between the ideal and real cases was performed in terms of operating point, output voltage, oscillation frequency, and phase noise, the latter representing the final performance metric.

II. Theoretical Model

A. RLC Group

The circuit is shown in Fig. 1. The first step is to size the LC tank so that it resonates at the required frequency of 5 GHz. Since there are two degrees of freedom, it is possible to start with an inductance value of 0.94 nH, as its real model is already available in the process library.

After selecting the inductance, the capacitor value is chosen using:

$$C = \frac{1}{\omega_0^2 L}.$$

This yields:

$$C = 1.08\,\mathrm{pF}.$$

The capacitance value C will need to be recalibrated later.

Following this, the resistive load across which the generated oscillation is taken was selected. Since this depends on the total quality factor of the parallel circuit, a value of 400 Ω was chosen as a first approximation. Using:

$$R_L = \frac{Q_{\text{tot}}}{\omega_0\, C}, \tag{1}$$

this leads to a total quality factor $Q_{\text{tot}} = 13.57$.

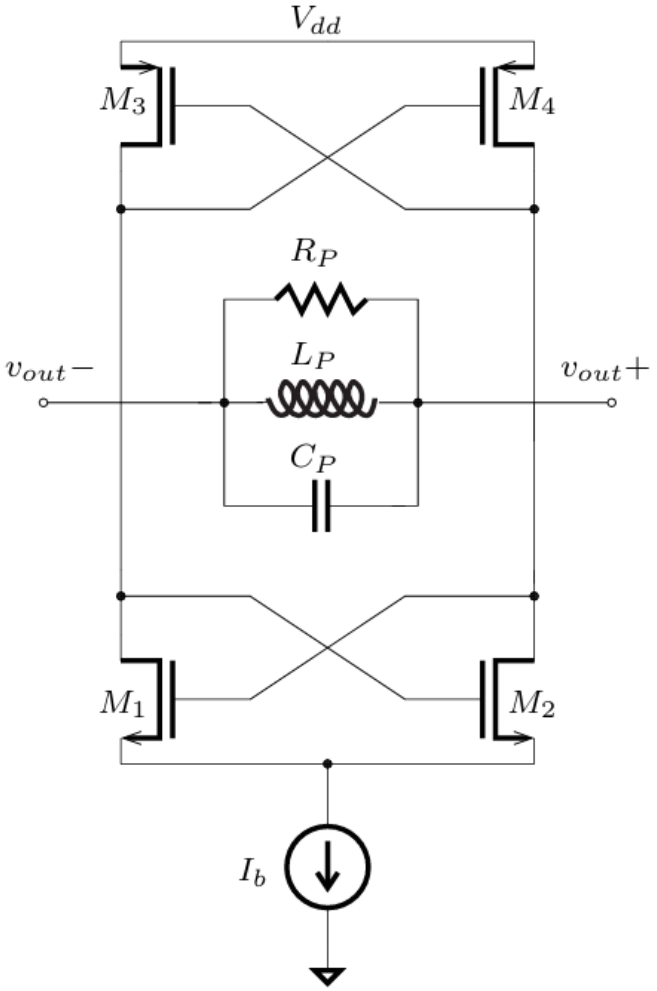


Figure 1: Circuit schematic.

B. Biasing Circuit Sizing

Moving on to the biasing circuit, as shown in Figure 2, the tail current I_t, the bias current I_{bias}, the bias resistance R_{bias}, and the dimensions of the transistors forming the current mirror must be sized.

To provide a more detailed derivation of the biasing conditions, we assume that the oscillation amplitude is large enough to drive the MOSFETs (see Figure 1) in switching mode. In

this regime, the transistors behave as ideal switches, and the drain currents can be modeled as two square waves with a mean value of $I_t/2$ and a peak-to-peak amplitude of I_t.

The differential current $I(t)$ injected into the RLC tank is therefore a square wave with zero mean and amplitude I_t. Expanding the expression for $I(t)$ into a Fourier series, we obtain:

$$I(t) = 2I_t \sum_{n=1}^{\infty} \left(\frac{\sin(n\pi/2)}{n\pi/2} \right) \cos(n\omega_0 t) \tag{2}$$

Due to the high-quality factor and the selective filtering property of the LC tank, it is assumed that only the fundamental harmonic ($n = 1$) contributes to the voltage drop across the load resistance R_L, while higher-order harmonics are effectively filtered out. Taking only the first harmonic into account, the current I_1 is given by:

$$I_1 = \frac{4I_t}{\pi} \cos(\omega_0 t) \tag{3}$$

The resulting peak-to-peak output voltage V_{pp} is twice the peak amplitude across R_L, leading to:

$$V_{pp} = \frac{8R_L I_t}{\pi} \tag{4}$$

By rearranging this formula, the required tail current I_t can be calculated to satisfy the design specifications:

$$I_t = \frac{\pi V_{pp}}{8R_L} \approx 1 \text{ mA} \tag{5}$$

where V_{pp} is set to 1 V for this specific design.

Since the bias current I_{bias} flowing through the master branch of the current mirror causes power dissipation across the resistance R_{bias}, [6], the mirror was designed with a magnification ratio of 10. This means that the width W of the MOSFET carrying the tail current I_t is 10 times larger than that of the master MOSFET.

The mirror ratio is defined as:

$$K_{\text{mirror}} = \frac{W_s/L_s}{W_m/L_m} = 10, \tag{6}$$

where W_s, L_s are the channel width and length of the slave MOSFET, and W_m, L_m are the channel width and length of the master MOSFET.

From these design choices:

$$I_{\text{bias}} = \frac{I_t}{K_{\text{mirror}}} = \frac{1\,\text{mA}}{10} = 100\,\mu\text{A}. \tag{7}$$

The channel lengths of the two MOSFETs in the mirror were chosen to be equal and set to 480 nm. These are not the minimum values allowed by the technology. This choice was made to prevent the mirror's output resistance from being too low, which would cause the tail current to depend heavily on the slave drain voltage. At the same time, the channel length was not made excessively large to avoid a significant roll-off effect, which would increase the threshold voltage of the MOSFETs.

Having set $W_m = 2\,\mu\text{m}$, W_s is consequently $W_s = 20\,\mu\text{m}$.

By utilizing, as demonstrated in [3], the saturation current formula for a MOSFET—modeled as a long-channel device for the reasons previously discussed:

$$I_{DS} = \frac{\mu_n C_{ox} W}{2L} (V_{gs} - V_t)^2 \tag{8}$$

So the gate-source voltage of the master transistor is found to be:

$$V_{gs} \approx 1.13 \text{ V} \tag{9}$$

This leads to:

$$R_{\text{bias}} = \frac{V_{dd} - V_{gs}}{I_{\text{bias}}} = 13.7\,\text{k}\Omega. \tag{10}$$

The supply voltage was set to $V_{dd} = 2.5\,\text{V}$.

C. Supply Voltage and Biasing Requirements

The supply voltage V_{DD} was set to 2.5 V to ensure that all transistors operate within their intended biasing regions. Specifically, the value of V_{DD} must be sufficiently high to provide the necessary headroom for the saturation drain-source voltage of the current mirror's slave transistor ($V_{DS,sat}$), as well as the gate-source voltages of the NMOS and PMOS devices operating in switching mode.

The gate-source voltage for the switching transistors can be approximated using the transconductance efficiency relationship:

$$V_{GS} = V_t + \frac{I_t/2}{g_m} \tag{11}$$

Furthermore, the saturation voltage of the tail current source is determined by its overdrive voltage:

$$V_{DS,sat} = V_{GS} - V_t \tag{12}$$

Considering a threshold voltage $V_t \approx 0.6\,\text{V}$, the required voltages are:

$$V_{GS,n} \approx 0.764\,\text{V} \tag{13}$$

$$|V_{GS,p}| \approx 0.786\,\text{V} \tag{14}$$

For the current mirror slave transistor, given a gate voltage $V_{GS} = 1.13\,\text{V}$, the saturation voltage is:

$$V_{DS,sat} = 1.13 - 0.6 = 0.53\,\text{V} \tag{15}$$

The minimum required supply voltage is therefore defined as:

$$V_{DD,min} = V_{DS,sat} + V_{GS,n} + |V_{GS,p}| \tag{16}$$

Substituting the calculated values:

$$V_{DD,min} = 0.53 + 0.764 + 0.786 \approx 2.08\,\text{V} \tag{17}$$

Since $V_{DD} = 2.5\,\text{V} > 2.08\,\text{V}$, the choice of supply voltage ensures that the core of the oscillator remains correctly biased even during large-signal swings, preventing the tail current source from entering the triode region.

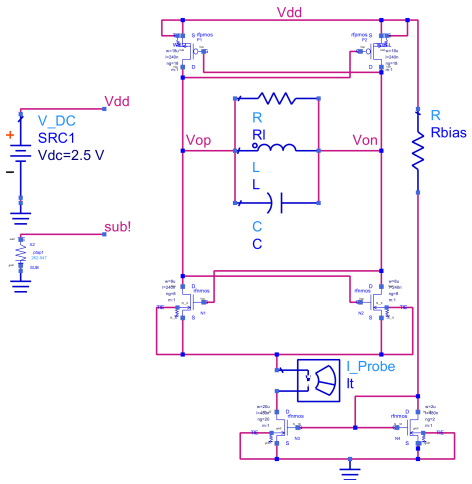


Figure 2: ADS schematic of the LC tank oscillator

Moving to the Advanced Design System (ADS) environment, the implemented circuit is shown in Figure 2. By subsequently performing a DC simulation on the biasing circuit, as shown in Fig. 3, the value of R_{bias} can be adjusted to achieve a more accurate value for the tail current I_t. Therefore, $R_{\text{bias}} = 12.67\,\text{k}\Omega$ was selected.

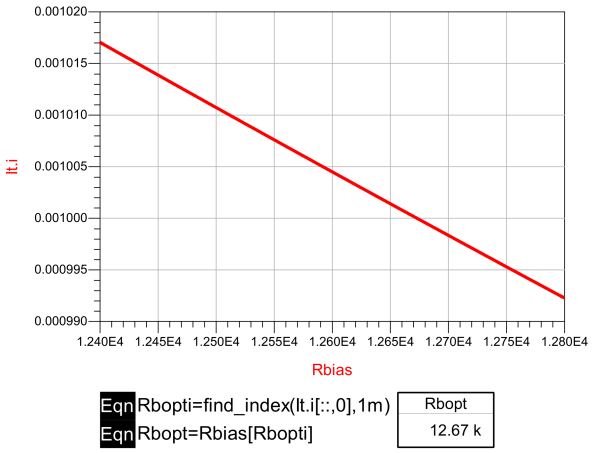


Figure 3: Parametric sweep of the R_{bias} resistance

D. Transconductance and Oscillation Startup

The purpose of the cross-coupled transistors is to generate and sustain the oscillation by compensating for the parasitic resistance R_L of the RLC tank. From small-signal analysis, it can be shown that a cross-coupled pair can be modeled as a negative resistance with value $-2/g_m$, where g_m is the transconductance of the MOSFETs.

Impedance Analysis: By considering the two NMOS transistors as an example, the impedance seen from their drains can be calculated by applying a test voltage generator V_G, as illustrated in Figure 4, and determining the ratio V_G/I_G.

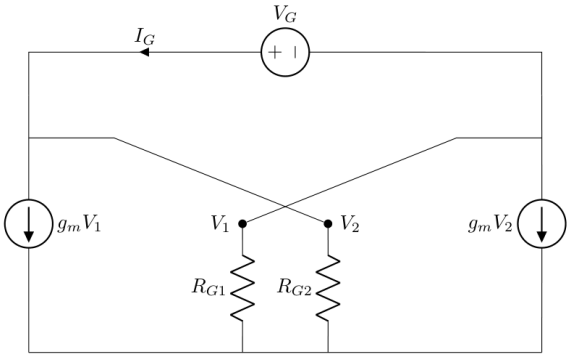


Figure 4: Impedance derivation

Neglecting the effects of capacitances and the output resistance R_o, we obtain:

$$V_2 = \frac{V_G}{2}, \quad V_1 = -\frac{V_G}{2} \tag{18}$$

Consequently:

$$I_G = \frac{V_G}{2}\left(\frac{1}{R_G} - g_m\right) \approx -\frac{V_G}{2} g_m \tag{19}$$

This derivation assumes that the transistors are ideally matched, meaning the gate resistances R_G are identical and the voltage V_G is distributed equally between them.

In conclusion, the resulting gate impedance is:

$$Z_G = \frac{V_G}{I_G} = -\frac{2}{g_m} \quad (\text{with } \text{Re}\{Z_G\} < 0) \tag{20}$$

The small-signal equivalent circuit is shown in Figure 5.

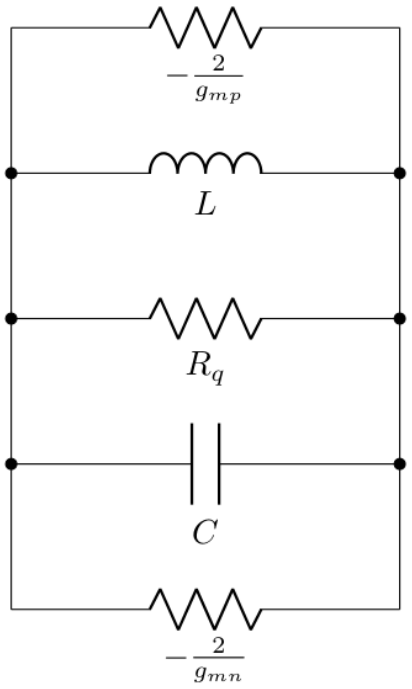


Figure 5: Small signal circuit

To ensure startup, according to Barkhausen's startup criterion, as also demonstrated in [1], the total conductance of the parallel circuit must be negative. This leads to:

$$\frac{g_{mn}}{2} + \frac{g_{mp}}{2} > \frac{1}{R_L} \tag{21}$$

where g_{mn} and g_{mp} denote the transconductance of the NMOS and PMOS transistors, respectively.

In determining the required g_m values, the channel length for these MOSFETs can be set to the minimum value allowed by the technology, 240 nm, as the issues previously mentioned regarding the current mirror transistors do not apply here.

By employing the drain current formula for a short-channel MOSFET, the expression for the transconductance is given by:

$$g_m = \frac{\mu_n C_{ox}}{2} W E_{sat} \tag{22}$$

where E_{sat} represents the saturation electric field. By rearranging this equation, the minimum transistor widths required for oscillation are found to be:

$$W_n = \frac{2}{R_L E_{sat} \mu_n C_{ox}} > 7.2 \text{ µm} \tag{23}$$

Consequently, assuming a W_p/W_n ratio of approximately 2.5 to compensate for the lower hole mobility, the width for the PMOS devices is:

$$W_p > 17.3 \text{ µm} \tag{24}$$

Based on these results, the values $W_n = 8\,\mu\text{m}$ and $W_p = 18\,\mu\text{m}$ were initially selected.

At this point, by performing a DC simulation with operating point analysis, the real values of g_m were extracted, as shown in Fig. 6, where the transconductances in question refer to transistors M_1, M_2 and M_5, M_6, respectively.

index	gm
1	1.988 m
2	1.988 m
3	2.835 m
4	333.6 u
5	1.586 m
6	1.586 m

Figure 6: g_m analysis with minimum transistor widths

Comparing these real g_m values, it is observed that:

$$\frac{g_{mn} + g_{mp}}{2} < \frac{1}{R_L}. \tag{25}$$

Consequently, the negative conductance provided by the active network is insufficient to compensate for the tank losses, and the circuit fails to oscillate with the current values of W_n and W_p. Therefore, we performed a resizing of W_n and W_p. The new values were set to $W_n = 16\,\mu\text{m}$ and $W_p = 48\,\mu\text{m}$ to ensure the oscillation condition is met.

index	gm
1	3.056 m
2	3.056 m
3	3.233 m
4	333.6 u
5	2.691 m
6	2.691 m

Figure 7: g_m analysis with $W_n = 16\,\mu\text{m}$ and $W_p = 48\,\mu\text{m}$

In this case the condition

$$\frac{g_{mn} + g_{mp}}{2} > \frac{1}{R_L}. \tag{26}$$

is verified; therefore, the circuit provides sufficient gain to compensate for the losses, ensuring the buildup of the oscillation. As illustrated in Figure 7, even a width ratio of 3 is insufficient to equalize the transconductances; in this specific case, the hole mobility is approximately 4 times lower than the electron mobility.

E. Verification of the Equivalent Impedance

The transconductance (g_m) values can be verified through an AC simulation. As shown in Figure 8, the RLC tank was removed in ADS and replaced with an AC current source and a `DC_feed` block. This component acts as a short circuit at DC and an open circuit for all other frequencies.

The ratio between the voltage drop across the generator and the injected current corresponds to the impedance seen by the RLC tank. As illustrated in Figure 9, the real part of the simulated total admittance is close to the theoretically calculated value, confirming the validity of the active core design.

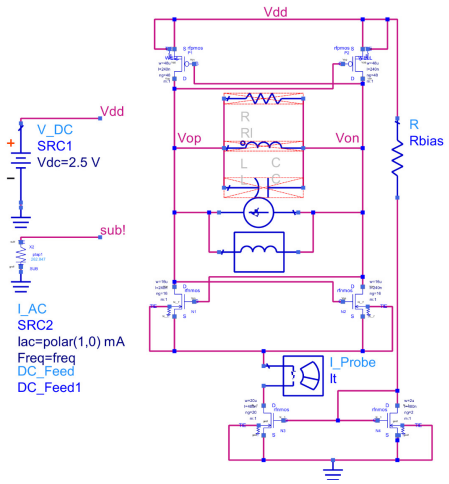


Figure 8: ADS schematic for seen impedance calculation

Eqn Vo=Vop-Von Eqn Ip=1m
Eqn Z_IN=Vo/Ip Eqn Y_IN=1/Z_IN

freq	Z_IN	Y_IN
5.000 GHz	-123.7 - j175.6	-2.681 m + j3.806 m

Figure 9: Equivalent Conductance

III. Transient Analysis

Once the circuit is sized, a transient simulation can be performed in ADS to visualize the output voltage. Since this is an autonomous circuit without an external input, an initial condition must be set to trigger the oscillation; in a real-world application, startup is initiated by thermal noise.

By setting an initial condition on the capacitor, the output waveform obtained is shown in Fig. 10.

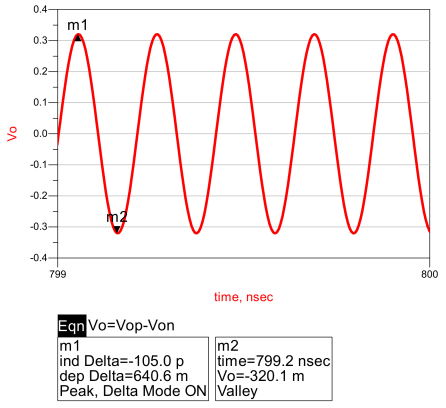


Figure 10: Output voltage waveform

As can be observed, the specification for the peak-to-peak voltage V_{pp} is not met. Indeed, the peak-to-peak voltage measures 0.640 V.

This behavior is due to the fact that the transistors enter the triode region during switching, which results in a lower effective transconductance g_m.

Indeed, the transconductance g_m is inversely proportional to the load resistance R_L:

$$g_m \propto \frac{1}{R_L} \tag{27}$$

By substituting the relationship previously derived for the output swing, the link between the transconductance and the peak-to-peak voltage V_{pp} is established as:

$$g_m \propto \frac{8I_t}{\pi V_{pp}} \tag{28}$$

Figure 11 illustrates the trend. As observed, also by considering the behavior of the two different DC transconductance values (g_{m1} and g_{m2}), g_m does not remain constant but decreases, resulting in a peak-to-peak voltage $V_{\text{pp}} < 1\,\text{V}$. It is therefore necessary to further increase the transistor widths to achieve the required peak-to-peak voltage.

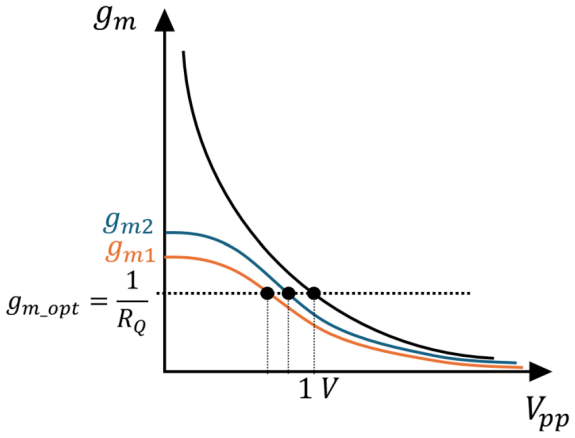


Figure 11: Analysis of g_m versus V_{pp} plot

Following several simulation iterations, the final values were set to $W_n = 26\,\mu\text{m}$ and $W_p = 78\,\mu\text{m}$. All MOSFETs were designed with a number of gate fingers such that the width of each individual finger is 1 µm.

The output voltage now exhibits a peak-to-peak amplitude $V_{\text{pp}} = 1.006\,\text{V}$, as shown in Fig. 12, which is in line with the design specifications.

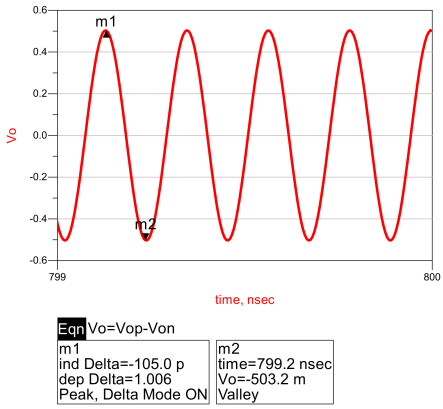


Figure 12: Output voltage waveform after width optimization

Continuing with the circuit analysis, it can be observed in Fig. 13 that the oscillation frequency specification is not met. From the spectral analysis, the fundamental frequency is found to be approximately 4.6 GHz.

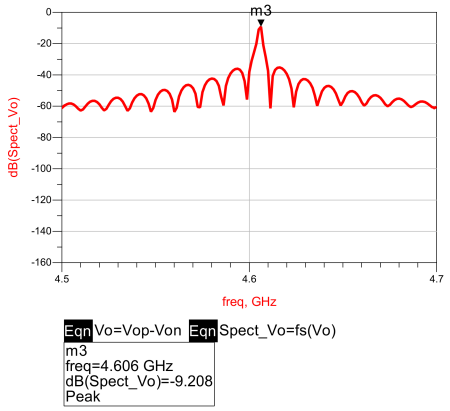


Figure 13: Spectrum of V_{out}

The initial capacitance calculation did not account for the fact that real MOSFETs exhibit parasitic capacitances. These parasitics contribute to the total tank capacitance, thereby shifting the oscillation frequency to a lower value.

Consequently, in addition to the transistor widths, it is necessary to resize the LC tank capacitance as well.

A. Capacitance sweep

By incorporating a parameter sweep of the capacitance into the Transient simulation, from an initial broader sweep of the capacitance, as shown in Figure 14, it can be observed that the optimal value lies between 880 fF and 980 fF.

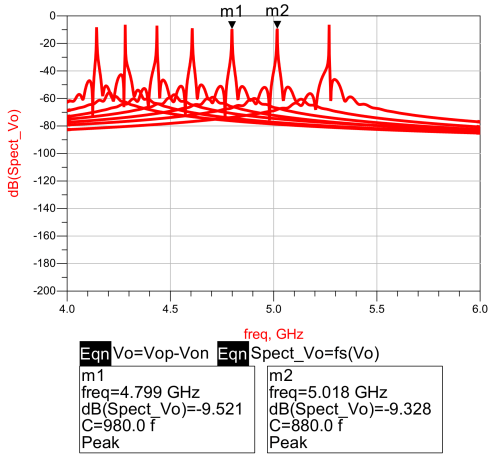


Figure 14: Initial coarse capacitance sweep

By further narrowing the capacitance sweep range, it can be observed that the correct capacitance value is 870 fF, as shown in Figure 15.

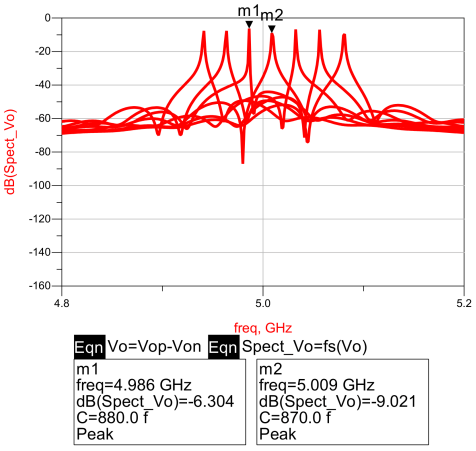


Figure 15: Finer capacitance sweep

IV. Harmonic Balance

Harmonic Balance simulation allows for circuit analysis in the frequency domain without requiring the transform of a transient simulation. Consequently, it significantly reduces the simulator's processing time. To perform a Harmonic Balance simulation, it is necessary to insert an *OscPort* within the feedback loop of the two cross-coupled transistors; this bypasses the initial oscillation startup, moving directly to steady-state conditions.

Since the Harmonic Balance simulation is computationally lighter, the capacitance value can be confirmed by performing a much finer sweep, as shown in Figure 16.

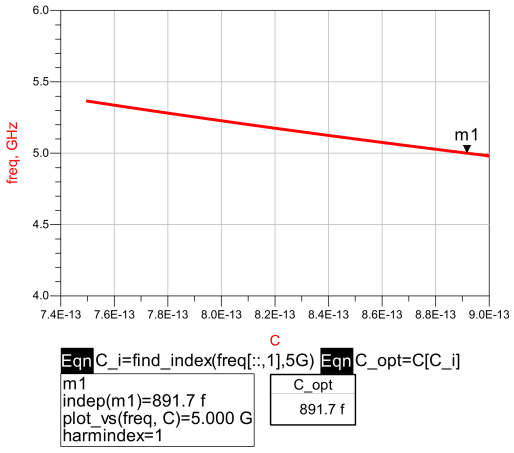


Figure 16: Parametric capacitance sweep using HB simulation

The definitive value is thus $C = 891.7$ fF.

Proceeding with the HB simulation, the output voltage waveform and its spectrum are reported again in Figure 17 and Figure 18 respectively. These results confirm the required specifications for the peak-to-peak voltage (V_{pp}) and the oscillation frequency.

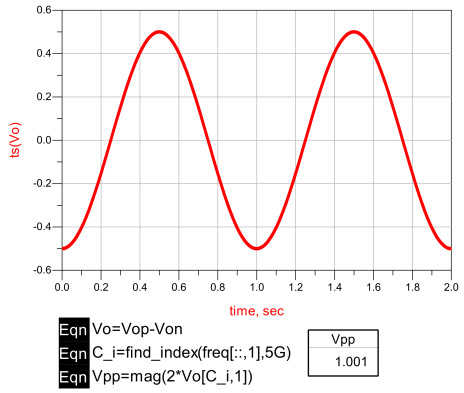


Figure 17: Output voltage waveform

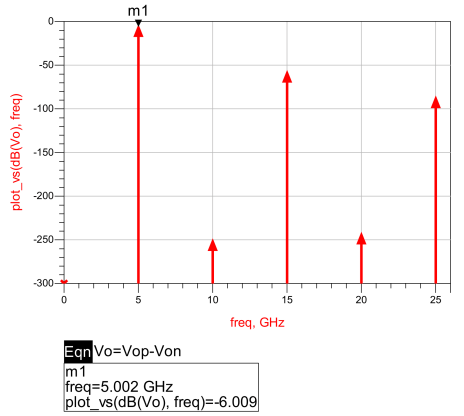


Figure 18: Output voltage spectrum

V. Phase Noise

Phase noise is a fundamental metric used to characterize the frequency stability of an oscillator. It is formally defined as the ratio of the Power Spectral Density (PSD) at a specific offset frequency $\Delta\omega$ from the carrier to the total power of the carrier signal:

$$\mathcal{L}(\Delta\omega) = \frac{S_\phi(\omega_0 + \Delta\omega)}{\frac{V_m^2}{2}} \tag{29}$$

where $S_\phi(\omega_0 + \Delta\omega)$ represents the noise power in a 1 Hz bandwidth at the offset frequency, and $\frac{V_m^2}{2}$ is the power of the carrier signal at frequency ω_0.

According to *Hajimiri's theory*, as demonstrated in [2] and in [4], the phase noise spectrum exhibits different regions based on the frequency offset from the carrier. In the region closest to the carrier, the noise follows a $1/\Delta\omega^3$ trend, which is primarily due to the upconversion of flicker noise ($1/f$ noise) from the active devices. As the offset increases, the spectrum transitions to a $1/\Delta\omega^2$ slope, dominated by thermal noise. Finally, at very large offsets, the phase noise reaches a constant floor, denoted as A_0, representing the broadband white noise of the system.

The phase noise power spectral density, accounting for both thermal and flicker noise contributions under the *Hajimiri LTV* framework, is expressed as:

$$\mathcal{L}(\Delta\omega) = \frac{S_0}{Q_m^2 \Delta\omega^2}\left[\Gamma_{rms}^2 + \frac{C_0^2}{4}\left(\frac{\omega_c}{\Delta\omega}\right)\right] \tag{30}$$

This analytical expression allows for a precise decomposition of the noise sources and their respective upconversion mechanisms:

- S_0: The power spectral density of the white noise current source (thermal noise). It represents the raw "noise power" injected into the oscillator tank before being shaped by the circuit's time-variant response.
- Q_m: The maximum charge displacement ($C_{tot}V_m$). It acts as a normalization factor; a higher charge swing effectively makes the phase of the oscillation more immune to external noise perturbations.
- $\Delta\omega$: The frequency offset from the carrier frequency ω_0. The formula shows how the noise power decays as we move further from the carrier.
- Γ_{rms}: The root-mean-square value of the Impulse Sensitivity Function (ISF). This term governs the $1/f^2$ region of the phase noise, representing the average sensitivity of the oscillator to thermal noise over a complete cycle.
- C_0: The DC coefficient (zero-order Fourier coefficient) of the ISF. This is a critical design parameter; it determines the amount of $1/f$ noise that is upconverted into the $1/f^3$ region. A perfectly symmetric waveform results in $C_0 \to 0$, theoretically eliminating flicker noise upconversion.
- ω_c: The flicker noise corner frequency of the active devices.

ADS Simulation Setup: To evaluate the phase noise performance of the designed oscillator, a simulation was performed in Advanced Design System (ADS) using the Harmonic Balance (HB) engine. To execute this analysis, it is necessary to add the *HB Noise Controller* to the schematic. Within this controller, the simulation interval must be specified around the carrier frequency ω_0, defining the range over which the phase noise will be calculated and plotted.

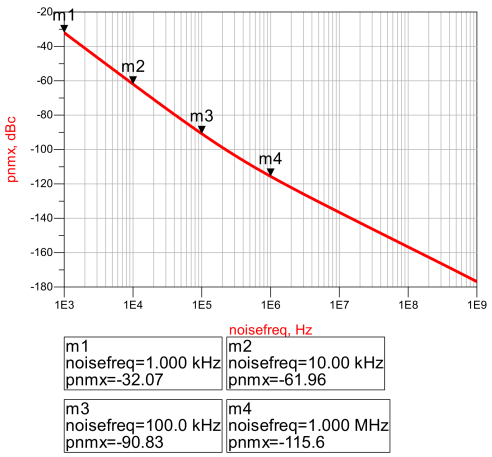


Figure 19: Phase noise plot in logarithmic scale

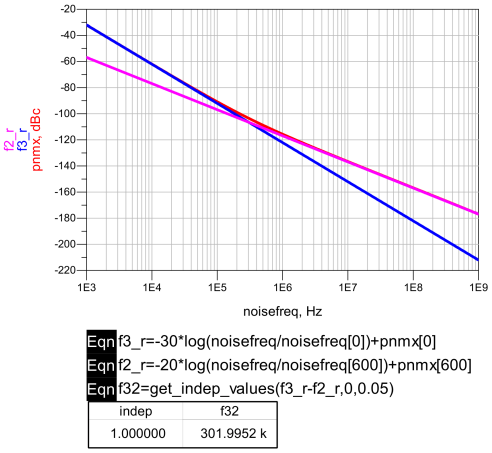


Figure 20: Phase noise profile highlighting $1/f^3$ and $1/f^2$ slope characteristics

As observed from the simulations, the results are in good agreement with *Hajimiri's theory*.

As illustrated in Fig. 20, the corner frequency marking the transition from a $1/f^3$ slope to a $1/f^2$ slope was also determined. This was achieved by plotting the two asymptotic lines with slopes of -30 dB/dec and -20 dB/dec on a logarithmic scale and identifying their intersection point.

The resulting cut-off frequency is calculated as follows:

$$f_t = 301.99 \text{ kHz} \tag{31}$$

The double-stage cross-coupled LC tank oscillator exhibits lower phase noise susceptibility compared to the single-stage topology. This improvement is primarily due to the constant presence of an active MOSFET at the output nodes (V_{out+} and V_{out-}), which ensures significantly higher symmetry between the positive and negative half-cycles.

This enhanced symmetry leads to a more balanced *Impulse Sensitivity Function* (ISF), denoted as $\Gamma(\omega_0\tau)$. By making the ISF more symmetric, its DC component (the c_0 Fourier coefficient) is substantially reduced. Since this DC component is the primary cause of flicker noise upconversion into the $1/\Delta\omega^3$ region, its reduction effectively minimizes the phase noise close to the carrier. This is a critical result, as the $1/\Delta\omega^3$ component is the most problematic to mitigate due to its proximity to the carrier frequency.

Furthermore, due to the inverse quadratic dependence of phase noise on the output voltage swing in the denominator, the double-stage version, under the same bias conditions, achieves an even further reduction in phase noise compared to the single-stage topology.

VI. Performance Validation using Realistic Component Models

In this section, the oscillator behavior is re-evaluated by incorporating the non-idealities of a physical LC tank. We focus on the discrepancies between the ideal model and the practical implementation, assessing how parasitic elements affect the resonance and overall phase noise.

A. Circuit Modifications

As illustrated in Figure 21, several modifications were implemented to transition from the ideal model to a process-specific implementation:

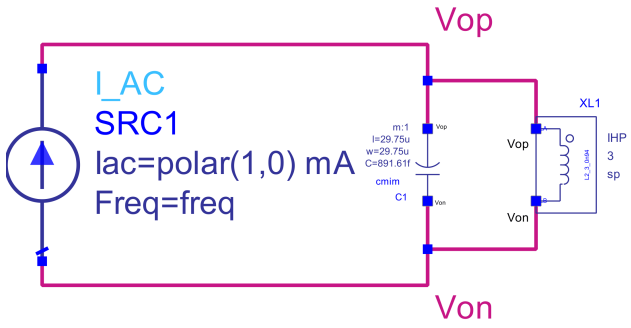


Figure 21: Real LC tank schematic

- *MIM Capacitor:* The ideal capacitance has been replaced by the "cmim" component, a Metal-Insulator-Metal capacitor provided by the technology library.
- *Physical Inductor:* The ideal inductor was substituted with its real counterpart. As noted in the initial design phase, a 0.94 nH inductor is already available within the provided process design kit (PDK).
- *Removal of R_L:* The explicit load resistor R_L has been removed from the schematic. In this realistic configuration, the equivalent parallel resistance is now intrinsically determined by the real LC tank components.

Regarding the capacitive element, a parameter-driven design strategy was adopted for this component: by defining the target capacitance value, the ADS environment automatically synthesizes the physical dimensions (W and L) of the square

capacitor geometry. In the technology process used for this design, the MIM capacitors exhibit a unit area capacitance of $1\,\text{fF}/\mu\text{m}^2$. Consequently, to achieve the required capacitance, the device dimensions were synthesized resulting in a square geometry with $W = L = 29.75\,\mu\text{m}$.

B. Equivalent Resistance Characterization

First, an AC simulation was performed, as shown in Figure 21, to characterize the equivalent parallel resistance (R_L) of the real LC tank [5]. This step is essential to quantify the impact of physical losses and to refine the circuit parameters accordingly.

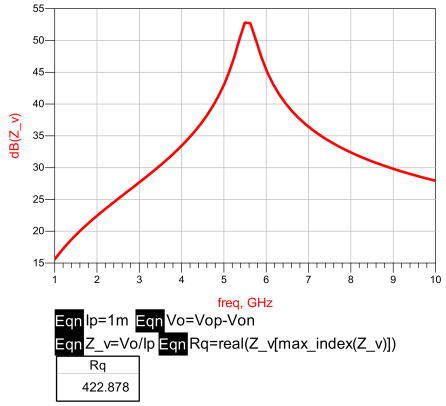


Figure 22: Equivalent R_L extraction via AC simulation

As shown in Figure 22, the resonance frequency of the tank was identified to evaluate the impedance magnitude at that point. From the simulation results, the equivalent resistance R_L was found to be approximately $422\,\Omega$. This value is in close agreement with the initial estimates made during the early design phase.

C. Circuit Resizing

Since the simulated R_L value at the resonance peak is consistent with the initial estimates, the dimensions of the cross-coupled transistor pairs were kept at $W_n = 26\,\mu\text{m}$ and $W_p = 78\,\mu\text{m}$. Although the slight increase in R_L could have allowed for a marginal reduction in channel widths, such a modification would have necessitated an increase in the tail current (I_t) to maintain the same performance metrics, thereby leading to higher power dissipation. Consequently, the original sizing was preserved to ensure a robust startup margin while optimizing the overall power efficiency.

D. Circuit Fine-Tuning and Harmonic Balance Validation

The subsequent design phase involves the calibration of the tail current (I_t) and the tank capacitance to strictly meet the specifications for peak-to-peak voltage (V_{pp}) and oscillation frequency (f_0).

Initial *Harmonic Balance* (HB) simulations using the previous values revealed that the oscillation frequency exceeded $5\,\text{GHz}$, while the V_{pp} remained below the $1\,\text{V}$ target, as illustrated in Figure 23.

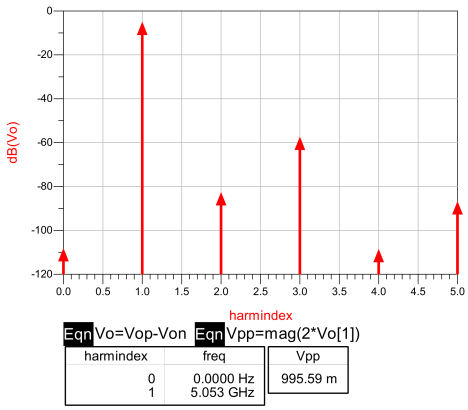


Figure 23: Simulation with initial C value

To address the frequency offset, a parametric sweep was performed on the tank capacitance. The optimal value was identified as:

$$C = 913\,\text{fF} \tag{32}$$

As shown in Figure 24, this adjustment successfully centered the oscillation frequency.

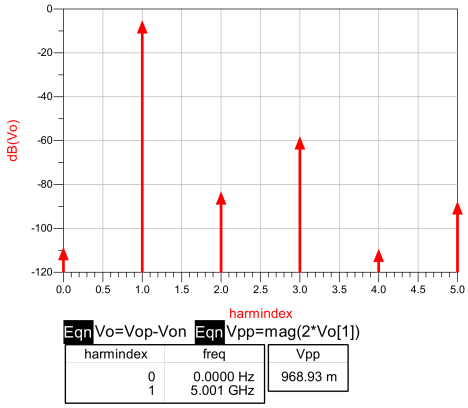


Figure 24: Simulation with corrected C value

Subsequently, to achieve the required $1\,\text{V}$ peak-to-peak swing, another sweep was performed on the bias resistor (R_{bias}), ranging from $11\,\text{k}\Omega$ to $12.5\,\text{k}\Omega$ with a $1\,\Omega$ step.

As depicted in Figure 25, the final value for the bias resistor was determined to be:

$$R_{bias} = 12.315\,\text{k}\Omega \tag{33}$$

which results in a tail current of:

$$I_{tail} \approx 1.04\,\text{mA} \tag{34}$$

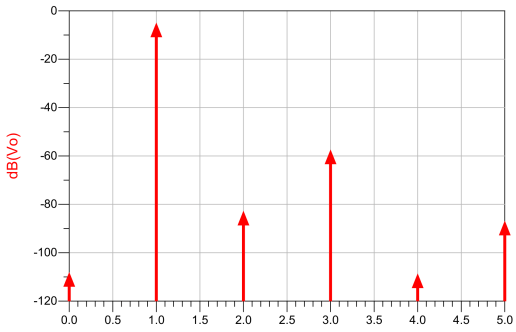
Eqn Vo=Vop-Von Eqn Vpp=mag(2*Vo[1])
Eqn Rbias_opt=get_indep_values(Vpp,1,0.00005,1)
Eqn It_opt=real(It.i[find_index(Rbias,Rbias_opt),0])

indep	Rbias_opt	It_opt
1.0000	12.315 k	1.0457 m

Figure 25: Final Rbias sweep

E. Specification Validation

Finally, as reported in Figure 26, a comprehensive Harmonic Balance (HB) simulation was performed to validate the overall performance of the oscillator. This verification step ensures that all design targets are met under the final circuit configuration.



Eqn Vo=Vop-Von Eqn Vpp=mag(2*Vo[1])

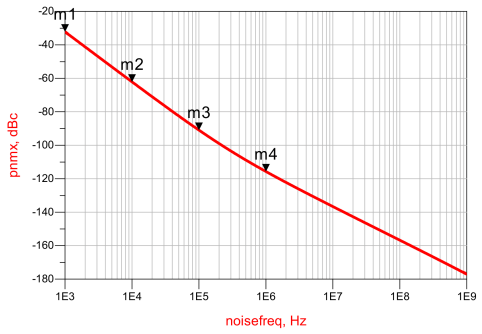
harmindex	freq	Vpp
0	0.0000 Hz	999.97 m
1	5.002 GHz	

Figure 26: Final HB simulation

F. Phase Noise

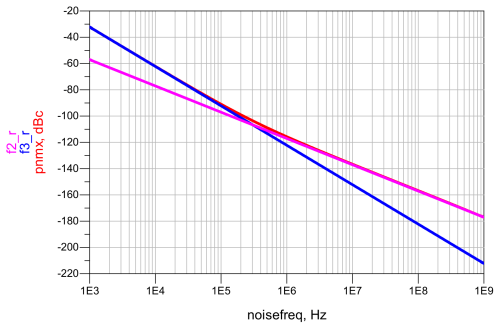
The phase noise characteristics were finally evaluated using the circuit configuration with physical component models. As illustrated in Figures 27 and 28, the noise profile remains highly consistent with the previously analyzed ideal case.

Both the absolute noise power spectral density and the corner frequency, representing the transition between the $1/f^3$ region and the $1/f^2$ region, exhibit negligible variations. This indicates that the design maintains its spectral integrity even when accounting for parasitic effects of the real LC tank.



m1 noisefreq=1.000 kHz pnmx=-32.23	m2 noisefreq=10.00 kHz pnmx=-62.11
m3 noisefreq=100.0 kHz pnmx=-90.96	m4 noisefreq=1.000 MHz pnmx=-115.7

Figure 27: Phase noise plot in logarithmic scale



Eqn f3_r=-30*log(noisefreq/noisefreq[0])+pnmx[0]
Eqn f2_r=-20*log(noisefreq/noisefreq[600])+pnmx[600]
Eqn f32=get_indep_values(f3_r-f2_r,0,0.05)

indep	f32
1.000000	301.9952 k

Figure 28: Phase noise profile highlighting $1/f^3$ and $1/f^2$ slope characteristics

VII. Conclusion

This work presented the design, optimization, and characterization of an LC-tank oscillator based on a complementary cross-coupled topology. The final implementation successfully met the design requirements, accurately centering the oscillation frequency at 5 GHz and providing a regulated 1 V peak-to-peak output swing.

The transition from ideal models to PDK-based physical components introduced a predictable, albeit slight, shift in performance metrics, primarily due to parasitic resistive losses in the tank. However, the phase noise performance proved to be remarkably resilient, maintaining a consistent profile between the ideal and realistic simulation stages. Due to the various advantages previously discussed, this type of oscillator enables the achievement of low phase noise and high-quality signal oscillation. Consequently, it proves to be highly effective for 5G band applications and high-performance RF systems.

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