ECE 4250/7250
VHDL AND PROGRAMMABLE LOGIC DEVICES

LAB #6
CLOCK GENERATION

I. Objective
The objective is to use Process (CLK) to generate a clock of periods 0.5s, 1s, 2s, 4s from the 50MHz clock on Spartan 3 board.

II. Problems
The clock frequency of the Spartan 3 board is 50MHz. You have to take this clock as the input and generate clocks with periods of 0.5s, 1s, 2s, 4s using Generic statement.

III. Instructions
- The generated clock should be displayed on LEDs. The LEDs should flash according to the period of the clock.
- You may need three files to complete your lab successfully
    - GenClock.vhd : to generate the clocks with different clock periods
    - TestClock.vhd : to test the generated clock
    - TestClock.ucf: to display the clocks generated on the LEDs on Spartan-3 FPGA.
- In the Generic statement; The time_period specifies the period of the clock to be generated.
- **OR**, you can come up with your own design and files to generate the clocks as stated at the objective.

The structure of this code may be as follows:

1. GenClock.vhd

```
Entity GenClock is
Generic(time_period : integer range 1 to 4 );
Port (clk: in std_logic;
        Clock: out std_logic);
End GenClock;

Architecture Behavior of GenClock is
    <...>
begin
    <...>
    process (clk)
    begin
        <...>
    end process;
end Behavior;
```

2. TestClock.vhd

Entity TestClock is
Port (<......>);
end TestClock;

Architecture Execute of TestClock is
Component GenClock
Generic(time_period : integer range 1 to 4);
Port (clk: in std_logic;
      Clock: out std_logic);
end Component;

begin
  <.......>
end execute;

3. TestClock.ucf
In order to get the "clk" input and display the generated clocks on the LED you must write your own
".UCF" file. Use the one from Lab4 as guide! (50MHz clock is on port "T9")

IV. Deliverables
1. Demonstration is required.
2. Pre- Lab:
   - Read about Generics in the textbook section 8.9
3. Report:
   1. Objective
   2. Lab work:
        i. Implementation: Describe your design and include the completed and compiled (.vhd) files
           and the (.ucf) file with comments for your code.
        ii. Answer this question.
           What is the function of the statement GENERIC, and how can one instantiate a Generic
           component. i.e How to port map it?
   3. Conclusion: What went wrong? Why? And how did you solve it? What did you learn from this
      lab?

V. Grading
This lab is worth 15 points:
1. Successful demonstration: 8 Points
2. Report: 7 Points.