ECE 4250/7250
VHDL AND PROGRAMMABLE LOGIC DEVICES

LAB#2
DESIGN SIMULATION USING MODELSIM II

I. Objective

This objective of this lab is to use ModelSim to create and simulate a 6-bit full subtractor.

II. Problems

In this lab you have to design and create a 6-bit full subtractor by using 6 full subtractors as the component. Your design should have two 6-bit inputs (A, B), a borrow-in input (B_{in}), a 6-bit subtract output (C) and a borrow-out output (B_{out}) as shown in figure 1.

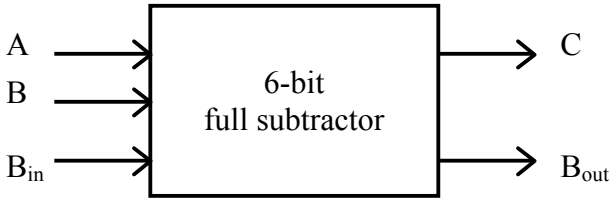

Figure 1 Block diagram of the system

III. Instructions

1. Create a new project in ModelSim. Then, develop and simulate your design in the program. Finally, display your results in the wave window of the program at least 3 samples.

2. Add or change time delay of your full subtractor. Show the simulation, describe the difference from the pervious simulations and explain the reason.

3. Draw a completed block diagram of your design showing both internal and external signals.

IV. Deliverables

1. **No** demonstration is required
2. **Pre- Lab**: No Pre-Lab is required.
3. **Report**:
   a. Objective
   b. Lab work:
      - Briefly describe your design
      - Print and comment the results including your codes
      - Draw block diagram
   c. Conclusion: What went wrong? Why? , And how did you solve it?

V. Grading

This lab has 15 points (12 lab work, and 3 organized and neat report format).