VHDL AND PROGRAMMABLE LOGIC DEVICES

LAB#1
DESIGN SIMULATION USING MODELSIM I

I. Objective
This objective of this lab is to make students familiar with the process of simulation and simulation and verify the functionality of VHDL code by using ModelSim.

II. Problems
1. Creating a project in ModelSim and VHDL coding
2. Compiling and debugging project files
3. Simulating the design

III. Instructions
1. Creating a project
Open the program by clicking "**Start**" → "**All program**" → "**Electrical Enge Software**" → "**Modelsim SE**" → "**Modelsim**"

Next "**File**" → "**New**" → "**Project**", then the following "Create Project" window (Fig.1) will appear. You need to enter a project name, a project location, and leave the "Default Library Name" to work. Click "OK" when finished.
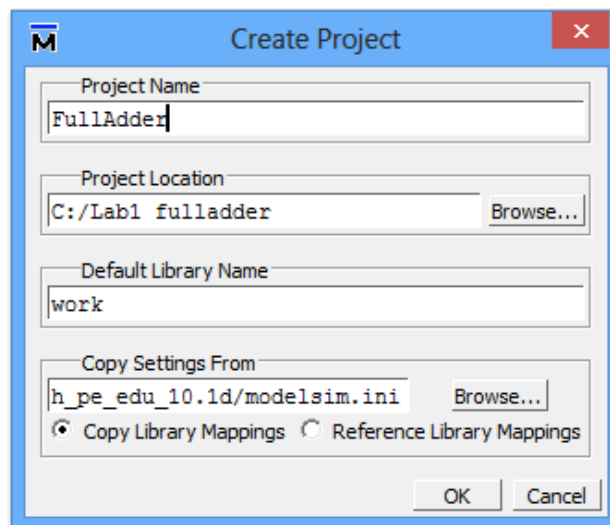

Fig.1 : Create New Project Window

A new window (Fig.2) will appear. You now have three options to add files to the project:
- You can create new VHDL files (from scratch) and then add them to the project, or
- You can add already existing files to the project, or
- You can do a combination of the two operations by combining the two above operations.
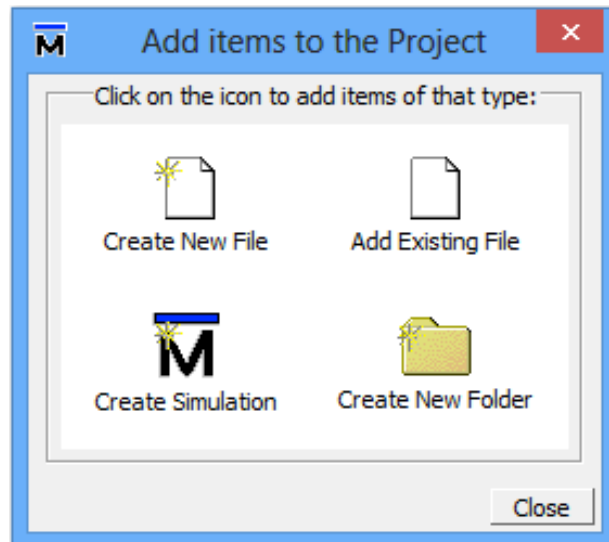
Fig.2 : New Project Window

1.1 Creating a new VHDL file from Scratch

Click on "**Create New File**" to create a new blank file. If you have closed the "Add items to the Project" window, then select "**Project**" → "**Add to Project**" → "**New file**"

Then the "**Create Project File**" window will appear (Fig.3). Select an appropriate file name (we use Adder4 in this lab) for the file you want to add; choose VHDL as the "Add file as type" option and Top level as the "Folder" option. Click "OK" when finished.
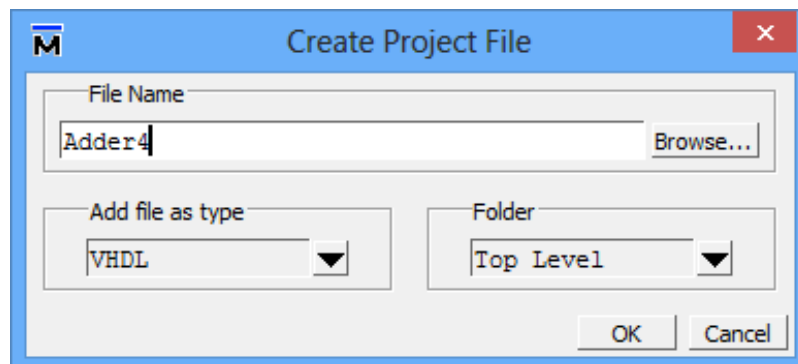

Fig.3: "Create Project File" dialog window

On the "Workspace" section of the Main Window (Fig.4), double-click on the file you have just created (Adder4.vhd in this lab).
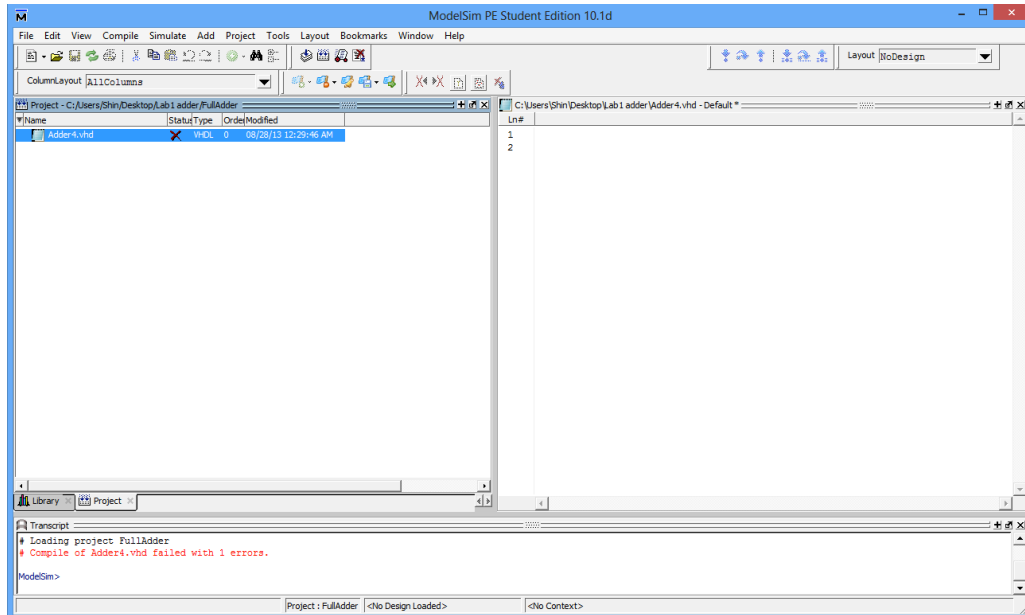

Fig.4: "ModelSim's Main Window"

Type in your code in the new window. For this tutorial, you will use below code.

```vhdl
1    library IEEE;
2    use IEEE.std_logic_1164.all;
3
4    entity adder4 is
5      port(A,B: in std_logic_vector(3 downto 0);
6        Ci: in std_logic; -- Inputs
7        S:  out std_logic_vector(3 downto 0);
8        Co: out std_logic); -- Output
9      end adder4;
10
11   Architecture Structure of adder4 is
12
13     component FullAdder
14       port(X,Y,Cin: in std_logic; -- Inputs
15             Cout,Sum: out std_logic); --Outputs
16       end component;
17
18     signal C: std_logic_vector(3 downto 1);
19     begin
20     FA1: Fulladder port map (A(0),B(0), Ci, C(1), S(0));
21     FA2: Fulladder port map (A(1),B(1), C(1), C(2), S(1));
22     FA3: Fulladder port map (A(2),B(2), C(2), C(3), S(2));
23     FA4: Fulladder port map (A(3),B(3), C(3), Co, S(3));
24   end Structure;
```

Fig.5: Code for Adder4.vhd

Save your code "**File**" → "**Save**"

1.2 Creating your own FullAdder.vhd

Refer to step 1.1 to open a new blank file (FullAdder.vhd), then make your own a full adder to use as the component in Adder4.vhd.

2. Compiling and debugging project files

Select "Compile" → "Compile All" to compile the project

The compilation result is shown on the main window (Fig.6). A red message indicates that there is an error in the code.


```
Transcript
# Compile of Adder4.vhd failed with 2 errors.
# Compile of FullAdder.vhd was successful.
# 2 compiles, 1 failed with 2 errors.

ModelSim>
```
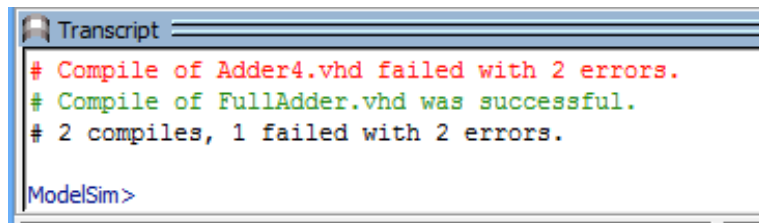
Fig.6: Compilation error in the transcript window

Double-click on the error (shown in red) in the main window. This will open a new window that describes the nature of the error. In this case the error message is as follows (Fig.7),


```
M                      ...1 adder/Adder4.vhd  -- Unsuccessful Compile          ×

vcom -work work -2002 -explicit {C:\Users\Shin\Desktop\Lab1 adder\Adder4.vhd}
Model Technology ModelSim PE Student Edition vcom 10.1d Compiler 2012.11 Nov  2 2012
-- Loading package STANDARD
-- Loading package TEXTIO
-- Loading package std_logic_1164
-- Compiling entity adder4
-- Compiling architecture Structure of adder4
** Error: C:\Users\Shin\Desktop\Lab1 adder\Adder4.vhd(24): near "EOF": expecting ';'

                                                                          Close
```
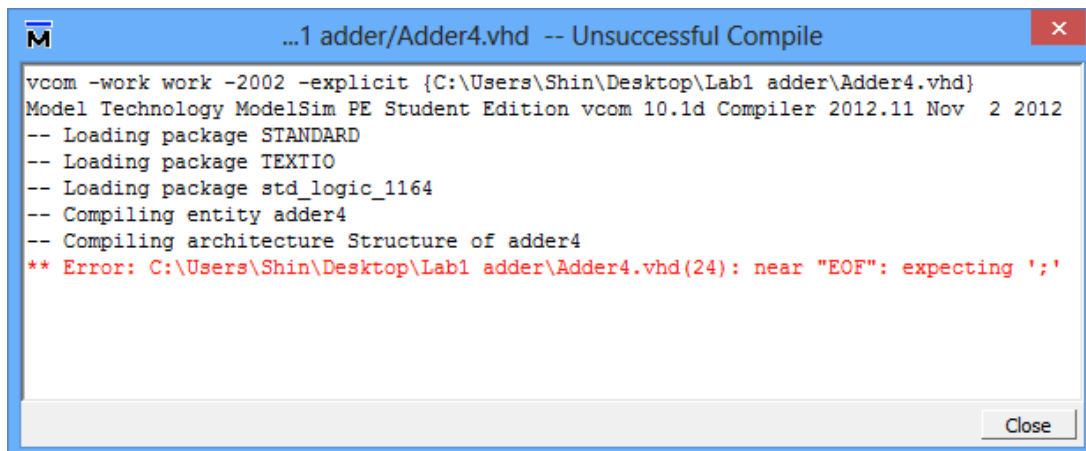
Fig.7: Error message

Double-click on the Error message. The error is highlighted in the source window (Fig.8)

```
19      begin
20      FA1: Fulladder port map (A(0),B(0), Ci, C(1), S(0));
21      FA2: Fulladder port map (A(1),B(1), C(1), C(2), S(1));
22      FA3: Fulladder port map (A(2),B(2), C(2), C(3), S(2));
23      FA4: Fulladder port map (A(3),B(3), C(3), Co, S(3));
24      end Structure
```

Fig.8: The error line is highlighted

3. Simulating the design.

Click on the "Library" tab of Workspace section in the main window and then click on the plus sign next to the work library. You should see the entity names of the codes that you have just compiled i.e., "adder4" and "fulladder". (Fig.9)

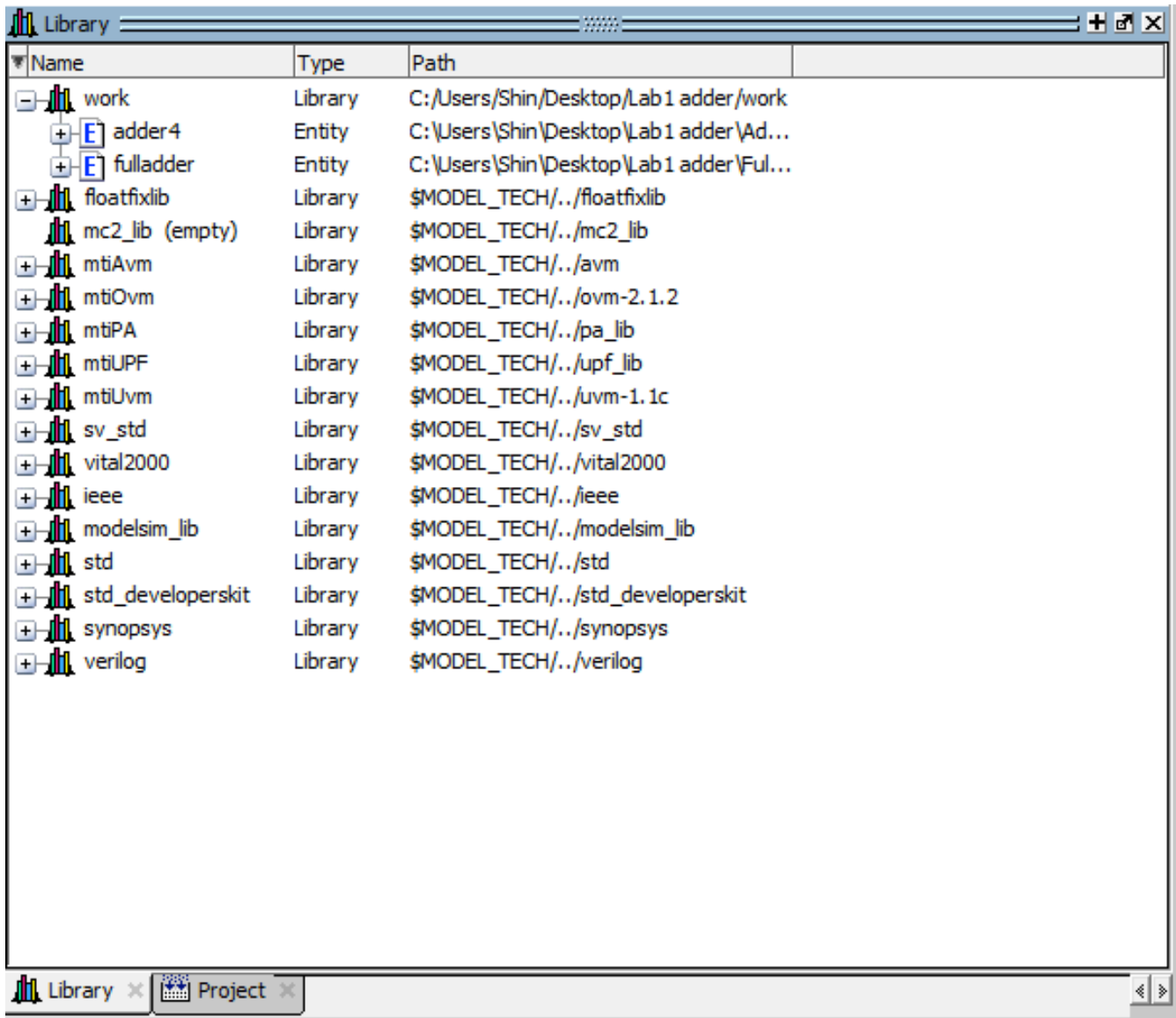| Name	Type	Path
work	Library	C:/Users/Shin/Desktop/Lab1 adder/work
adder4	Entity	C:\Users\Shin\Desktop\Lab1 adder\Ad...
fulladder	Entity	C:\Users\Shin\Desktop\Lab1 adder\Ful...
floatfixlib	Library	$MODEL_TECH/../floatfixlib
mc2_lib (empty)	Library	$MODEL_TECH/../mc2_lib
mtiAvm	Library	$MODEL_TECH/../avm
mtiOvm	Library	$MODEL_TECH/../ovm-2.1.2
mtiPA	Library	$MODEL_TECH/../pa_lib
mtiUPF	Library	$MODEL_TECH/../upf_lib
mtiUvm	Library	$MODEL_TECH/../uvm-1.1c
sv_std	Library	$MODEL_TECH/../sv_std
vital2000	Library	$MODEL_TECH/../vital2000
ieee	Library	$MODEL_TECH/../ieee
modelsim_lib	Library	$MODEL_TECH/../modelsim_lib
std	Library	$MODEL_TECH/../std
std_developerskit	Library	$MODEL_TECH/../std_developerskit
synopsys	Library	$MODEL_TECH/../synopsys
verilog	Library	$MODEL_TECH/../verilog

Library ✕ | Project ✕

Fig.9: Library window

Double-click on the top level entity to load the design (In this lab, adder4 is the top level entity). This will open a third tab "sim" in the main window.

Now select "**View**" → "**Objects**" from the main window to open the Objects window if it does not appear (Fig.10).
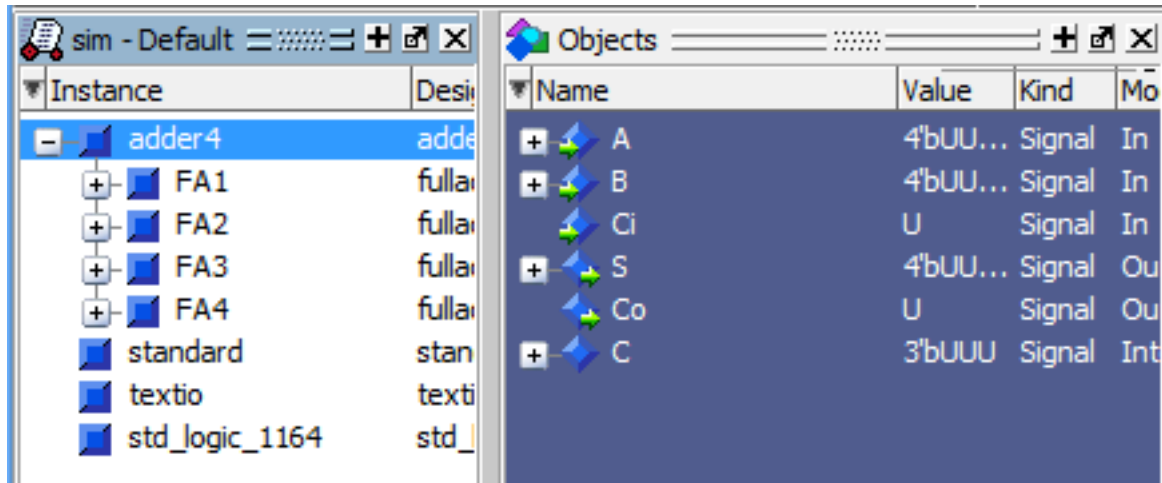
Fig.10: sim window and Objects window

Then, select "**Add**" → "**To Wave**" → "**All items in region**" to open wave window (Fig.11).
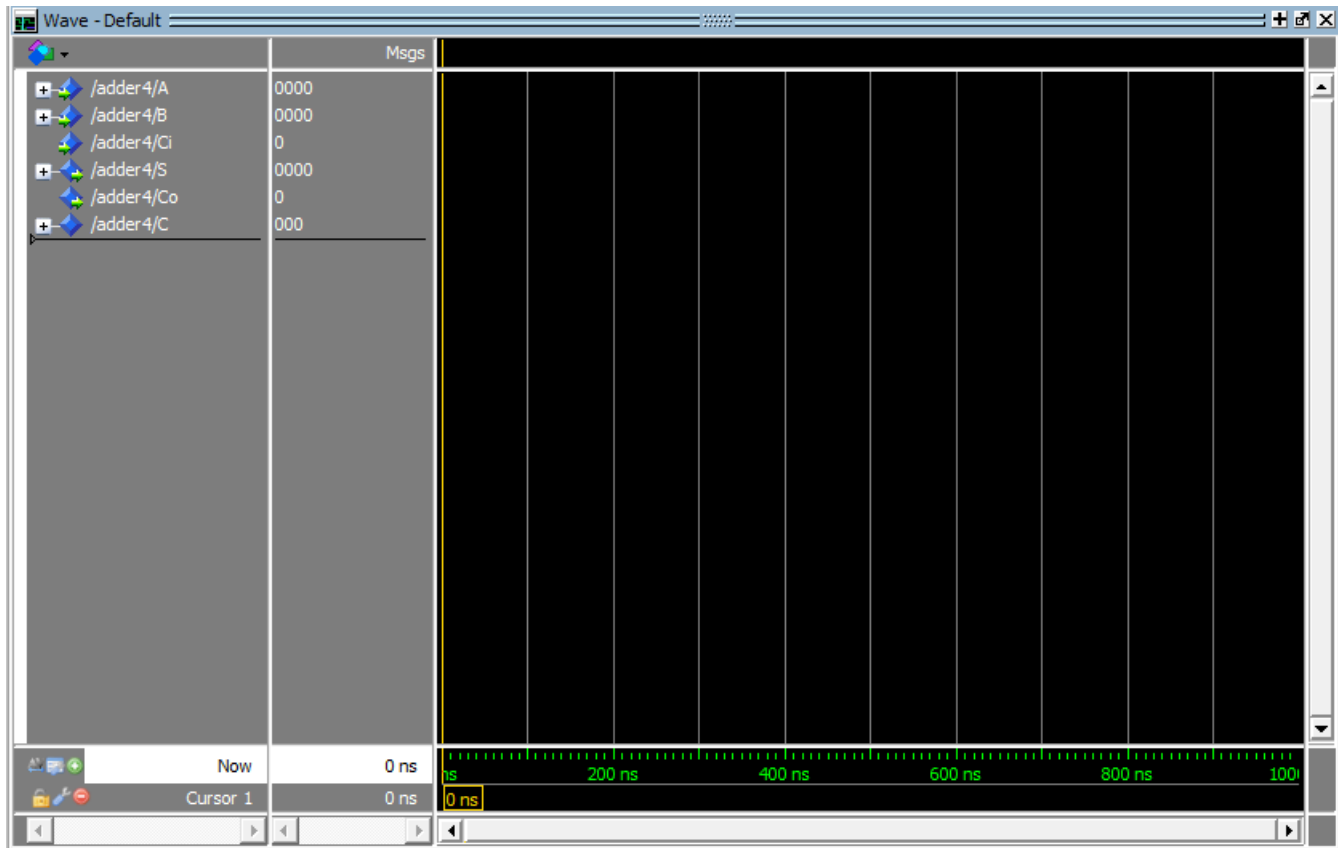

Fig.11: Wave window

Now you are ready to simulate this design. Before you do this, you need to set the input signal value. In the wave window, right-click on the signal that you want to set the value, and select "Force" (Fig.12), then it will appear a new window (Fig.13). Enter the value in the new window, then click OK to finish. Repeat this to set every signal that you want to set the input value. (In this lab, you need to set signal a, signal b, and signal ci. For example, Set a <= 0101, b <= 0111, ci <= 0.)
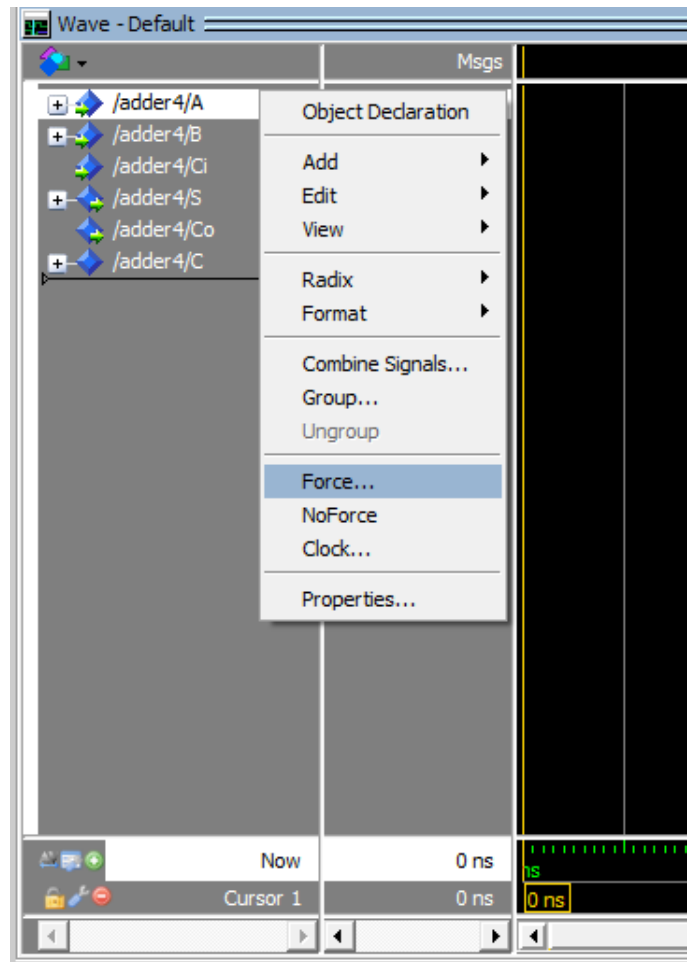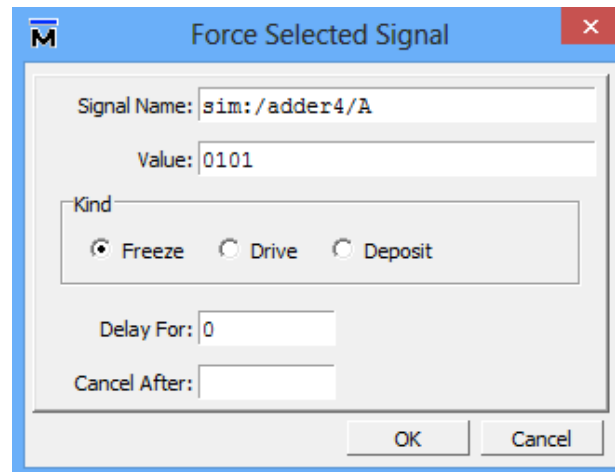
Fig.12: Click Force to assign the value

Fig.13: Force signal window

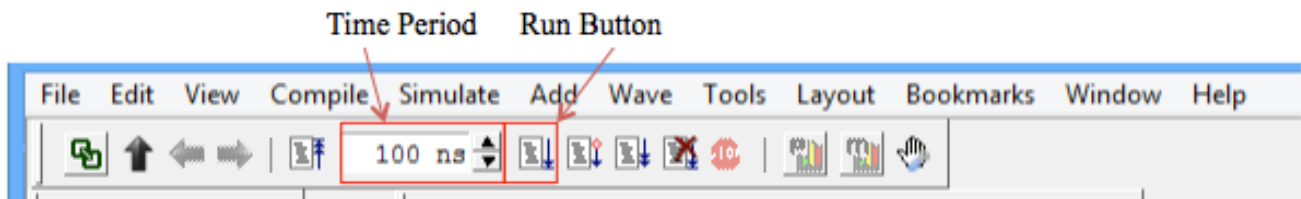Now set the simulation period and click the run button next to it (Fig.14).
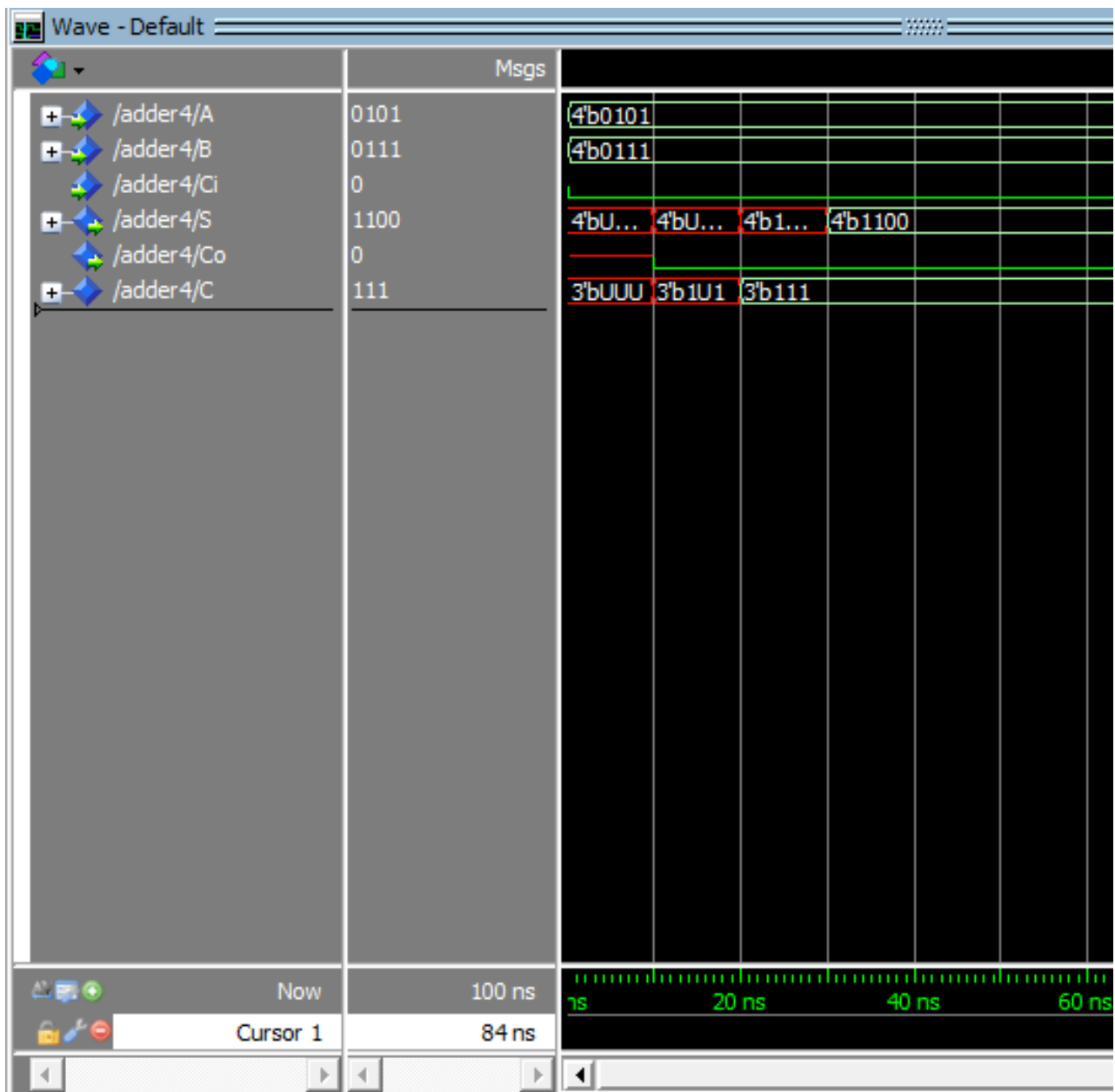

Fig.14: Run the simulation

Fig.15: Simulation result

IV. Lab Requirements:

Complete the above lab procedure and print the final results. Simulate at least 3 additions showing that your design can work successfully. Then, <u>briefly describe</u> about the function and the syntax of port-map statements? For example, in our Adder4.vhd, why does the order have to be *port map (A(0),B(0),Ci,C(1),S(0))*?

V. Deliverables
1. **No** demonstration is required
2. **Pre- Lab**: No Pre-Lab is required.
3. **Report**:
    a. Objective
    b. Lab work: See IV above.
      i. Print and comment the results.
      ii. Answer the question.
    c. Conclusion: What went wrong? Why? , And how did you solve it?

V. Grading
This lab has 15 points (12 lab work, and 3 organized and neat report format).