ECE 4250/7250
VHDL AND PROGRAMMABLE LOGIC DEVICES

LAB #4
4 Bit Full Adder Implementation on Xilinx Spartan-3

I. Objective

The objective of creating a project, synthesizing and implementing a simple design to the NEXUS4 FPGA board by downloading using the VIVADO Project Navigator. Mainly, you will implement a 4---bit full adder displayed by 2 LED displays on the board.

II. Procedure

a. Creating and adding a project source codes in VIVADO provided Project Navigator, completing in advance.

b. Synthesizing the design and viewing the RTL schematic.

c. Going through and placing the process and routing of translating, mapping, to implement the design.

d. Generating programming file and configuring the device.

e. Displaying the result on LCDs and testing the design.

III. Instructions

a. Open the six attached (.vhd) files and the (.XDC) file that you have downloaded.

b. The .XDC file is complete, and there is no need to modify it.

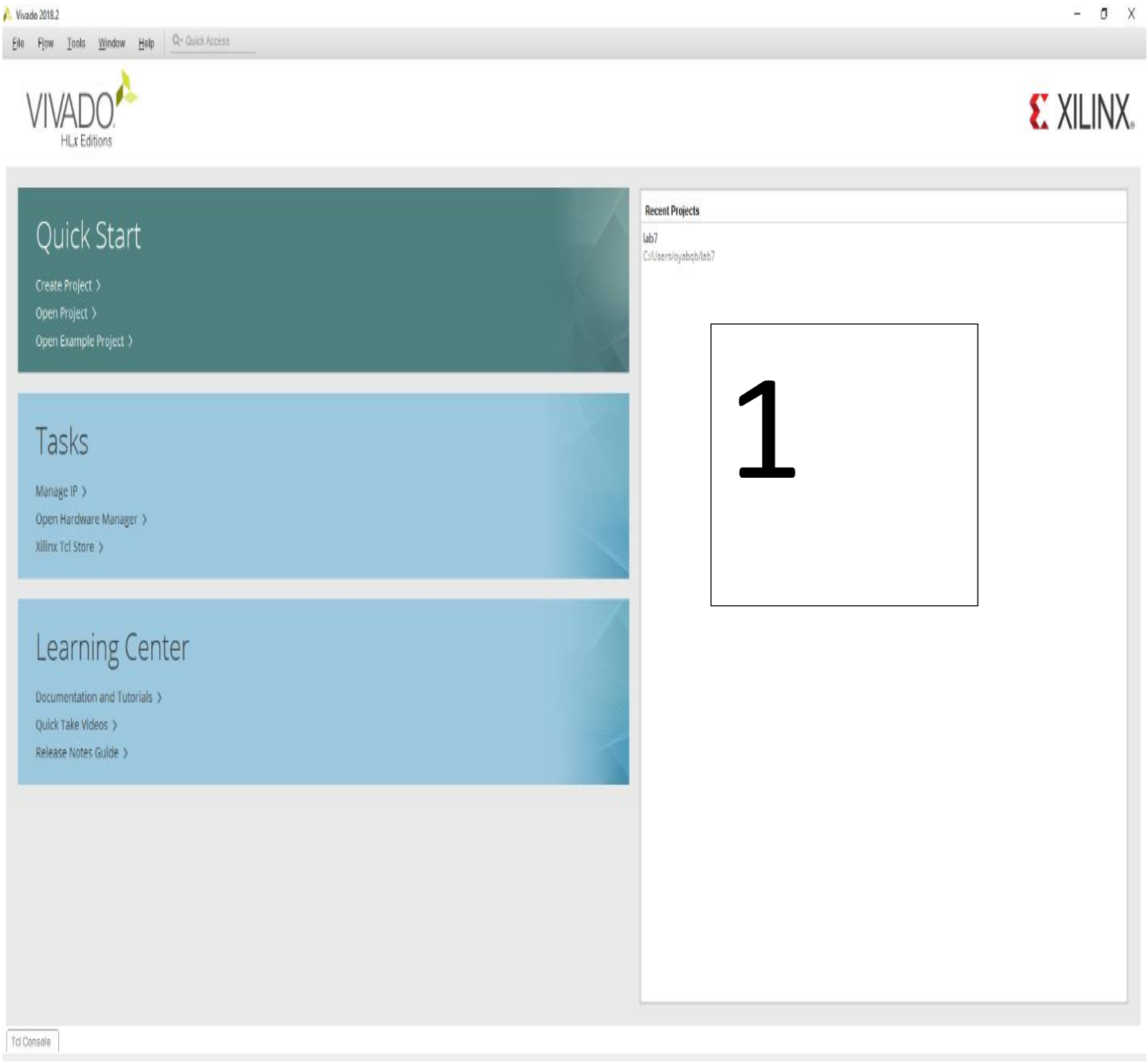
c. **You will need to complete the syntax and some part of the VHD files**. At every location where you would need to fill in with code, you will see a comment.

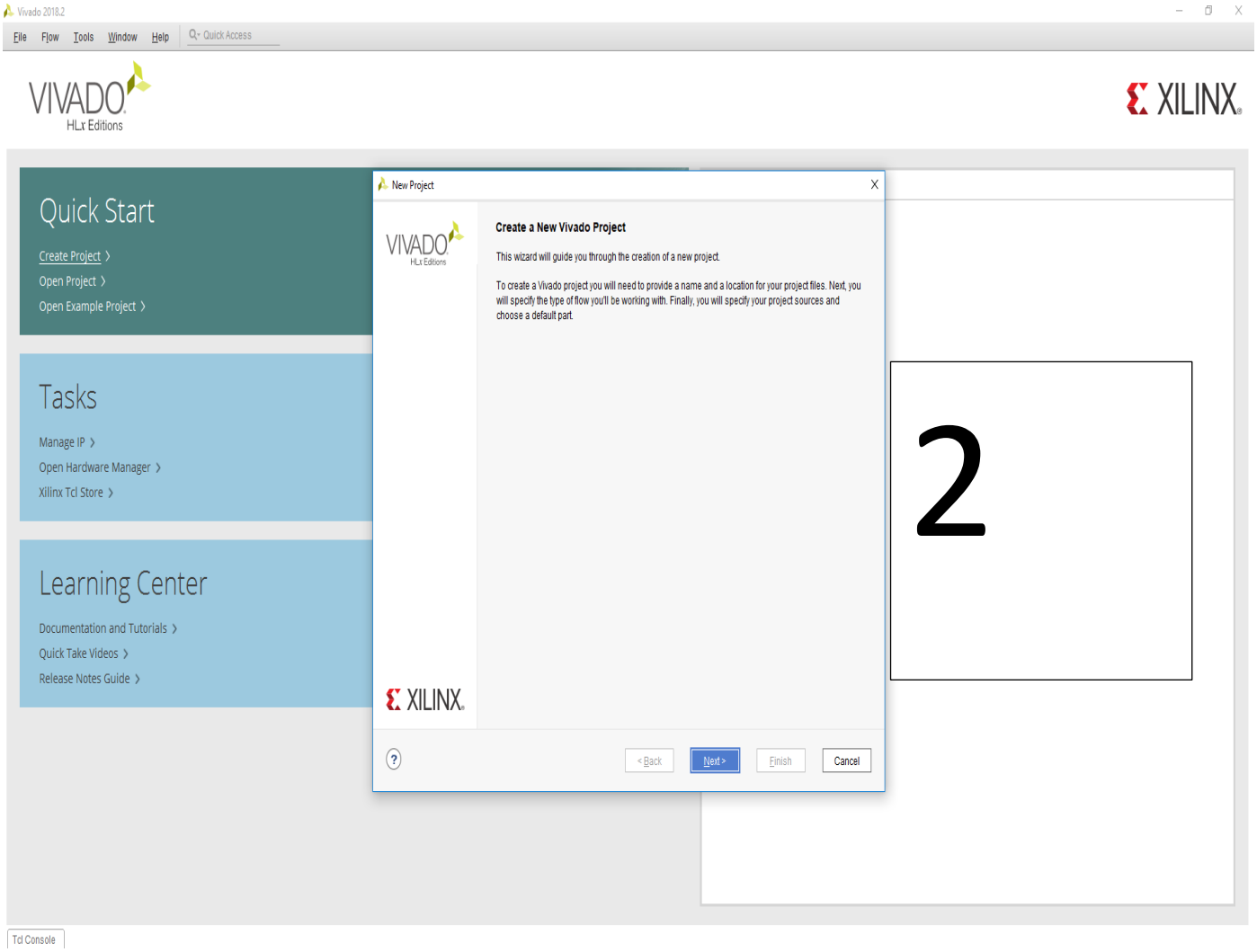
1. Creating a project

Open the program by clicking "**Start**" then "**All program**" then "**xilinex design tools**" then left click on the **VIVADO 2018.2** The welcome screen will show up.(figure1).

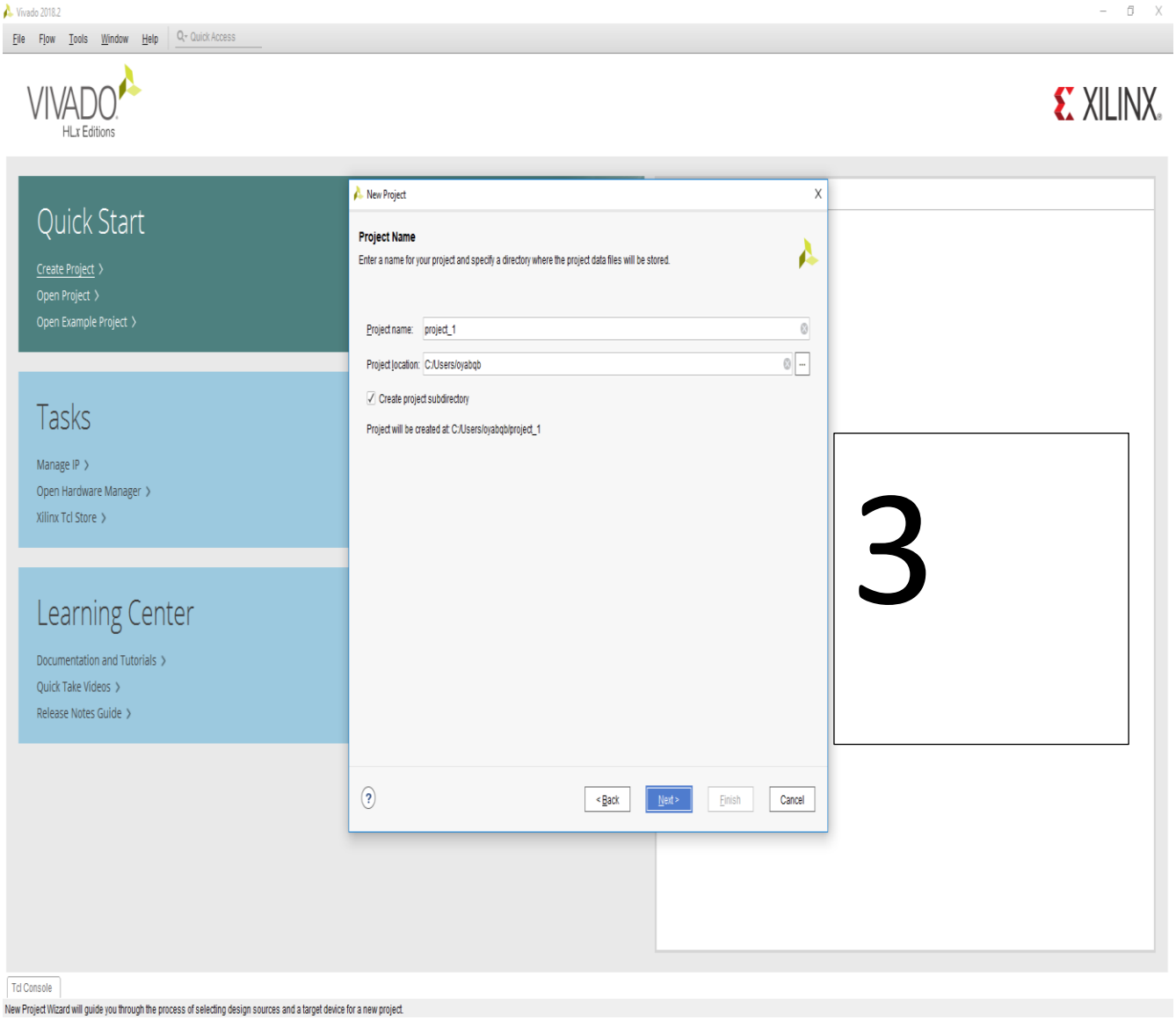
Using **quick start** submenu select **create project** the **creating new vivado project screen** window will pop up to the screen.(figure2).

Click **NEXT…**

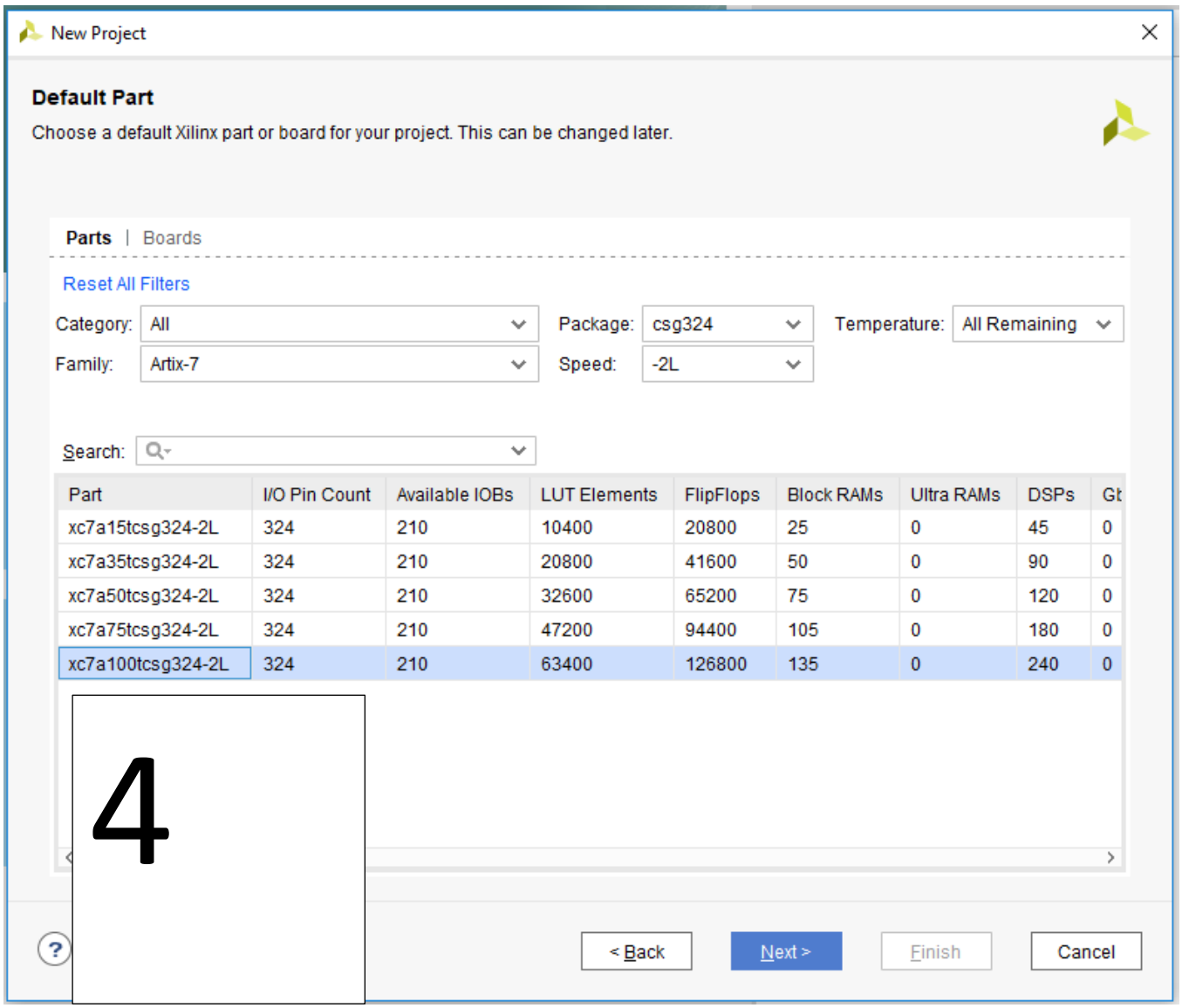

Vivado 2018.2
File Flow Tools Window Help Quick Access
VIVADO
HLx Editions
XILINX
Quick Start
Create Project
Open Project
Open Example Project
Tasks
Manage IP
Open Hardware Manager
Xilinx Tcl Store
Learning Center
Documentation and Tutorials
Quick Take Videos
Release Notes Guide
Recent Projects
lab7
C:/Users/oyabqb/lab7
1
Tcl Console



- The **NEW PROJECT** window will appear now you can select the location and name of your project through this screen (Always select destination path in your account folder). (as shown in figure.3) Press **Next…**



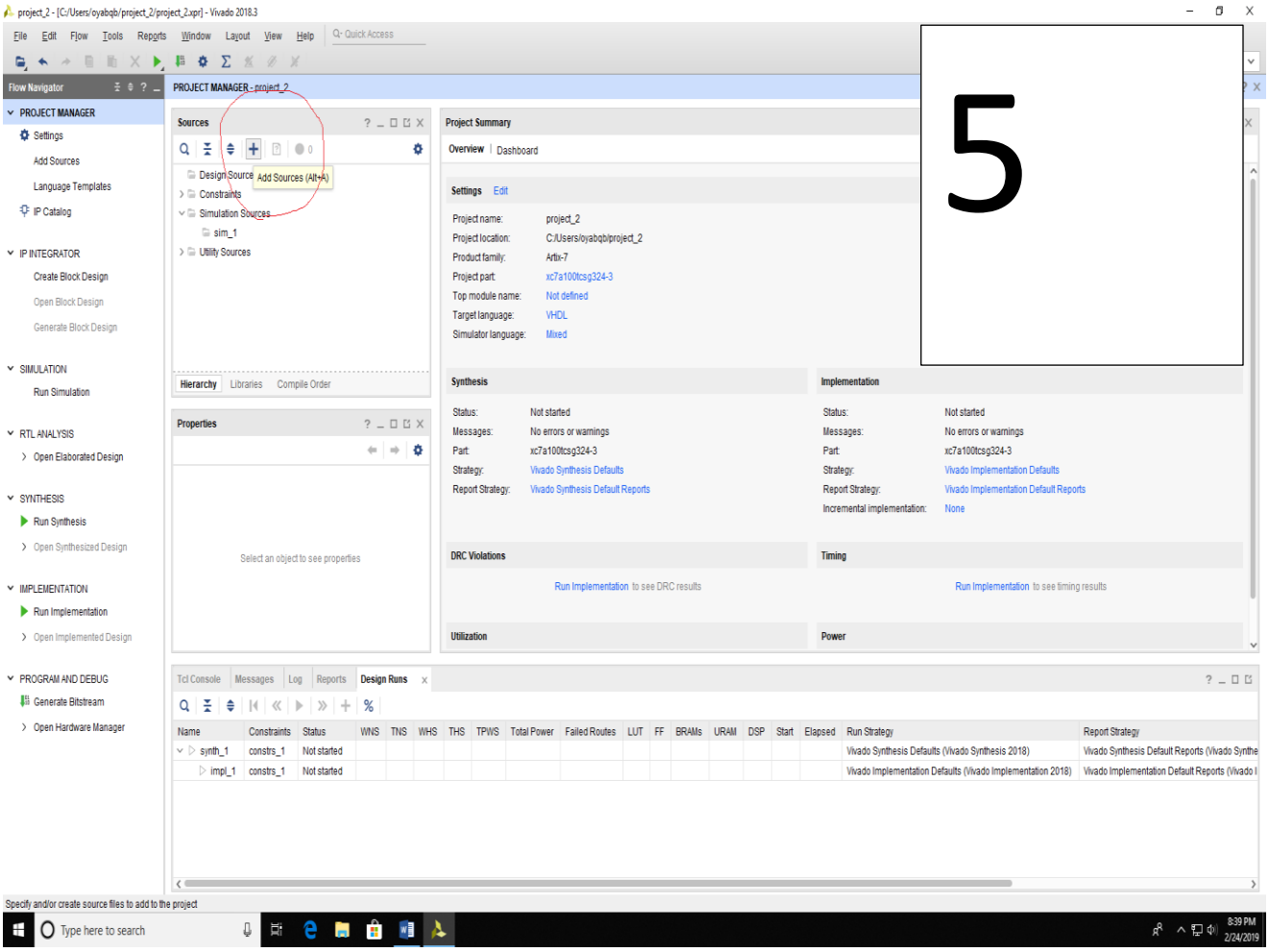
- The **PROJECT TYPE** window will show up and we always select **RTL PROJECT** then click **NEXT…**
- **(Note)** For this experiment only active creating file from scratch by clicking the tick of **Do not specify sources at this time**.
- The Default Part window that used to set the properties of your project and the hard ware used will show up in this window please follow the attached figure to set your values.(figure 4). Then after setting all properties click **NEXT..**
- New Summary Project window will appear to summarize all the options you select. Click **Finish.**

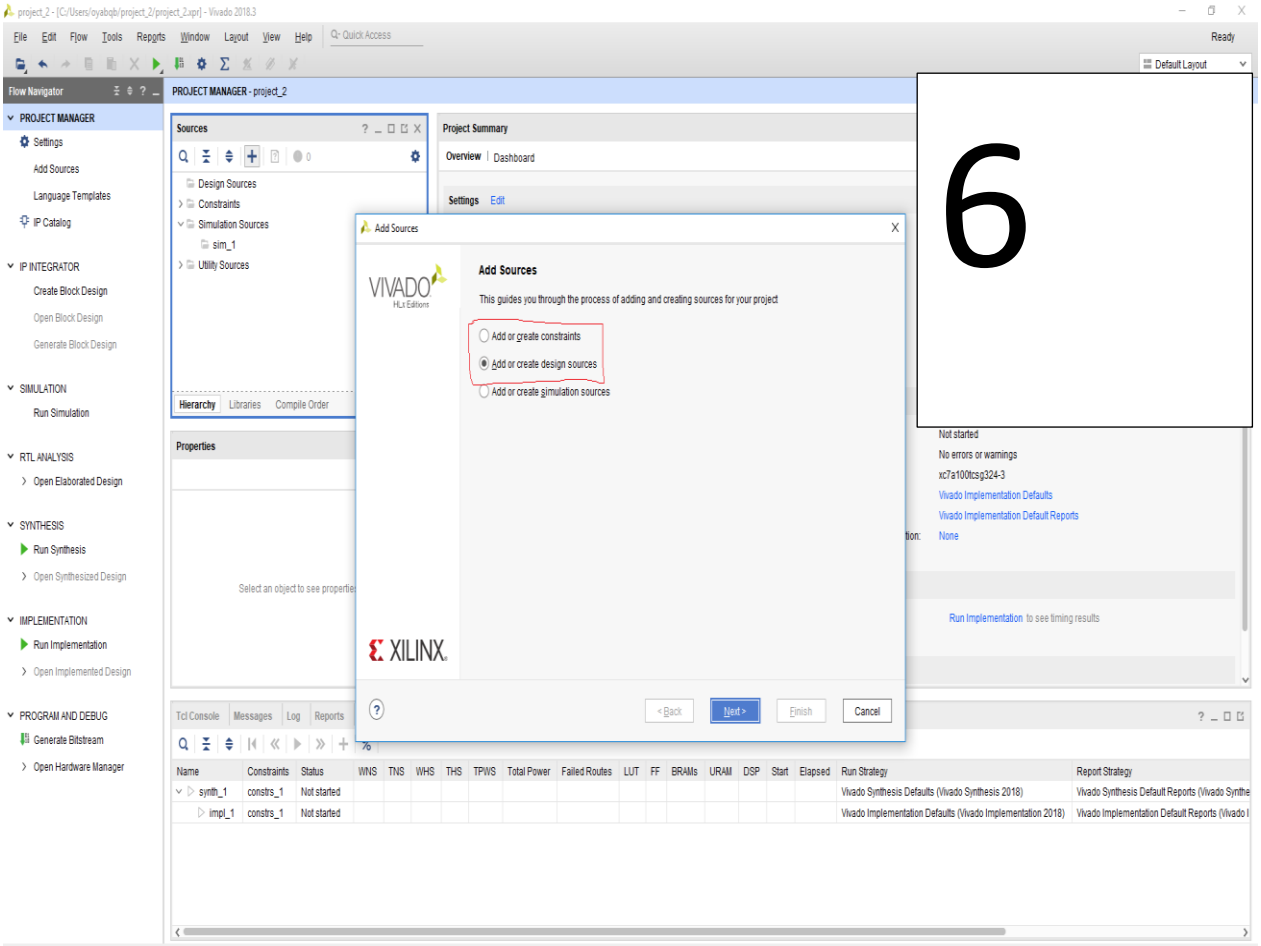

New Project
Default Part
Choose a default Xilinx part or board for your project. This can be changed later.
Parts | Boards
Reset All Filters
Category: All
Package: csg324
Temperature: All Remaining
Family: Artix-7
Speed: -2L
Search:
Part I/O Pin Count Available IOBs LUT Elements FlipFlops Block RAMs Ultra RAMs DSPs Gt
xc7a15tcsg324-2L 324 210 10400 20800 25 0 45 0
xc7a35tcsg324-2L 324 210 20800 41600 50 0 90 0
xc7a50tcsg324-2L 324 210 32600 65200 75 0 120 0
xc7a75tcsg324-2L 324 210 47200 94400 105 0 180 0
xc7a100tcsg324-2L 324 210 63400 126800 135 0 240 0
4
< Back
Next >
Finish
Cancel

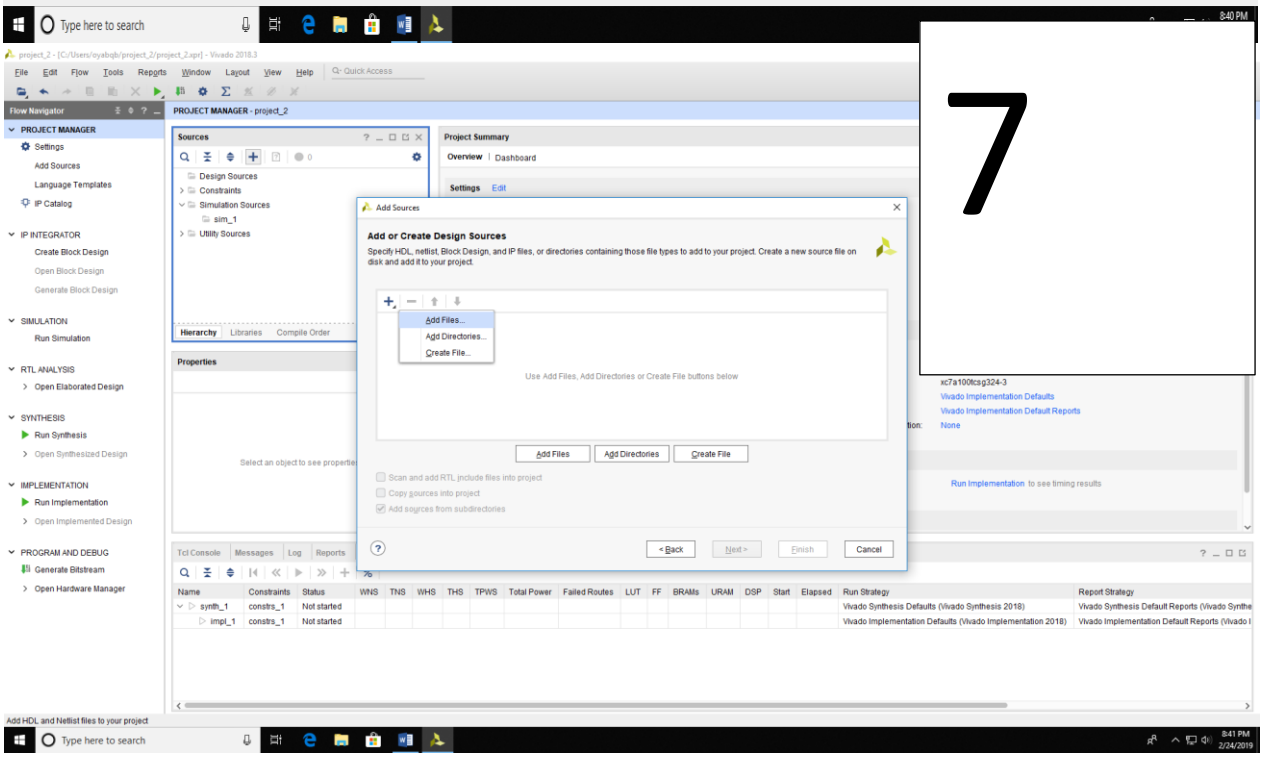
2-Adding Source files to the project

After Finish setting up your VIVADO, Next step is to add files and constrain to your project.

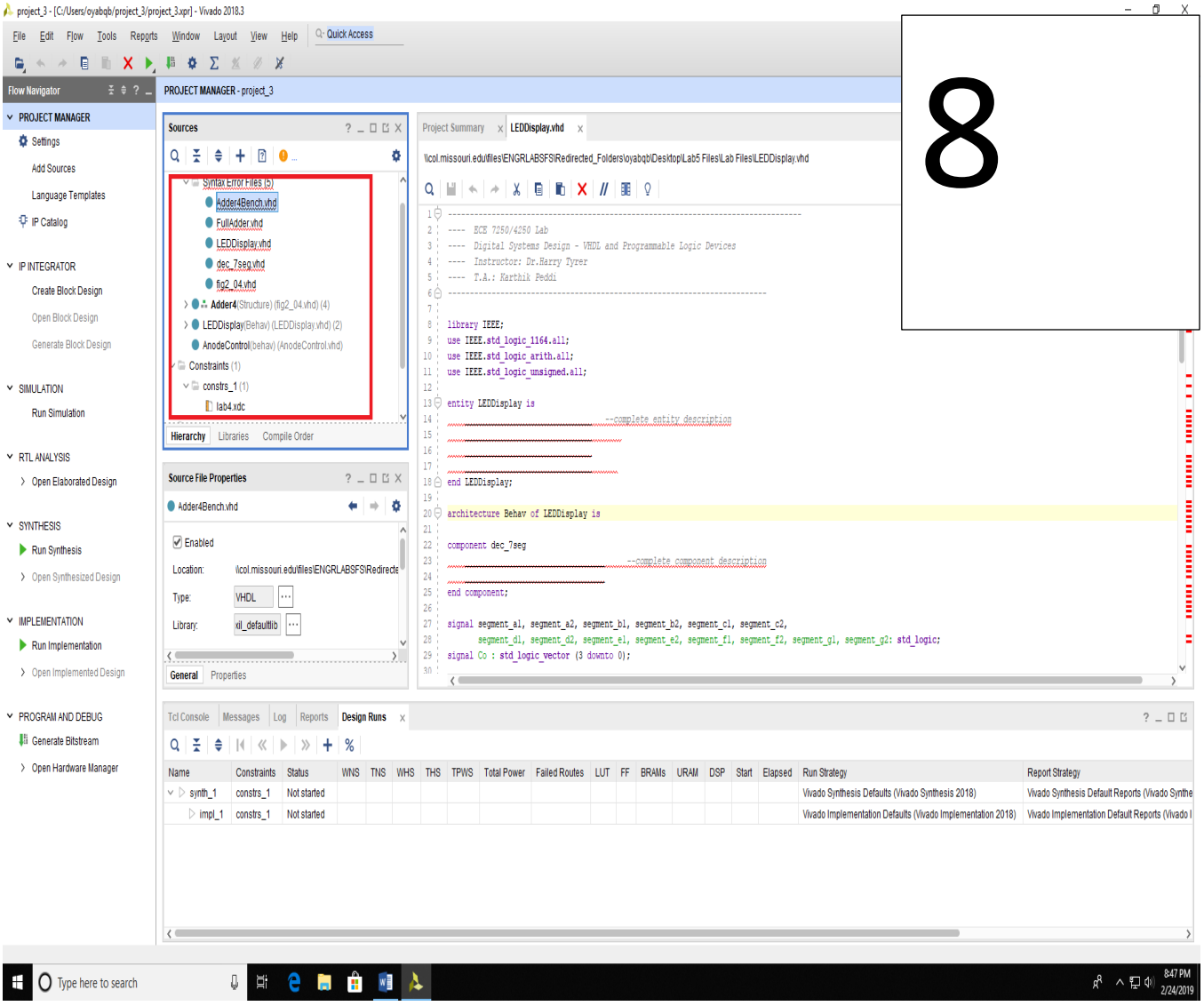
A-from the source window (Plus Sign) add your downloaded files as “Design Source files” as shown figure 5, 6,7. You should add up all your 6 files (Adder4Bench, LED Display, Anode Control, dec_7seg, fig2-4, Full Adder).




6
Add Sources
Add Sources
This guides you through the process of adding and creating sources for your project
Add or create constraints
Add or create design sources
Add or create simulation sources
VIVADO
XILINX
< Back
Next >
Finish
Cancel


7
Add Sources
Add or Create Design Sources
Specify HDL, netlist, Block Design, and IP files, or directories containing those file types to add to your project. Create a new source file on disk and add it to your project.
Add Files...
Add Directories...
Create File...
Use Add Files, Add Directories or Create File buttons below
Add Files
Add Directories
Create File
Scan and add RTL include files into project
Copy sources into project
Add sources from subdirectories
< Back
Next >
Finish
Cancel

Repeat the same procedure with constrain file (.XRD) you should end up adding all required files and constrains as shown figure 8.

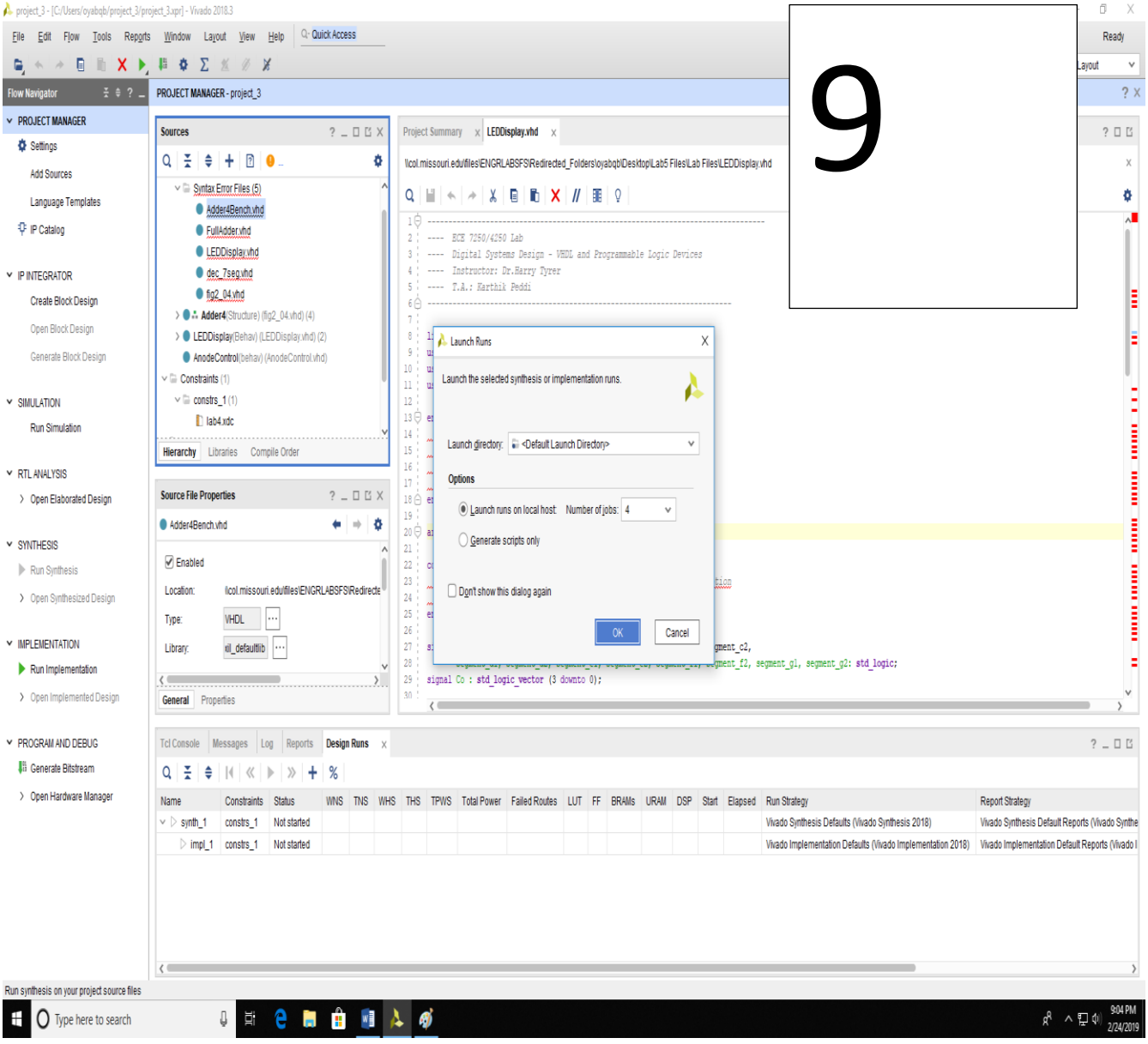


After You finish fill in all blank spaces in all files you can go to the synthesis step.

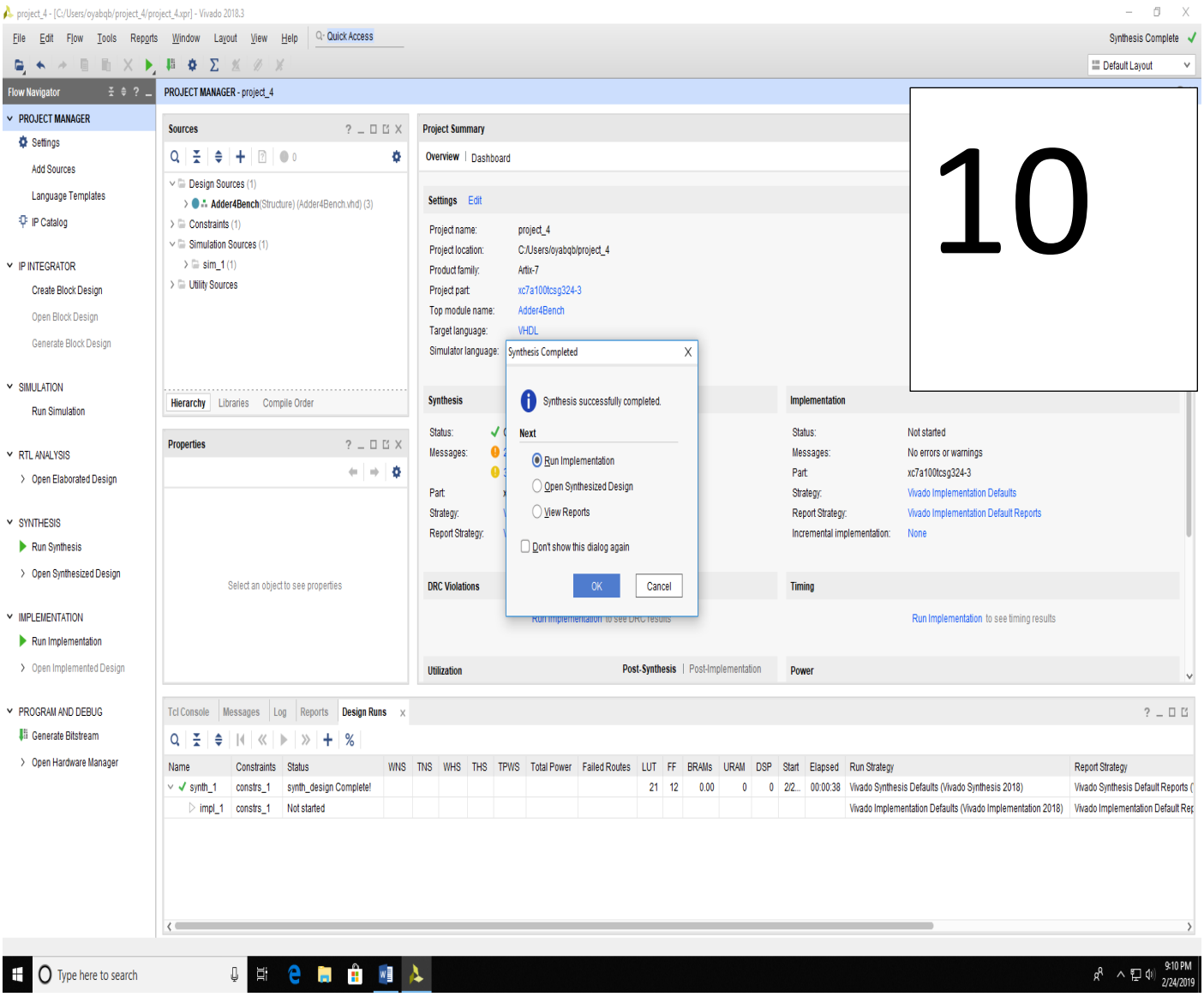
Note(Do NOT edit the .XDC) file it already completed for you this time.

3. Synthesizing the project

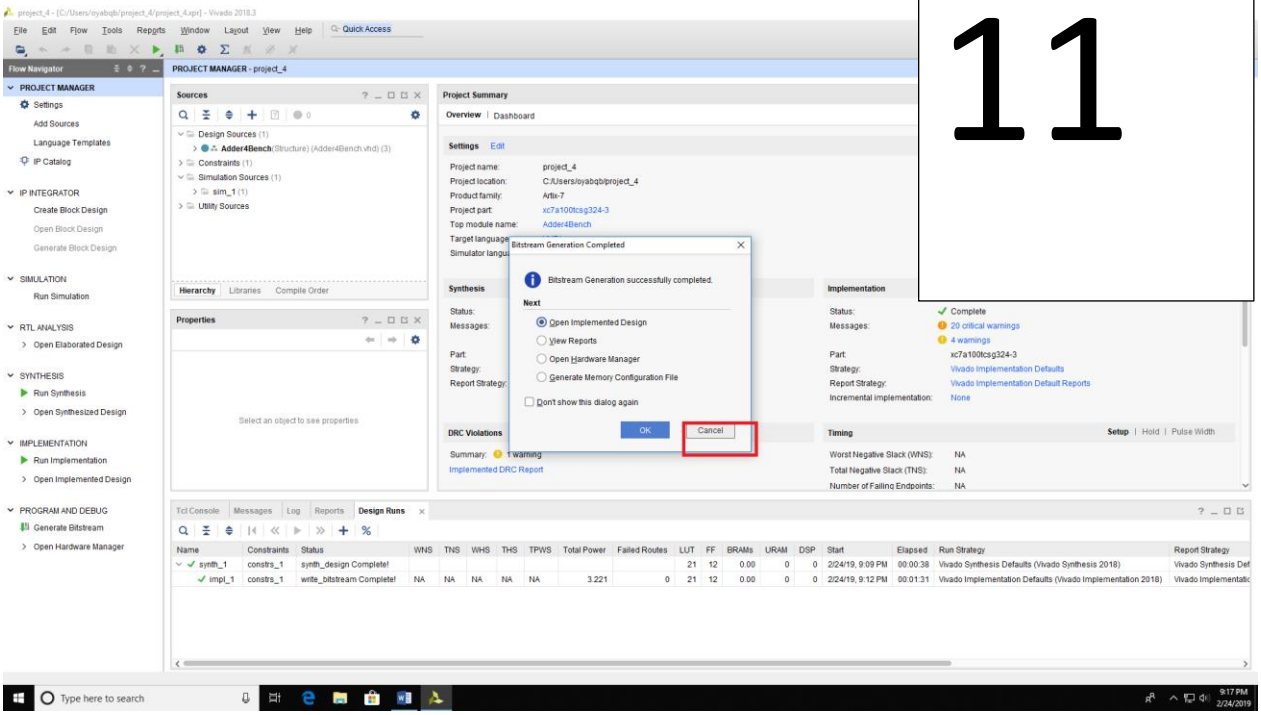
Click on RUN synthesis on the Project Manager Window then press ok on the next screen as show in figure 9.



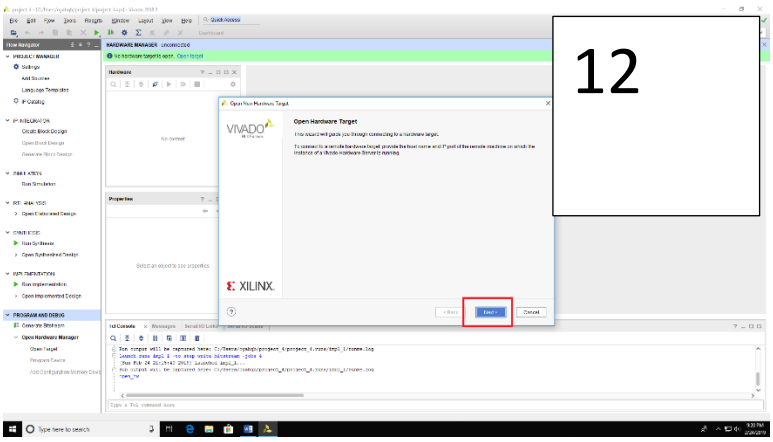
When synthesis finished the following window will pop up click OK then OK on the next screen and wait for the Implementation step finish.as shown figure 10 the

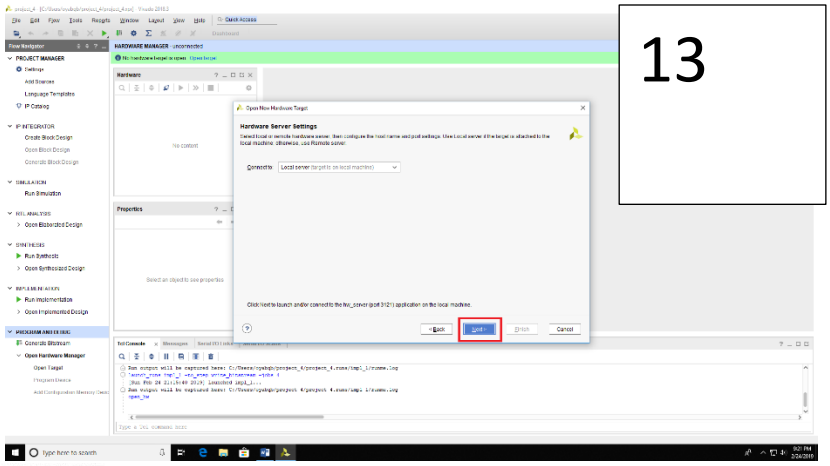


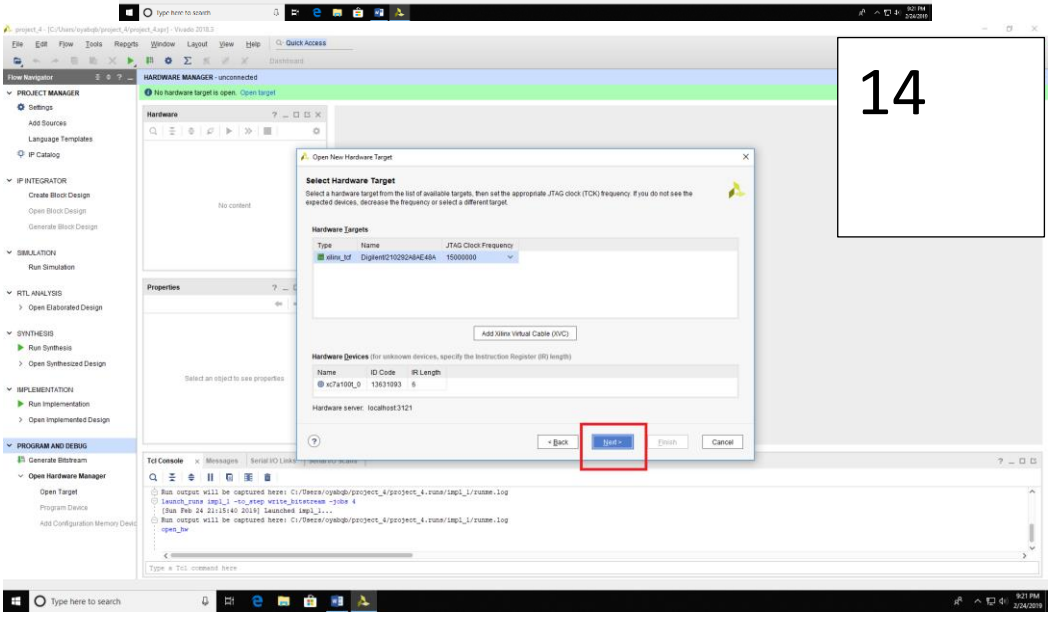
Select GENERATE BIT STREAM on the next window and then press OK in order to generate downloadable file by the NEXS 4 FPGA. When the generation finished the following screen will pop up click on CANCEL (As shown in figure 11)



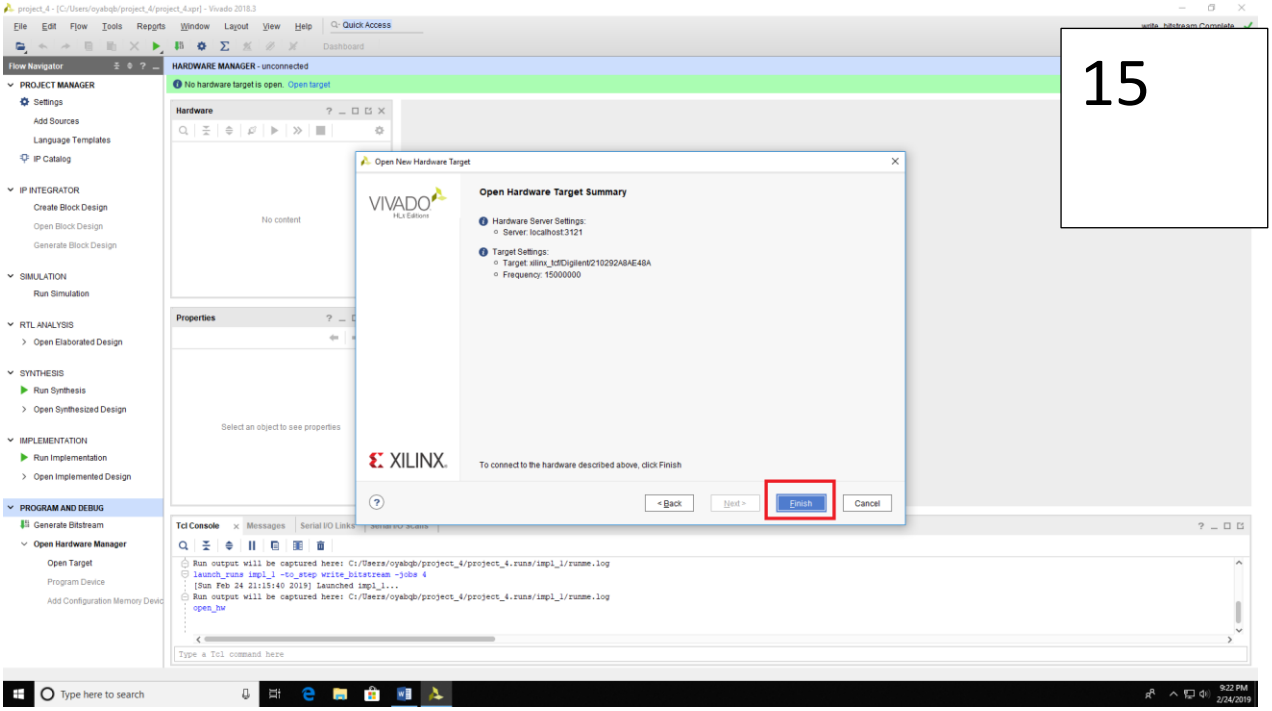
NEXT, open Hardware manager under **program and debug** in **the Project Manager window** and click on open target then open new target. Next follow figures (12-15) to prepare file to download into our hardware.

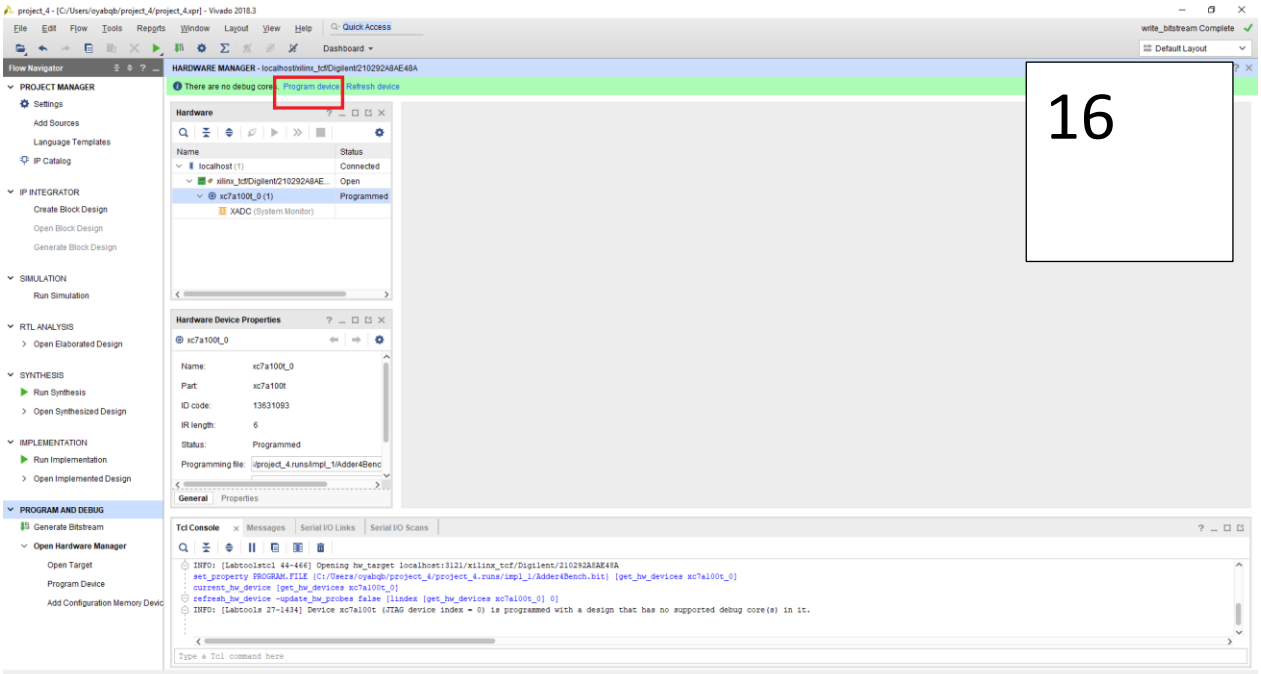


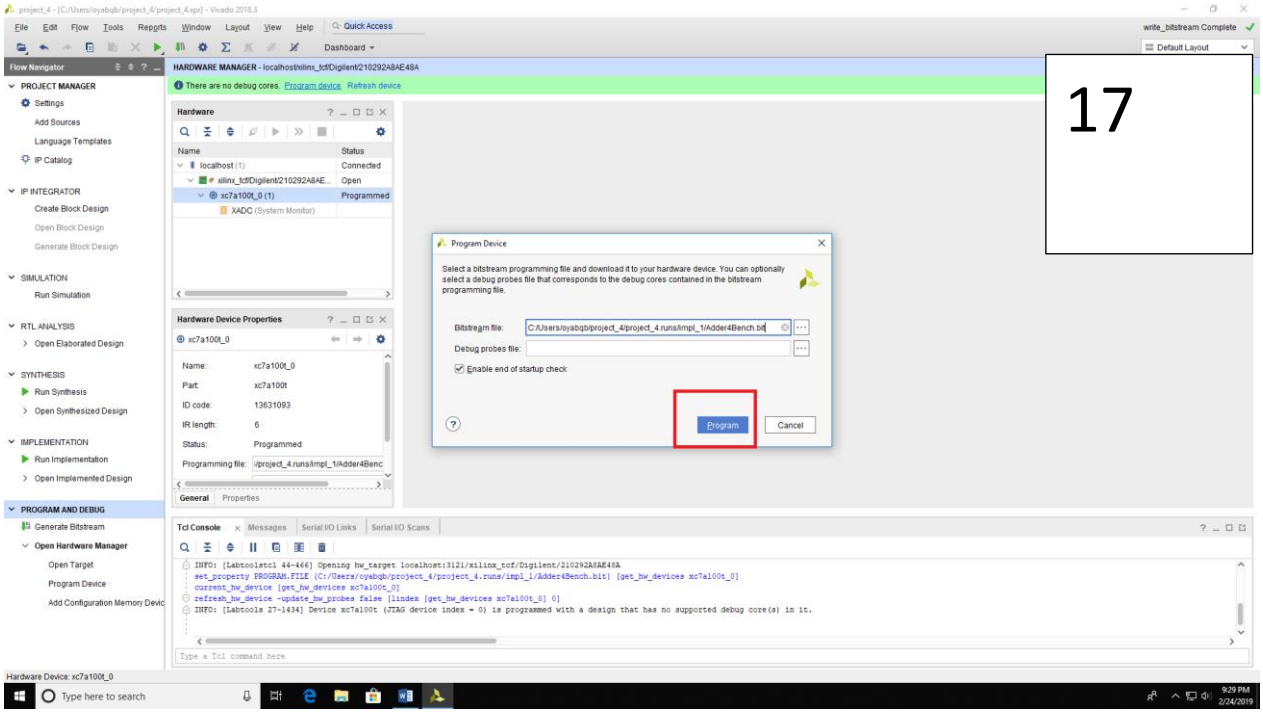




Finally you will be able to download the bit stream file you created into your hardware by click on program device then follow the figures(16 and 17)


Open New Hardware Target
VIVADO
Open Hardware Target Summary
Hardware Server Settings:
Server: localhost:3121
Target Settings:
Target: xilinx_tcf/Digilent/210292A8AE48A
Frequency: 15000000
XILINX
To connect to the hardware described above, click Finish
< Back
Next >
Finish
Cancel


16


17
Program Device
Select a bitstream programming file and download it to your hardware device. You can optionally select a debug probes file that corresponds to the debug cores contained in the bitstream programming file.
Bitstream file:
C:/Users/oyabqb/project_4/project_4.runs/impl_1/Adder4Bench.bit
Debug probes file:
Enable end of startup check
Program
Cancel

Deliverables

1. Demonstration is required
2. Report:
    1. Objective
    2. Lab work:
        a. Implementation: write a note on how the .vhd files involved in the code and the working of the program in general.
        b. Answer the following questions:
            i. What is the function of the XDC file?

        c. Conclusion: what went wrong? Why? How was it solved?
3. Grading: Total points 25
    1. Demonstration: 15 points
    2. Report: 10 points