# ECE 4250/7250
# VHDL AND PROGRAMMABLE LOGIC DEVICES

# LAB#5
# SIMULATION TEST BENCH OF 6 BIT SUBTRACTOR

## I. Objective

The objective is to learn writing a Test Bench for a 6-bit subtractor. You will simulate your design using ModelSim and write a test bench for obtaining the simulation results.

## II. Instructions

- ❖Read section 2.19, Page Text Book for example on how to write Test Bench
- ❖Revise Class notes
- ❖Create a test bench for the 6-bit subtractor from lab 2
- ❖Provide 5 test samples to the subtractor and check the outputs

## III. Deliverables

**1.** Demonstration is **required**

**2. Pre- Lab**: No Pre-Lab is required.

**3. Report**:

a. Objective

b. Lab work:

- Implementation: describe your design
- Print and report the results including your codes

c. Conclusion: What went wrong? Why? , And how did you solve it?

## V. Grading

This lab has 15 points (8 demonstration, and 7 report).