ECE 4250/7250
VHDL AND PROGRAMMABLE LOGIC DEVICES

LAB#2
Sequential Process Design: BCD Counter

I. Objective

This objective of this lab is to make students familiar with the sequential process design by modeling a counter VHDL Process and verify the functionality of the model by using ModelSim.

II. Problems

Implement a 1 digit BCD (binary coded decimal) counter. It should be a synchronous (4-bit) up/down decade counter with output Q that works as follows: All state changes occur on the rising edge of the CLK input, except the asynchronous clear (CLR). When CLR = 0, the counter is reset regardless of the values of the other inputs. You can keep the time period of the CLK signal to 10ns for simulating your design.

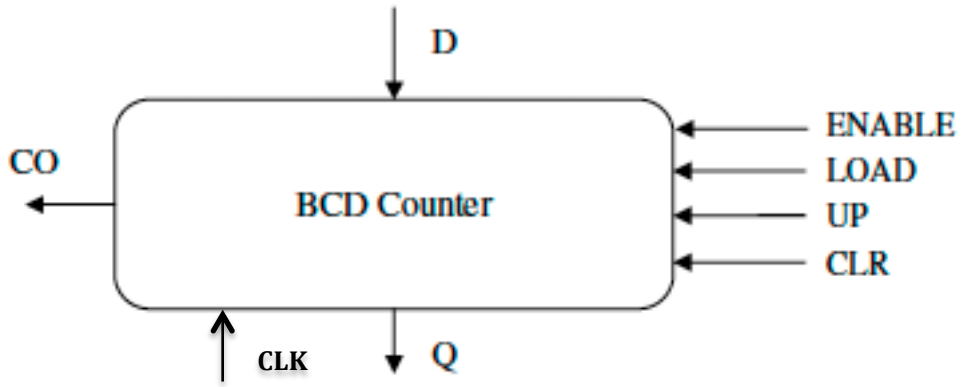

Figure1. Counter Block Diagram

A BCD counter has the range from 0-9. Shown below are the conditions for the counter. If the:

LOAD = ENABLE = 1, the data input D is loaded into the counter.
LOAD = 0 and ENABLE = UP = 1, the counter is incremented.
LOAD = 0, ENABLE = 1, and UP = 0, the counter is decremented.
ENABLE = 1 and UP = 1, the carry output (CO) = 1 only when the counter's previous value is 9.
ENABLE = 1 and UP = 0, the carry output (CO) = 1 only when the counter's previous value is 0.

Truth table for the counter:

Decimal count	A(3)	A(2)	A(1)	A(0)	Carry Out (CO)
0	0	0	0	0	0
1	0	0	0	1	0
2	0	0	1	0	0
3	0	0	1	1	0
4	0	1	0	0	0
5	0	1	0	1	0
6	0	1	1	0	0
7	0	1	1	1	0
8	1	0	0	0	0
9	1	0	0	1	0
0	**0**	**0**	**0**	**0**	**1**
1	0	0	0	1	0
2	0	0	1	0	0

III. VHDL Implementation

Part one: 0-9 BCD counter

Write a VHDL description of the counter. You may implement your design in any style you wish. It will be easier to use a behavioral description, which can be either written in the algorithmic way (eg. Count <= Count + 1)

You may also use dataflow or structural descriptions, although that will be more work. Use the following simulation for your waveforms:

1. Load counter with 6
2. Increment counter four times. You should get 9 and then 0.
3. Decrement counter once. You should get 9.
4. Clear the counter.

Part two: 00-99 BCD counter

Write a VHDL description of a decimal counter that uses two of the above counters to form a two-decade decimal up/down counter that counts up from 00 to 99 or down from 99 to 00. In other words, instantiate (port map) two single digit counters in a top module (the two-digit counter). You may need some extra logic in the top module too other than these instantiations.

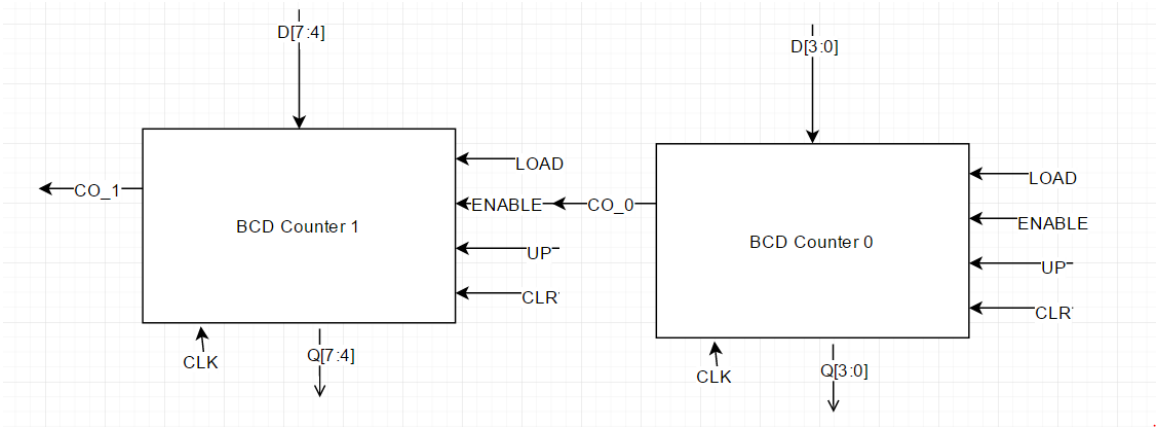

Figure 1. Two- Cascaded BCD Counter

The top module will have these inputs and outputs as shown above in the block diagram: CLR, CLK, ENABLE, LOAD, UP, D1, D2, Q1, D2, CO. Use the following simulation for your waveforms:

1. Load counter with 97
2. Increment counter five times.
3. Do nothing for 2 clock periods
3. Decrement counter four times.
4. Clear the counter.

IV. Questions:

1. In part a, step 2, what is the value of Co? Justify your answer?
2. If the counter current state is 0, and you have UP=0 (decrement)? How do you handle this case, explain?
3. In part b, when the counter current state is 00, and you have UP=0(decrement)? What is the expected output?

V. Deliverables

1. Demonstration is required

2. Pre- Lab: Read text book section 2.14

3. Report:

a. Objective

b. Lab work:

i. Print and comment the results. Take a close-up snapshot of the simulation and add it to the report. Snapshot for a one set of input values should suffice.

ii. Answer the question.

c. Conclusion: What went wrong? Why? And how did you solve it?

V. Grading

This lab is worth 20 points (See lab rules “Grading” section for details).