APPENDIX A

OUTPUT DIFFERENTIALS FOR EACH BYTE OBSERVED IN 1000 TESTS

Appendix A includes the number of times the respective output differentials $\delta_j = 1$ in 1000 tests for each state bit of any given byte of the moderate control model. The results from these tests are then used to formulate the conditions for identifying the target registers for each byte in the 1-byte moderate control model.

Table A.1: Number of Times $\delta_j = 1$, where $79 \leq j \leq 86$ for Each State Bits in S_{byte_0} in 1000 Tests

Target State Bit	Output Differential							
	δ_{79}	δ_{80}	δ_{81}	δ_{82}	δ_{83}	δ_{84}	δ_{85}	δ_{86}
s_0	1000	0	0	0	0	267	508	0
s_1	0	1000	0	0	0	0	218	479
s_2	0	0	1000	0	0	0	0	246
s_3	0	0	0	1000	0	0	0	0
s_4	0	0	0	0	1000	0	0	0
s_5	0	0	0	0	0	1000	0	0
s_6	0	0	0	0	0	0	1000	0
s_7	0	0	0	0	0	0	0	1000

Table A.2: Number of Times $\delta_j = 1$, where $87 \leq j \leq 94$ for Each State Bits in S_{byte_1} in 1000 Tests

Target State Bit	Output Differential							
	δ_{87}	δ_{88}	δ_{89}	δ_{90}	δ_{91}	δ_{92}	δ_{93}	δ_{94}
s_8	1000	0	0	0	0	247	496	0
s_9	0	1000	0	0	0	0	292	484
s_{10}	0	0	1000	0	0	0	0	259
s_{11}	0	0	0	1000	0	0	0	0
s_{12}	0	0	0	0	1000	0	0	0
s_{13}	0	0	0	0	0	1000	0	0
s_{14}	0	0	0	0	0	0	1000	0
s_{15}	0	0	0	0	0	0	0	1000

Table A.3: Number of Times $\delta_j = 1$, where $65 \leq j \leq 72$ for Each State Bits in S_{byte_2} in 1000 Tests

Target State Bit	Output Differential							
	δ_{65}	δ_{66}	δ_{67}	δ_{68}	δ_{69}	δ_{70}	δ_{71}	δ_{72}
s_{16}	1000	0	0	0	0	256	0	0
s_{17}	496	1000	0	0	0	0	240	0
s_{18}	0	529	1000	0	0	0	0	267
s_{19}	0	0	482	1000	0	0	0	0
s_{20}	0	0	0	500	1000	0	0	0
s_{21}	0	0	0	0	524	1000	0	0
s_{22}	0	0	0	0	0	501	1000	0
s_{23}	1000	0	0	0	0	0	511	1000

Table A.4: Number of Times $\delta_j = 1$, where $66 \leq j \leq 73$ for Each State Bits in S_{byte_3} in 1000 Tests

Target State Bit	Output Differential							
	δ_{66}	δ_{67}	δ_{68}	δ_{69}	δ_{70}	δ_{71}	δ_{72}	δ_{73}
s_{24}	1000	0	0	0	0	0	498	1000
s_{25}	0	1000	0	0	0	0	0	514
s_{26}	0	0	1000	0	0	0	0	0
s_{27}	0	0	0	1000	0	0	0	0
s_{28}	0	0	0	0	1000	0	0	0
s_{29}	0	0	0	0	0	1000	0	0
s_{30}	0	0	0	0	0	0	1000	0
s_{31}	0	0	0	0	0	0	0	1000

Table A.5: Number of Times $\delta_j = 1$, where $74 \leq j \leq 81$, for Each State Bits in S_{byte_4} in 1000 Tests

Target State Bit	Output Differential							
	δ_{74}	δ_{75}	δ_{76}	δ_{77}	δ_{78}	δ_{79}	δ_{80}	δ_{81}
s_{32}	1000	0	0	0	0	0	508	1000
s_{33}	0	1000	0	0	0	0	0	516
s_{34}	0	0	1000	0	0	0	0	0
s_{35}	0	0	0	1000	0	0	0	0
s_{36}	0	0	0	0	1000	0	0	0
s_{37}	0	0	0	0	0	1000	0	0
s_{38}	0	0	0	0	0	0	1000	0
s_{39}	0	0	0	0	0	0	0	1000

Table A.6: Number of Times $\delta_j = 1$, where $82 \leq j \leq 89$, for Each State Bits in S_{byte_5} in 1000 Tests

Target State Bit	Output Differential							
	δ_{82}	δ_{83}	δ_{84}	δ_{85}	δ_{86}	δ_{87}	δ_{88}	δ_{89}
s_{40}	1000	0	0	0	0	0	505	1000
s_{41}	0	1000	0	0	0	0	0	507
s_{42}	0	0	1000	0	0	0	0	0
s_{43}	0	0	0	1000	0	0	0	0
s_{44}	0	0	0	0	1000	0	0	0
s_{45}	0	0	0	0	0	1000	0	0
s_{46}	0	0	0	0	0	0	1000	0
s_{47}	0	0	267	508	0	0	0	1000

Table A.7: Number of Times $\delta_j = 1$, where $80 \leq j \leq 87$ and $90 \leq j \leq 91$, for Each State Bits in S_{byte_6} in 1000 Tests

Target State Bit	Output Differential									
	δ_{80}	δ_{81}	δ_{82}	δ_{83}	δ_{84}	δ_{85}	δ_{86}	δ_{87}	δ_{90}	δ_{91}
s_{48}	1000	0	0	0	0	218	479	0	1000	0
s_{49}	0	1000	0	0	0	0	246	503	0	1000
s_{50}	0	0	1000	0	0	0	0	251	0	0
s_{51}	0	0	0	1000	0	0	0	0	0	0
s_{52}	0	0	0	0	1000	0	0	0	490	0
s_{53}	0	0	0	0	0	1000	0	0	272	491
s_{54}	537	0	0	0	0	0	1000	0	0	251
s_{55}	0	514	0	0	0	0	0	1000	0	0

Table A.8: Number of Times $\delta_j = 1$, where $64 \leq j \leq 68$ and $88 \leq j \leq 90$, for Each State Bits in S_{byte_7} in 1000 Tests

Target State Bit	Output Differential							
	δ_{64}	δ_{65}	δ_{66}	δ_{67}	δ_{68}	δ_{88}	δ_{89}	δ_{90}
s_{56}	0	0	0	500	0	1000	0	0
s_{57}	251	0	0	0	494	0	1000	0
s_{58}	0	252	0	0	0	0	0	1000
s_{59}	1000	0	288	0	0	0	0	0
s_{60}	0	1000	0	239	0	0	0	0
s_{61}	0	0	1000	0	235	0	0	0
s_{62}	1000	0	0	1000	0	512	0	0
s_{63}	481	1000	0	0	1000	0	512	0

Table A.9: Number of Times $\delta_j = 1$, where $66 \leq j \leq 73$, for Each State Bits in S_{byte_8} in 1000 Tests

Target State Bit	Output Differential							
	δ_{66}	δ_{67}	δ_{68}	δ_{69}	δ_{70}	δ_{71}	δ_{72}	δ_{73}
s_{64}	1000	0	0	1000	0	240	0	0
s_{65}	529	1000	0	0	1000	0	267	0
s_{66}	0	482	1000	0	0	1000	0	250
s_{67}	0	0	500	1000	0	0	1000	0
s_{68}	0	0	0	524	1000	0	0	1000
s_{69}	0	0	0	0	501	1000	0	0
s_{70}	0	0	0	163	0	511	1000	0
s_{71}	1000	0	0	0	177	0	498	1000

Table A.10: Number of Times $\delta_j = 1$, where $67 \leq j \leq 74$, for Each State Bits in S_{byte_9} in 1000 Tests

Target State Bit	Output Differential							
	δ_{67}	δ_{68}	δ_{69}	δ_{70}	δ_{71}	δ_{72}	δ_{73}	δ_{74}
s_{72}	1000	0	0	0	208	0	514	1000
s_{73}	0	1000	0	0	0	194	0	515
s_{74}	253	0	1000	0	0	0	207	0
s_{75}	0	245	0	1000	0	0	0	163
s_{76}	0	0	261	0	1000	0	0	0
s_{77}	0	0	0	253	0	1000	0	0
s_{78}	0	0	0	0	232	0	1000	0
s_{79}	0	0	0	0	0	250	0	1000

Table A.11: Number of Times $\delta_j = 1$, where $75 \leq j \leq 82$, for Each State Bits in $S_{byte_{10}}$ in 1000 Tests

Target State Bit	Output Differential							
	δ_{75}	δ_{76}	δ_{77}	δ_{78}	δ_{79}	δ_{80}	δ_{81}	δ_{82}
s_{80}	1000	0	0	0	171	0	516	1000
s_{81}	0	1000	0	0	0	173	0	511
s_{82}	254	0	1000	0	0	0	184	0
s_{83}	0	251	0	1000	0	0	0	205
s_{84}	0	0	256	0	1000	0	0	0
s_{85}	0	0	0	246	505	1000	0	0
s_{86}	0	0	0	0	245	493	1000	0
s_{87}	0	0	0	0	0	256	506	1000

Table A.12: Number of Times $\delta_j = 1$, where $86 \leq j \leq 93$, for Each State Bits in $S_{byte_{11}}$ in 1000 Tests

Target State Bit	Output Differential							
	δ_{86}	δ_{87}	δ_{88}	δ_{89}	δ_{90}	δ_{91}	δ_{92}	δ_{93}
s_{88}	0	253	257	507	1000	0	0	1000
s_{89}	0	0	251	271	495	1000	0	0
s_{90}	0	0	0	266	242	510	1000	0
s_{91}	1000	0	0	0	274	428	491	1000
s_{92}	512	1000	0	0	0	266	429	520
s_{93}	370	513	1000	0	0	0	255	448
s_{94}	0	380	481	1000	0	0	0	265
s_{95}	0	0	376	487	1000	0	0	0

Table A.13: Number of Times $\delta_j = 1$, where $84 \leq j \leq 91$, for Each State Bits in $S_{byte_{12}}$ in 1000 Tests

Target State Bit	Output Differential							
	δ_{84}	δ_{85}	δ_{86}	δ_{87}	δ_{88}	δ_{89}	δ_{90}	δ_{91}
s_{96}	1000	0	0	0	0	360	474	1000
s_{97}	0	1000	0	0	0	0	390	488
s_{98}	0	0	1000	0	0	0	0	388
s_{99}	0	0	0	1000	0	0	0	0
s_{100}	246	0	0	0	1000	0	0	0
s_{101}	0	255	0	0	0	1000	0	0
s_{102}	0	0	254	0	0	0	1000	0
s_{103}	0	0	0	243	0	0	0	1000

Table A.14: Number of Times $\delta_j = 1$, where $72 \leq j \leq 79$ and $92 \leq j \leq 95$, for Each State Bits in $S_{byte_{13}}$ in 1000 Tests

Target State Bit	Output Differential											
	δ_{72}	δ_{73}	δ_{74}	δ_{75}	δ_{76}	δ_{77}	δ_{78}	δ_{79}	δ_{92}	δ_{93}	δ_{94}	δ_{95}
s_{104}	1000	126	0	0	491	0	0	0	1000	0	0	0
s_{105}	0	1000	129	0	0	484	0	0	0	1000	0	0
s_{106}	0	0	1000	134	0	0	496	0	0	0	1000	0
s_{107}	0	0	0	1000	106	0	0	484	0	0	0	1000
s_{108}	502	0	0	0	1000	115	0	0	230	0	0	0
s_{109}	382	519	0	0	0	1000	127	0	0	244	0	0
s_{110}	0	359	540	0	0	0	1000	120	0	0	245	0
s_{111}	0	0	346	535	0	0	0	1000	0	0	0	233

Table A.15: Number of Times $\delta_j = 1$, where $64 \leq j \leq 67, j = 69,\ j = 70,\ j = 80$ and $j = 85$, for Each State Bits in $S_{byte_{14}}$ in 1000 Tests

Target State Bit	Output Differential							
	δ_{64}	δ_{65}	δ_{66}	δ_{67}	δ_{69}	δ_{70}	δ_{80}	δ_{85}
s_{112}	0	0	0	0	517	0	1000	0
s_{113}	1000	0	0	0	260	525	0	515
s_{114}	0	1000	0	0	0	229	0	0
s_{115}	0	0	1000	0	0	0	0	0
s_{116}	0	0	0	1000	0	0	529	111
s_{117}	0	0	0	0	0	0	372	1000
s_{118}	0	0	0	0	1000	0	0	0
s_{119}	0	0	0	0	0	1000	0	0

Table A.16: Number of Times $\delta_j = 1$, where $71 \leq j \leq 78$, for Each State Bits in $S_{byte_{15}}$ in 1000 Tests

Target State Bit	Output Differential							
	δ_{71}	δ_{72}	δ_{73}	δ_{74}	δ_{75}	δ_{76}	δ_{77}	δ_{78}
s_{120}	1000	0	0	0	0	251	496	0
s_{121}	0	1000	0	0	0	0	234	487
s_{122}	0	0	1000	0	0	0	0	251
s_{123}	0	0	0	1000	0	0	0	0
s_{124}	0	0	0	0	1000	0	0	0
s_{125}	0	0	0	0	0	1000	0	0
s_{126}	0	0	0	0	0	0	1000	0
s_{127}	0	0	0	0	0	0	0	1000

APPENDIX B

LIST OF CONDITIONS OF EACH BYTE IN MODERATE CONTROL ON TINYJAMBUv2

Appendix B includes the conditions in each byte of TinyJAMBUv2 that have to be fulfilled in order to confirm the all the state bits have been affected with fault in the moderate control model.

Table B.1: Conditions that Have to be Fulfilled to Confirm that all the State Bits in S_{byte_0} are Affected with the Injected Faults

S_{byte_0}		
Target State Bit	Required Keystream and Condition	Remarks/Comments
s_0	$\delta_{79} = 1$	-
s_1	$\delta_{80} = 1$	-
s_2	$\delta_{81} = 1$	-
s_3	$\delta_{82} = 1$	-
s_4	$\delta_{83} = 1$	-
s_5	$\delta_{84} = 1$ and $\delta_{79} \neq 1$	If condition does not satisfy for target register 0 and [84] = 1
s_6	$\delta_{85} = 1$ and $\delta_{79} \neq 1$ and $\delta_{80} \neq 1$	If condition does not satisfy for target register 0,1 and [85] = 1
s_7	$\delta_{86} = 1$ and $\delta_{80} \neq 1$ and $\delta_{81} \neq 1$	If condition does not satisfy for target register 1,2 and [86] = 1

Table B.2: Conditions that Have to be Fulfilled to Confirm that all the State Bits in S_{byte_1} are Affected with the Injected Faults

S_{byte_1}		
Target State Bit	Required Keystream and Condition	Remarks/Comments
s_8	$\delta_{87} = 1$	-
s_9	$\delta_{88} = 1$	-
s_{10}	$\delta_{89} = 1$	-
s_{11}	$\delta_{90} = 1$	-
s_{12}	$\delta_{91} = 1$	-
s_{13}	$\delta_{92} = 1$ and $\delta_{87} \neq 1$	If condition does not satisfy for target register 8 and [92] = 1
s_{14}	$\delta_{93} = 1$ and $\delta_{87} \neq 1$ and $\delta_{88} \neq 1$	If condition does not satisfy for target register 8,9 and [93] = 1
s_{15}	($\delta_{94} = 1$ and $\delta_{88} \neq 1$ and $\delta_{89} \neq 1$)	If condition does not satisfy for target register 9,10 and [94] = 1 .

Table B.3: Conditions that Have to be Fulfilled to Confirm that all the State Bits in S_{byte_2} are Affected with the Injected Faults

S_{byte_2}		
Target State Bit	Required Keystream and Condition	Remarks/Comments
s_{16}	$\delta_{65}= 1$ and $\delta_{66} \neq 1$ and $\delta_{72} \neq 1$	-
s_{17}	$\delta_{66} = 1$ and $\delta_{67} \neq 1$	-
s_{18}	$\delta_{67} = 1$ and $\delta_{68} \neq 1$	-
s_{19}	$\delta_{68} = 1$ and $\delta_{69} \neq 1$	-
s_{20}	$\delta_{69} = 1$ and $\delta_{70} \neq 1$	-
s_{21}	$\delta_{70} = 1$ and $\delta_{65} \neq 1$ and $\delta_{71} \neq 1$	If condition does not satisfy for target register 16, 22 and [70] = 1
s_{22}	$\delta_{71} = 1$ and $\delta_{66} \neq 1$ and ($\delta_{65} \neq 1$ or $\delta_{72} \neq 1$)	If condition does not satisfy for target register 17, 23 and [71] = 1
s_{23}	$\delta_{65} = 1$ and $\delta_{72} = 1$	-

Table B.4: Conditions that Have to be Fulfilled to Confirm that all the State Bits in S_{byte_3} are Affected with the Injected Faults

S_{byte_3}		
Target State Bit	Required Keystream and Condition	Remarks/Comments
s_{24}	$\delta_{66} = 1$ or ($\delta_{66} = 1$ and $\delta_{73} = 1$)	-
s_{25}	$\delta_{67} = 1$	-
s_{26}	$\delta_{68} = 1$	-
s_{27}	$\delta_{69} = 1$	-
s_{28}	$\delta_{70} = 1$	-
s_{29}	$\delta_{71} = 1$	-
s_{30}	$\delta_{72} = 1$ and ($\delta_{66} \neq 1$ or $\delta_{73} \neq 1$)	If condition does not satisfy for target register 24 and [72] = 1
s_{31}	$\delta_{73} = 1$ and $\delta_{66} \neq 1$ and $\delta_{67} \neq 1$	If condition does not satisfy for target register 24, 25 and [73] = 1

Table B.5: Conditions that Have to be Fulfilled to Confirm that all the State Bits in S_{byte_4} are Affected with the Injected Faults

S_{byte_4}		
Target State Bit	Required Keystream and Condition	Remarks/Comments
s_{32}	$\delta_{74} = 1$ or ($\delta_{74} = 1$ and $\delta_{81} = 1$)	-
s_{33}	$\delta_{75} = 1$	-
s_{34}	$\delta_{76} = 1$	-
s_{35}	$\delta_{77} = 1$	-
s_{36}	$\delta_{78} = 1$	-
s_{37}	$\delta_{79} = 1$	-
s_{38}	$\delta_{80} = 1$ and ($\delta_{74} \neq 1$ or $\delta_{81} \neq 1$)	If condition does not satisfy for target register 32 and [80] = 1
s_{39}	$\delta_{81} = 1$ and $\delta_{74} \neq 1$ and $\delta_{75} \neq 1$	If condition does not satisfy for target register 32, 33 and [81] = 1

Table B.6: Conditions that Have to be Fulfilled to Confirm that all the State Bits in S_{byte_5} are Affected with the Injected Faults

S_{byte_5}		
Target State Bit	Required Keystream and Condition	Remarks/Comments
s_{40}	$\delta_{82} = 1$ or ($\delta_{82} = 1$ and $\delta_{89} = 1$)	-
s_{41}	$\delta_{83} = 1$	-
s_{42}	$\delta_{84} = 1$ and $\delta_{89} \neq 1$	If condition does not satisfy for target register 47 and [84] = 1
s_{43}	$\delta_{85} = 1$ and $\delta_{89} \neq 1$	If condition does not satisfy for target register 47 and [85] = 1
s_{44}	$\delta_{86} = 1$	-
s_{45}	$\delta_{87} = 1$	-
s_{46}	$\delta_{88} = 1$ and ($\delta_{82} \neq 1$ or $\delta_{89} \neq 1$)	If condition does not satisfy for target register 40 and [88] = 1
s_{47}	$\delta_{89} = 1$ and $\delta_{82} \neq 1$ and $\delta_{83} \neq 1$	If condition does not satisfy for target register 40, 41 and [89] = 1

Table B.7: Conditions that Have to be Fulfilled to Confirm that all the State Bits in S_{byte_6} are Affected with the Injected Faults

S_{byte_6}		
Target State Bit	Required Keystream and Condition	Remarks/Comments
s_{48}	$\delta_{80} = 1$ and $\delta_{90} = 1$	-
s_{49}	$\delta_{81} = 1$ and $\delta_{91} = 1$	-
s_{50}	$\delta_{82} = 1$	-
s_{51}	$\delta_{83} = 1$	-
s_{52}	$\delta_{84} = 1$	-
s_{53}	$\delta_{85} = 1$ and $\delta_{80} \neq 1$	If condition does not satisfy for target register 48 and [85] = 1
s_{54}	$\delta_{86} = 1$ and $\delta_{81} \neq 1$ and $\delta_{90} \neq 1$	If condition does not satisfy for target register 48, 49 and [86] = 1
s_{55}	$\delta_{87} = 1$ and $\delta_{82} \neq 1$ and $\delta_{91} \neq 1$	If condition does not satisfy for target register 49, 50 and [87] = 1

Table B.8: Conditions that Have to be Fulfilled to Confirm that all the State Bits in S_{byte_7} are Affected with the Injected Faults

S_{byte_7}		
Target State Bit	Required Keystream and Condition	Remarks/Comments
s_{56}	$\delta_{88} = 1$ and $\delta_{64} \neq 1$	If condition does not satisfy for target register 62 and [88] = 1
s_{57}	$\delta_{89} = 1$ and $\delta_{65} \neq 1$	If condition does not satisfy for target register 63 and [89] = 1
s_{58}	$\delta_{90} = 1$	-
s_{59}	$(\delta_{64} = 1$ and $\delta_{67} \neq 1$ and $\delta_{68} \neq 1$ and $\delta_{89} \neq 1)$	If condition does not satisfy for target register 57, 62, 63 and [64] = 1
s_{60}	$(\delta_{65} = 1$ and $\delta_{68} \neq$ and $1\ \delta_{90} \neq 1\ )$	If condition does not satisfy for target register 58, 63 and [65] = 1
s_{61}	$(\delta_{66} = 1$ and $\delta_{64} \neq 1)$	If condition does not satisfy for target register 59 and [66] = 1
s_{62}	$(\delta_{64} = 1$ and $\delta_{67} = 1)$	-
s_{63}	$(\delta_{65} = 1$ and $\delta_{68} = 1)$	-

Table B.9: Conditions that Have to be Fulfilled to Confirm that all the State Bits in S_{byte_8} are Affected with the Injected Faults

S_{byte_8}		
Target State Bit	Required Keystream and Condition	Remarks/Comments
s_{64}	$\delta_{66} = 1$ and $\delta_{69} = 1$	-
s_{65}	$\delta_{67} = 1$ and $\delta_{70} = 1$	
s_{66}	$\delta_{68} = 1$ and $\delta_{71} = 1$	-
s_{67}	$(\delta_{69} = 1$ and $\delta_{72} = 1)$ and $\delta_{65} \neq 1$	If condition does not satisfy for target register 70 and [69, 72] = 1
s_{68}	$(\delta_{70} = 1$ and $\delta_{66} \neq 1$ and $\delta_{67} \neq 1$ and $\delta_{71} \neq 1)$	If condition does not satisfy for target register 64, 65, 69 and [70] = 1
s_{69}	$\delta_{71} = 1$ and $(\delta_{65} \neq 1$ or $\delta_{72} \neq 1)$ and $\delta_{68} \neq 1$ and $\delta_{69} \neq 1$	If condition does not satisfy for target register 64, 66, 70 and [71] = 1
s_{70}	$(\delta_{65} = 1$ and $\delta_{72} = 1)$	-
s_{71}	$(\delta_{66} = 1$ and $\delta_{73} = 1)$	-

Table B.10: Conditions that Have to be Fulfilled to Confirm that all the State Bits in S_{byte_9} are Affected with the Injected Faults

S_{byte_9}		
Target State Bit	Required Keystream and Condition	Remarks/Comments
s_{72}	$(\delta_{67} = 1 \text{ and } \delta_{74} = 1)$	-
s_{73}	$(\delta_{68} = 1 \text{ and } \delta_{70} \neq 1)$	If condition does not satisfy for target register 75 and [68] = 1
s_{74}	$(\delta_{69} = 1 \text{ and } \delta_{71} \neq 1)$	If condition does not satisfy for target register 76 and [69] = 1
s_{75}	$(\delta_{70} = 1 \text{ and } \delta_{72} \neq 1)$	If condition does not satisfy for target register 77 and [70] = 1
s_{76}	$(\delta_{71} = 1 \text{ and } \delta_{67} \neq 1 \text{ and } \delta_{73} \neq 1)$	If condition does not satisfy for target register 72, 78 and [71] = 1
s_{77}	$(\delta_{72} = 1 \text{ and } \delta_{68} \neq 1 \text{ and } \delta_{74} \neq 1)$	If condition does not satisfy for target register 73, 79 and [72] = 1
s_{78}	$\delta_{73} = 1 \text{ and } \delta_{67} \neq 1 \text{ and } \delta_{69} \neq 1$	If condition does not satisfy for target register 72, 74 and [73] = 1
s_{79}	$(\delta_{74} = 1 \text{ and } \delta_{67} \neq 1 \text{ and } \delta_{68} \neq 1 \text{ and } \delta_{70} \neq 1)$	If condition does not satisfy for target register 72, 73, 75 and [74] = 1

Table B.11: Conditions that Have to be Fulfilled to Confirm that all the State Bits in $S_{byte_{10}}$ are Affected with the Injected Faults

$S_{byte_{10}}$		
Target State Bit	Required Keystream and Condition	Remarks/Comments
s_{80}	$(\delta_{75} = 1 \text{ and } \delta_{82} = 1)$	-
s_{81}	$(\delta_{76} = 1 \text{ and } \delta_{78} \neq 1)$	If condition does not satisfy for target register 83 and [76] = 1
s_{82}	$(\delta_{77} = 1 \text{ and } \delta_{79} \neq 1)$	If condition does not satisfy for target register 84 and [77] = 1
s_{83}	$(\delta_{78} = 1 \text{ and } \delta_{80} \neq 1)$	If condition does not satisfy for target register 85 and [78] = 1
s_{84}	$\delta_{79} = 1$ and $(\delta_{75} \neq 1$ or $\delta_{82} \neq 1)$ and $\delta_{80} \neq 1$ and $\delta_{81} \neq 1$	If condition does not satisfy for target register 80, 85, 86 and [79] = 1
s_{85}	$(\delta_{80} = 1 \text{ and } \delta_{76} \neq 1 \text{ and } \delta_{81} \neq 1 \text{ and } \delta_{82} \neq 1)$	If condition does not satisfy for target register 81, 86, 87 and [80] = 1
s_{86}	$\delta_{81} = 1$ and $(\delta_{75} \neq 1$ or $\delta_{82} \neq 1)$ and $\delta_{77} \neq 1$ and $\delta_{82} \neq 1$	If condition does not satisfy for target register 80, 82, 87 and [81] = 1
s_{87}	$(\delta_{82} = 1 \text{ and } \delta_{75} \neq 1 \text{ and } \delta_{76} \neq 1 \text{ and } \delta_{78} \neq 1)$	If condition does not satisfy for target register 80, 81, 83 and [82] = 1

Table B.12: Conditions that Have to be Fulfilled to Confirm that all the State Bits in $S_{byte_{11}}$ are Affected with the Injected Faults

$S_{byte_{11}}$		
Target State Bit	Required Keystream and Condition	Remarks/Comments
s_{88}	$(\delta_{90} = 1 \text{ and } \delta_{93} = 1 \text{ and } \delta_{86} \neq 1)$	If condition does not satisfy for target register 91 and [90, 93] = 1
s_{89}	$\delta_{91} = 1 \text{ and } (\delta_{86} \neq 1 \text{ or } \delta_{93} \neq 1) \text{ and } \delta_{87} \neq 1 \text{ and } \delta_{92} \neq 1$	If condition does not satisfy for target register 90, 91, 92 and [91] = 1
s_{90}	$\delta_{92} = 1 \text{ and } (\delta_{86} \neq 1 \text{ or } \delta_{93} \neq 1) \text{ and } \delta_{87} \neq 1 \text{ and } \delta_{88} \neq 1$	If condition does not satisfy for target register 91, 92, 93 and [91] = 1
s_{91}	$\delta_{86} = 1 \text{ and } \delta_{93} = 1 \text{ and } \delta_{87} \neq 1 \text{ and } \delta_{88} \neq 1$	If condition does not satisfy for target register 92, 93 and [86, 93] = 1
s_{92}	$\delta_{87} = 1 \text{ and } \delta_{88} \neq 1 \text{ and } \delta_{89} \neq 1 \text{ and } \delta_{90} \neq 1$	If condition does not satisfy for target register 88, 93, 94 and [87] = 1
s_{93}	$\delta_{88} = 1 \text{ and } \delta_{89} \neq 1 \text{ and } \delta_{90} \neq 1 \text{ and } \delta_{91} \neq 1$	If condition does not satisfy for target register 89, 94, 95 and [88] = 1
s_{94}	$(\delta_{89} = 1 \text{ and } \delta_{90} \neq 1 \text{ and } \delta_{91} \neq 1 \text{ and } \delta_{92} \neq 1)$	If condition does not satisfy for target register 88, 89, 90, 95 and [88] = 1
s_{95}	$(\delta_{90} = 1 \text{ and } \delta_{91} \neq 1 \text{ and } \delta_{92} \neq 1 \text{ and } \delta_{93} \neq 1)$	If condition does not satisfy for target register 88, 89, 90, 91 and [82] = 1

Table B.13: Conditions that Have to be Fulfilled to Confirm that all the State Bits in $S_{byte_{12}}$ are Affected with the Injected Faults

$S_{byte_{12}}$		
Target State Bit	Required Keystream and Condition	Remarks/Comments
s_{96}	$\delta_{84} = 1$ and $\delta_{91} = 1$	-
s_{97}	$\delta_{85} = 1$ and $\delta_{89} \neq 1$	If condition does not satisfy for target register 101 and [85] = 1
s_{98}	$\delta_{86} = 1$ and $\delta_{90} \neq 1$	If condition does not satisfy for target register 102 and [86] = 1
s_{99}	$\delta_{87} = 1$ and $\delta_{91} \neq 1$	If condition does not satisfy for target register 103 and [87] = 1
s_{100}	$\delta_{88} = 1$	-
s_{101}	$\delta_{89} = 1$ and ($\delta_{84} \neq 1$ or $\delta_{91} \neq 1$)	If condition does not satisfy for target register 96 and [89] = 1
s_{102}	$\delta_{90} = 1$ and ($\delta_{84} \neq 1$ or $\delta_{91} \neq 1$) and $\delta_{85} \neq 1$	If condition does not satisfy for target register 96, 97 and [90] = 1
s_{103}	$\delta_{91} = 1$ and $\delta_{84} \neq 1$ and $\delta_{85} \neq 1$ and $\delta_{86} \neq 1$	If condition does not satisfy for target register 96, 97, 98 and [91] = 1

Table B.14: Conditions that Have to be Fulfilled to Confirm that all the State Bits in $S_{byte_{13}}$ are Affected with the Injected Faults

$S_{byte_{13}}$		
Target State Bit	Required Keystream and Condition	Remarks/Comments
s_{104}	$\delta_{72} = 1$ and $\delta_{92} = 1$ and $\delta_{76} \neq 1$	Cannot be determined (Condition coincides with target register 108
s_{105}	$\delta_{73} = 1$ and $\delta_{93} = 1$ and $\delta_{77} \neq 1$	Condition coincides with target register 109
s_{106}	$\delta_{74} = 1$ and $\delta_{94} = 1$ and $\delta_{78} \neq 1$	Condition coincides with target register 110
s_{107}	$\delta_{75} = 1$ and $\delta_{95} = 1$ and $\delta_{79} \neq 1$	Condition coincides with target register 111
s_{108}	$\delta_{76} = 1$ and $\delta_{75} \neq 1$ and ($\delta_{72} \neq 1$ or $\delta_{92} \neq 1$)	Condition coincides with target register 104
s_{109}	$\delta_{77} = 1$ and $\delta_{76} \neq 1$ and ($\delta_{73} \neq 1$ or $\delta_{93} \neq 1$)	Condition coincides with target register 105
s_{110}	$\delta_{78} = 1$ and $\delta_{77} \neq 1$ and ($\delta_{74} \neq 1$ or $\delta_{94} \neq 1$)	Condition coincides with target register 106
s_{111}	$\delta_{79} = 1$ and $\delta_{78} \neq 1$ and ($\delta_{75} \neq 1$ or $\delta_{95} \neq 1$)	Condition coincides with target register 107

Table B.15: Conditions that Have to be Fulfilled to Confirm that all the State Bits in $S_{byte_{14}}$ are Affected with the Injected Faults

$S_{byte_{14}}$		
Target State Bit	Required Keystream and Condition	Remarks/Comments
s_{112}	$\delta_{80} = 1$ and $\delta_{67} \neq 1$ and $\delta_{85} \neq 1$	If condition does not satisfy for target register 116, 117 and [79] = 1
s_{113}	$\delta_{64} = 1$	-
s_{114}	$\delta_{65} = 1$	-
s_{115}	$\delta_{66} = 1$	-
s_{116}	$\delta_{67} = 1$	-
s_{117}	$\delta_{85} = 1$ and $\delta_{64} \neq 1$ and $\delta_{67} \neq 1$	If condition does not satisfy for target register 113, 116 and [85] = 1
s_{118}	$\delta_{69} = 1$ and $\delta_{64} \neq 1$ and $\delta_{80} \neq 1$	If condition does not satisfy for target register 112, 113 and [69] = 1
s_{119}	$\delta_{70} = 1$ and $\delta_{64} \neq 1$ and $\delta_{65} \neq 1$	If condition does not satisfy for target register 113, 114 and [70] = 1

Table B.16: Conditions that Have to be Fulfilled to Confirm that all the State Bits in $S_{byte_{15}}$ are Affected with the Injected Faults

$S_{byte_{15}}$		
Target State Bit	Required Keystream and Condition	Remarks/Comments
s_{120}	$\delta_{71} = 1$	-
s_{121}	$\delta_{72} = 1$	-
s_{122}	$\delta_{73} = 1$	-
s_{123}	$\delta_{74} = 1$	-
s_{124}	$\delta_{75} = 1$	-
s_{125}	$\delta_{76} = 1$ and $\delta_{71} \neq 1$	If condition does not satisfy for target register 120 and [76] = 1
s_{126}	$\delta_{77} = 1$ and $\delta_{71} \neq 1$ and $\delta_{72} \neq 1$	If condition does not satisfy for target register 120, 121 and [77] = 1
s_{127}	$\delta_{78} = 1$ and $\delta_{72} \neq 1$ and $\delta_{73} \neq 1$	If condition does not satisfy for target register 121, 122 and [78] = 1