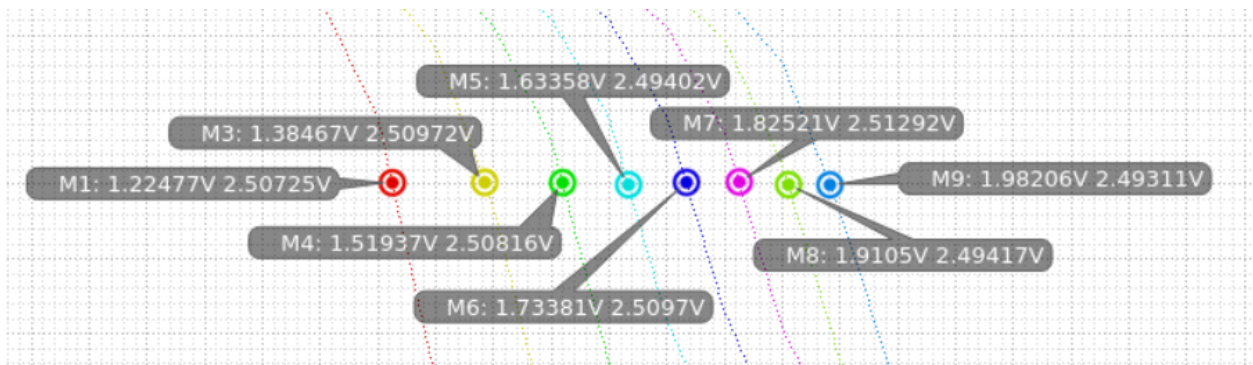
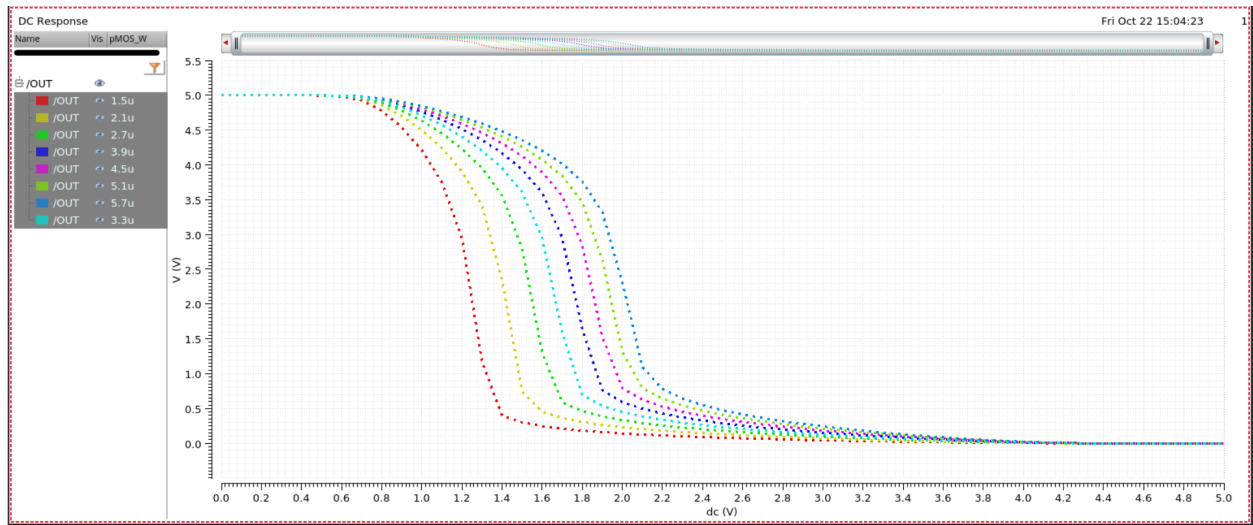


Sam Sylvester
ECE 4130 - Intro to VLSI
Design 1

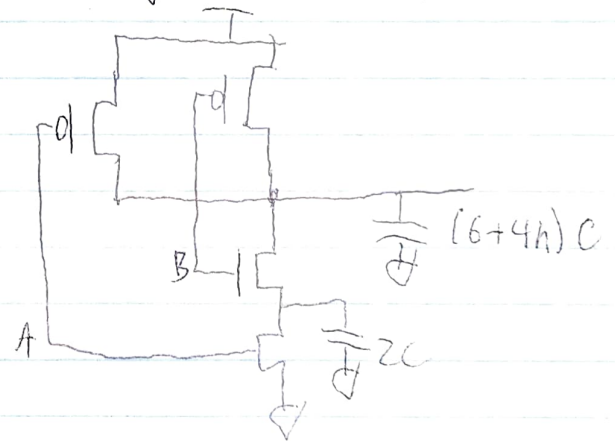
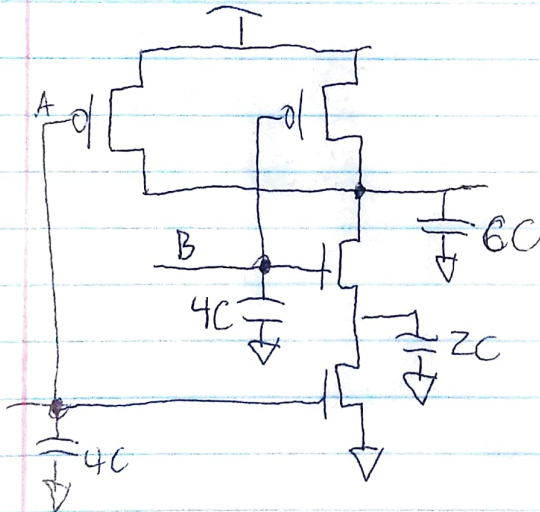
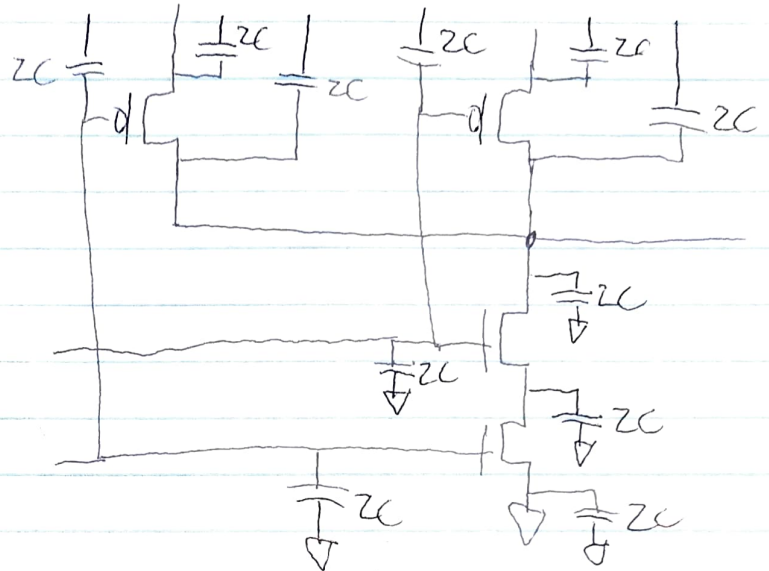
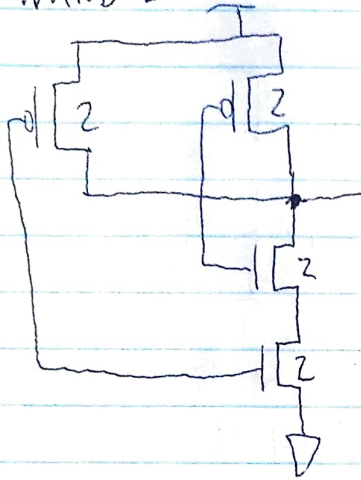


The curves to the right have a higher B_p/B_n ratio than the curves to the left. This feels intuitive because as the width of the pMOS increases, the Beta ratio also increases.

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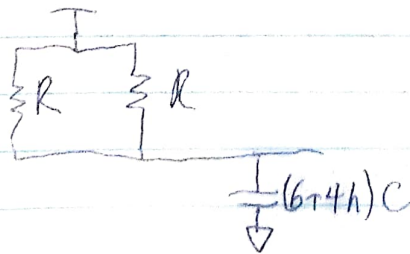
VLSI Design I

NAND 2



Case AB

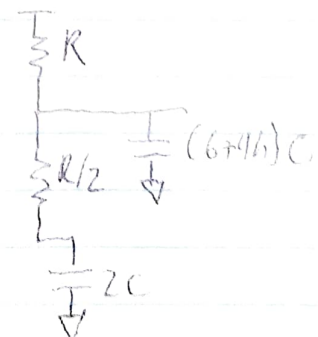
Case 00



$$t = \frac{1}{2} (6+4h) RC$$

$$= (3+2h) RC$$

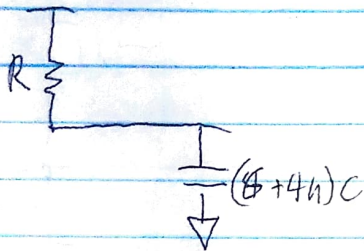
Case 01



$$t = R (6+4h) C + R 2C$$

$$= (8+4h) RC$$

Case 10



$$t = (6+4h)RC$$

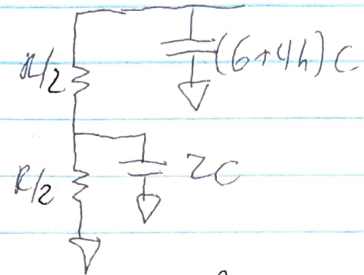
$$t_{pdr} = (8+4h)RC$$

$$t_{pdf} = (7+4h)RC$$

$$t_{cdr} = (3+2h)RC$$

$$t_{cdf} = (7+4h)RC$$

Case 11



$$t = R(6+4h)C + \frac{R}{2}(2C)$$

$$= (7+4h)RC$$

Using $h=0$, $R=10\text{LSI} \cdot \mu\text{m}$, $C=2\text{fF}/\mu\text{m}$

$$3RC = 60\text{ps}$$

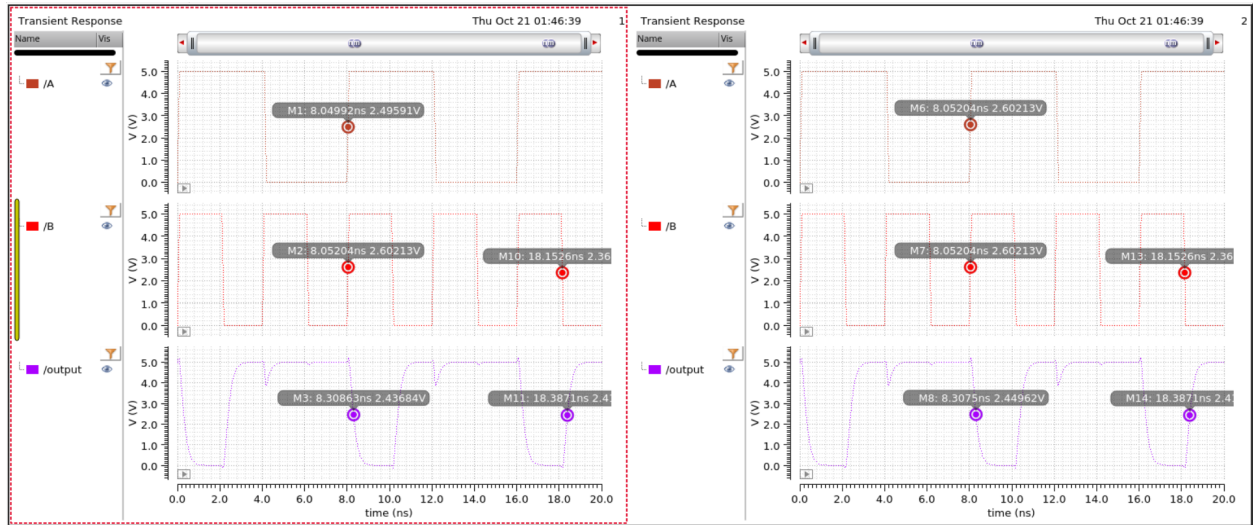
$$RC = 20\text{ps}$$

$$t_{pdr} = 160\text{ps}$$

$$t_{pdf} = 140\text{ps}$$

$$t_{cdr} = 60\text{ps}$$

$$t_{cdf} = 140\text{ps}$$

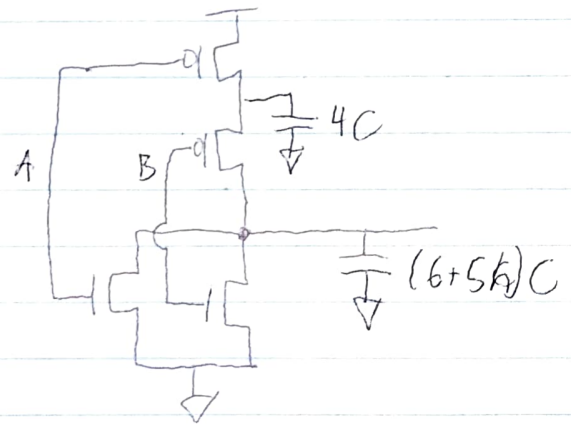
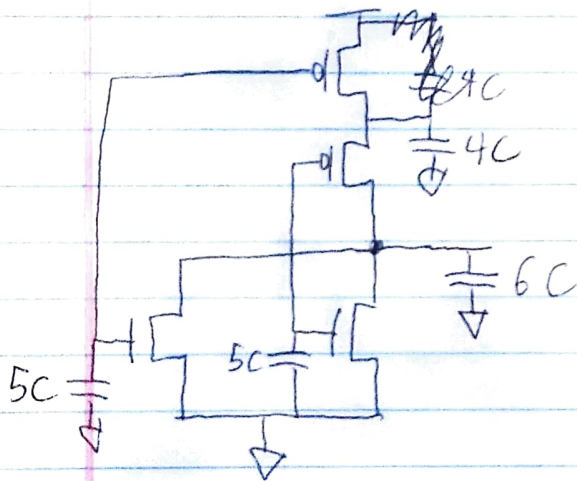
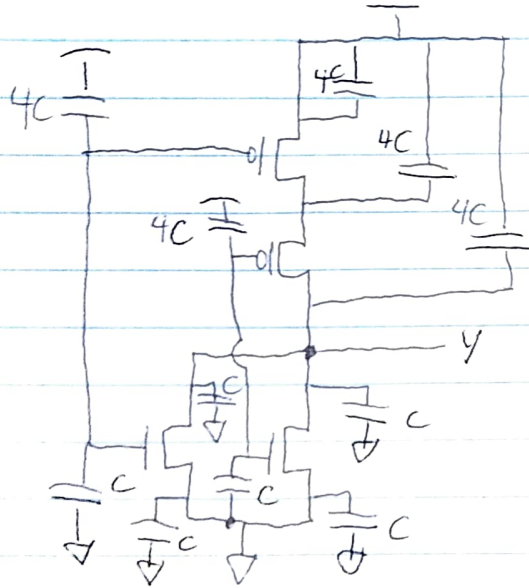
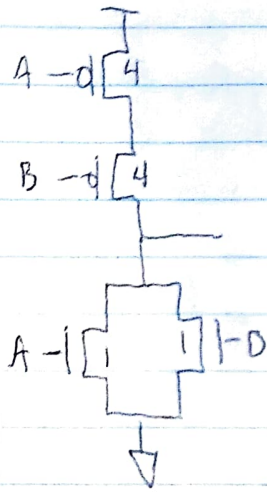


$$t_{\text{fall}} = 255.46 \text{ ps}$$

$$t_{\text{rise}} = 234.5 \text{ ps}$$

These results do not match up with the by paper results very well, but they do match up enough.

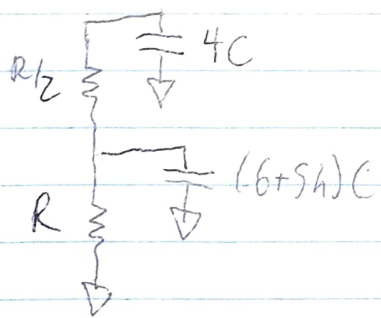
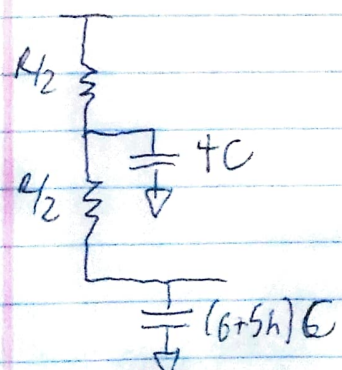
NOR 2



Case AB

Case 00

Case 01



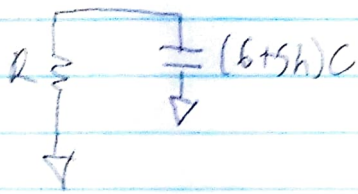
$$t = \frac{R}{2} (6+5h)C + \frac{R}{2} (4C)$$

$$= (5 + \frac{5}{2}h)C$$

$$t = \frac{3R}{2} (4C) + (6+5h)RC$$

$$= (12+5h)RC$$

Case 10



$$t = (6+5h)RC$$

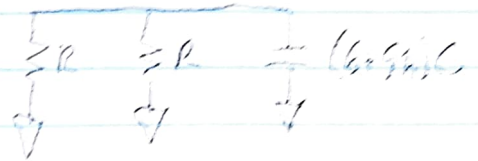
$$t_{pdr} = (5 + \frac{5}{2}h)RC$$

$$t_{pdf} = (12 + 5h)RC$$

$$t_{cdr} = (5 + \frac{5}{2}h)RC$$

$$t_{cdf} = (3 + \frac{5}{2}h)RC$$

Case 11



$$t = (6+5h)C \cdot \frac{R}{2}$$

$$= (3 + \frac{5}{2}h)RC$$

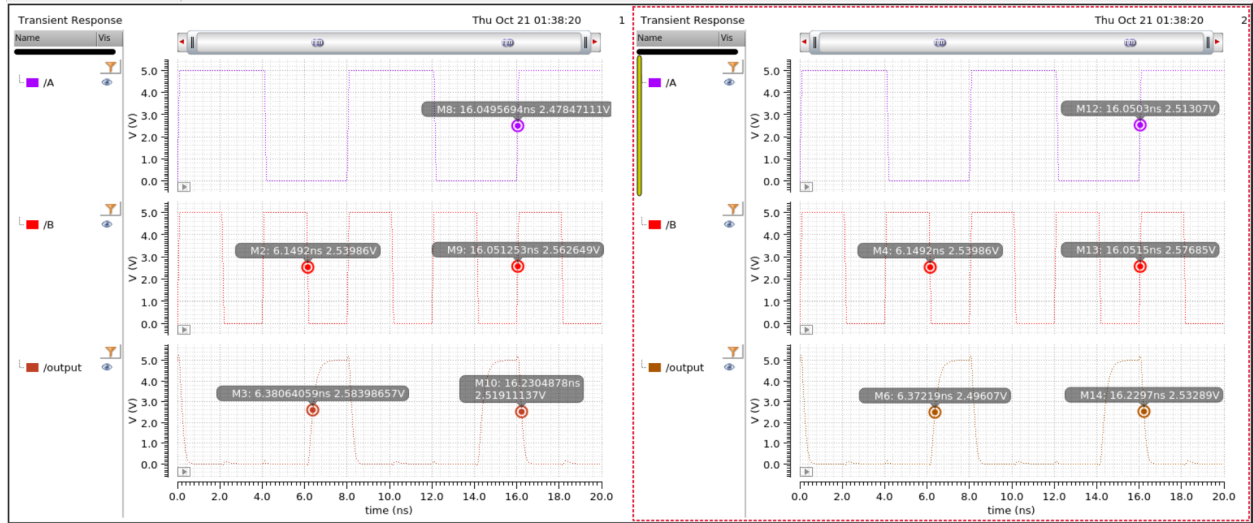
Using $h=0$, $3RC = 60ps \Rightarrow RC = 20ps$

$$t_{pdr} = 100ps$$

$$t_{pdf} = 70ps$$

$$t_{cdr} = 100ps$$

$$t_{cdf} = 50ps$$



$$t_{\text{fall}} = 179.25 \text{ ps}$$

$$t_{\text{rise}} = 231.44 \text{ ps}$$

Again, these values don't match very well to the paper results, however they are close enough for the fact that the paper results are a first degree estimation.

	NAND	NOR
t_{pdr} (paper)	160 ps	100 ps
t_{pdf} (paper)	140 ps	240 ps
t_{cdr} (paper)	60 ps	100 ps
t_{cdf} (paper)	140 ps	60 ps
t_{fall} (sim)	255 ps	179 ps
t_{rise} (sim)	234 ps	231 ps

My results from paper analysis show much lower delay values than my simulation results, but that is due to the simulation results being more accurate and accounting for more capacitances than is reasonable to do by hand.