Samuel Sylvester

Other Team Members- William Scarlett and Jonathan Sanderson

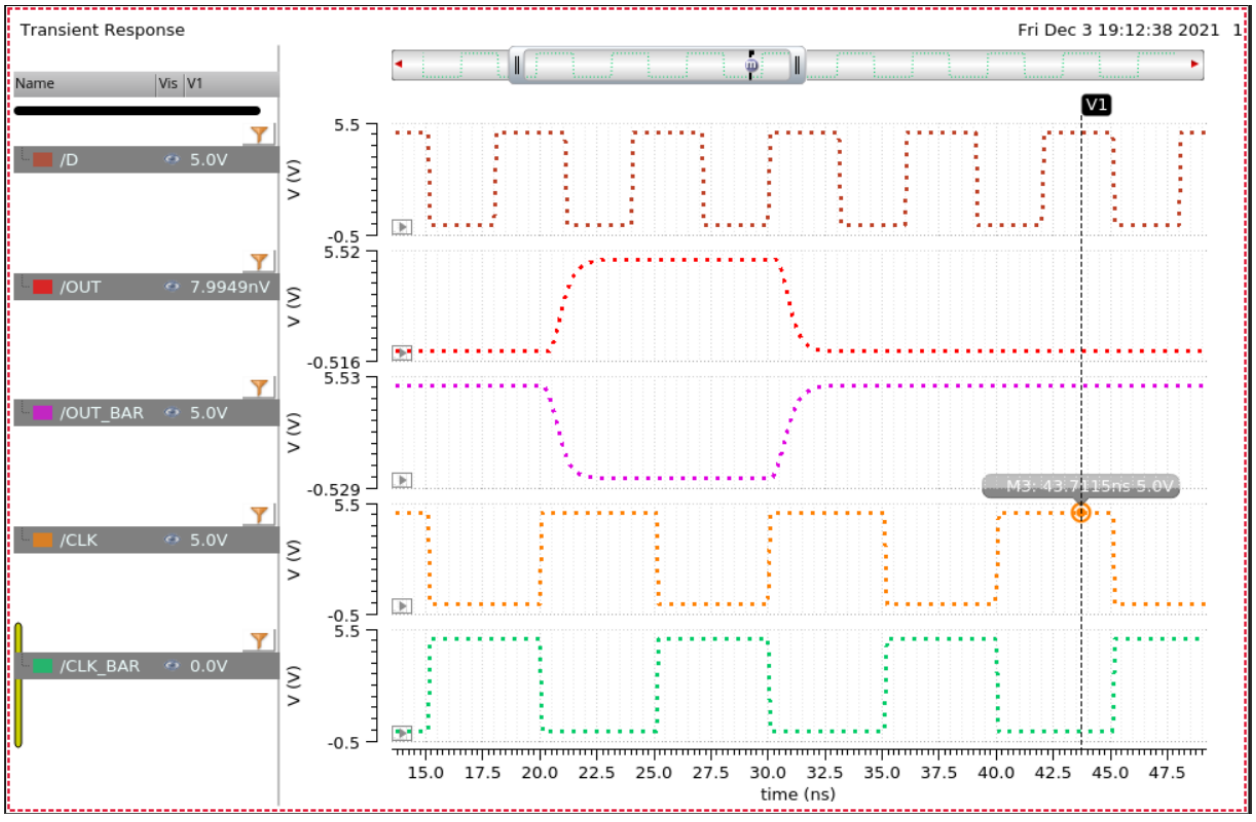
Design Assignment 3

Individual Submission

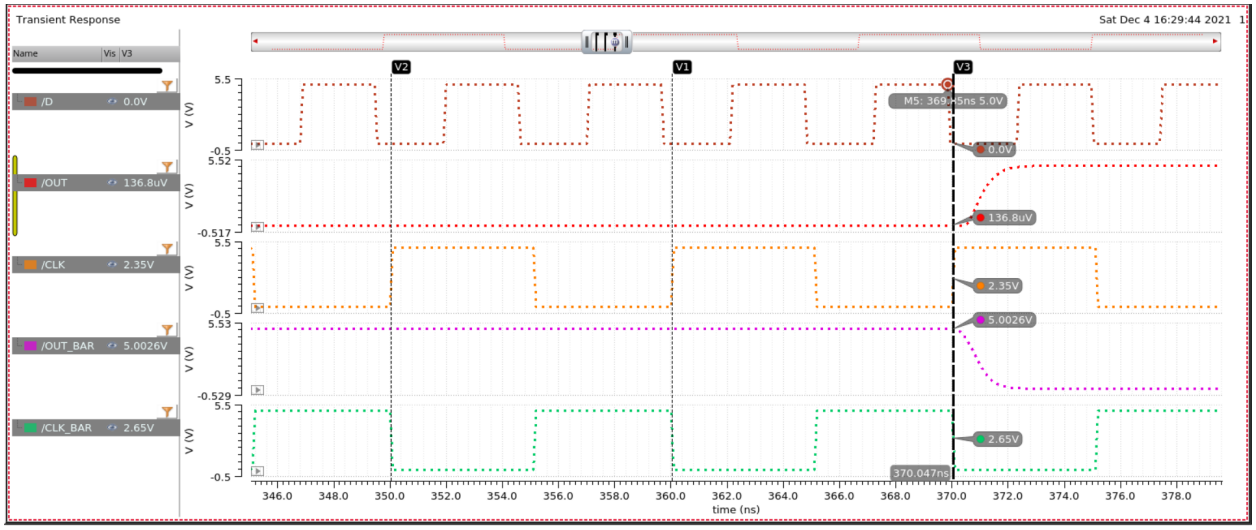
1. Technical Contributions

For this assignment, I worked on getting the timings for the D Flip Flip, as well as doing the on paper design for the XOR gate to be used in the adder. Will took my paper design, and adjusted it while making the XOR gate in Cadence.

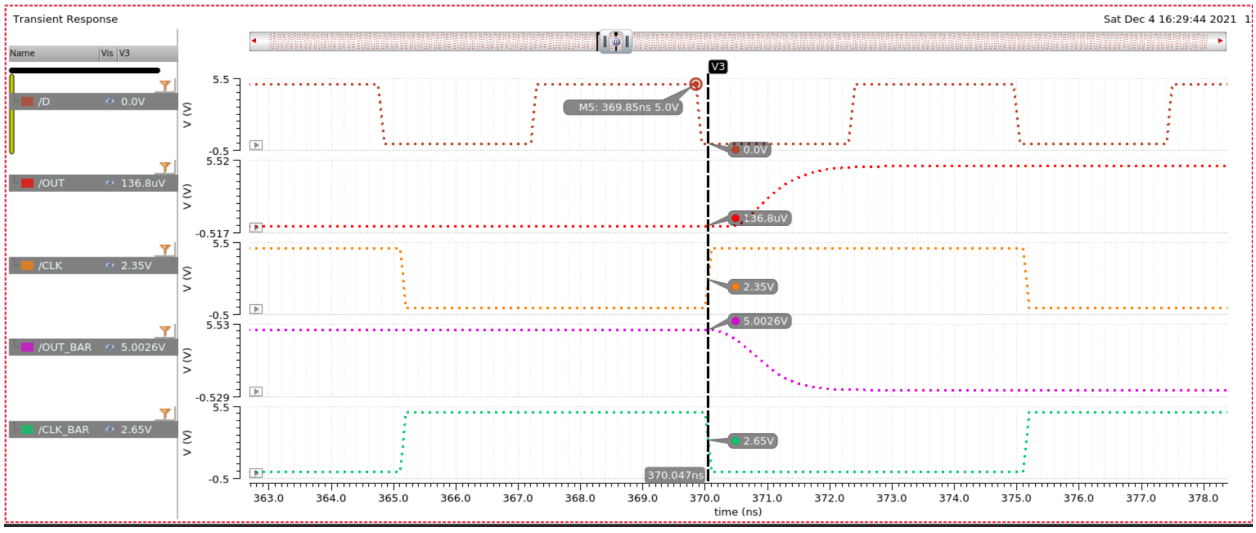
2. Evidence of Work Contributed



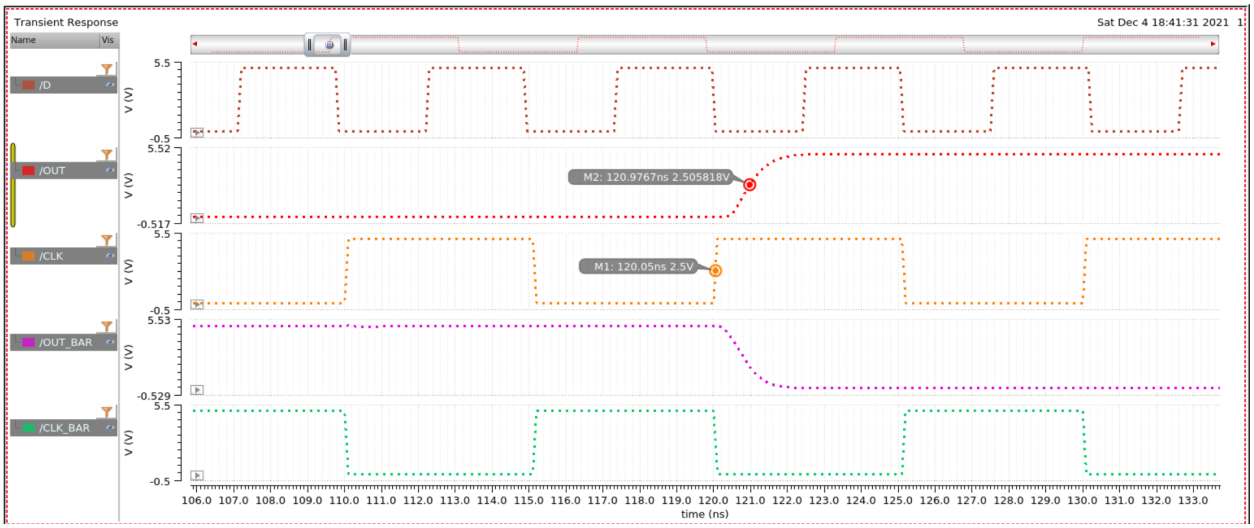
Test of given D Flip Flop



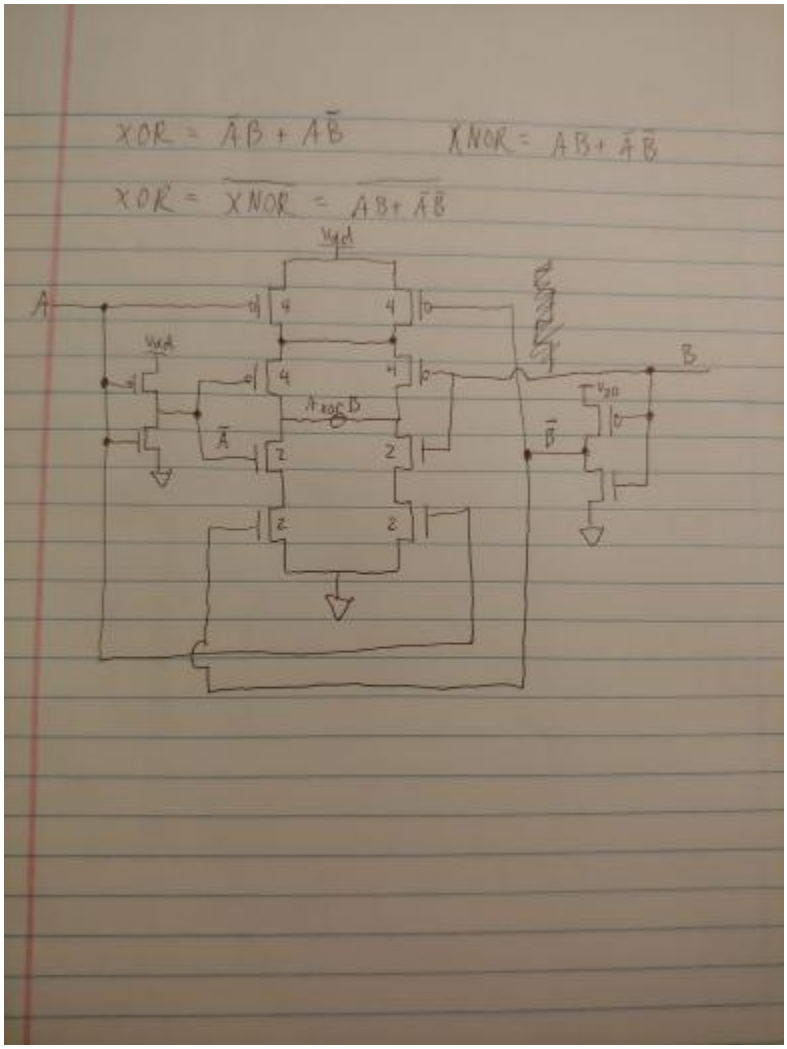
Plot Points to get t_{setup}



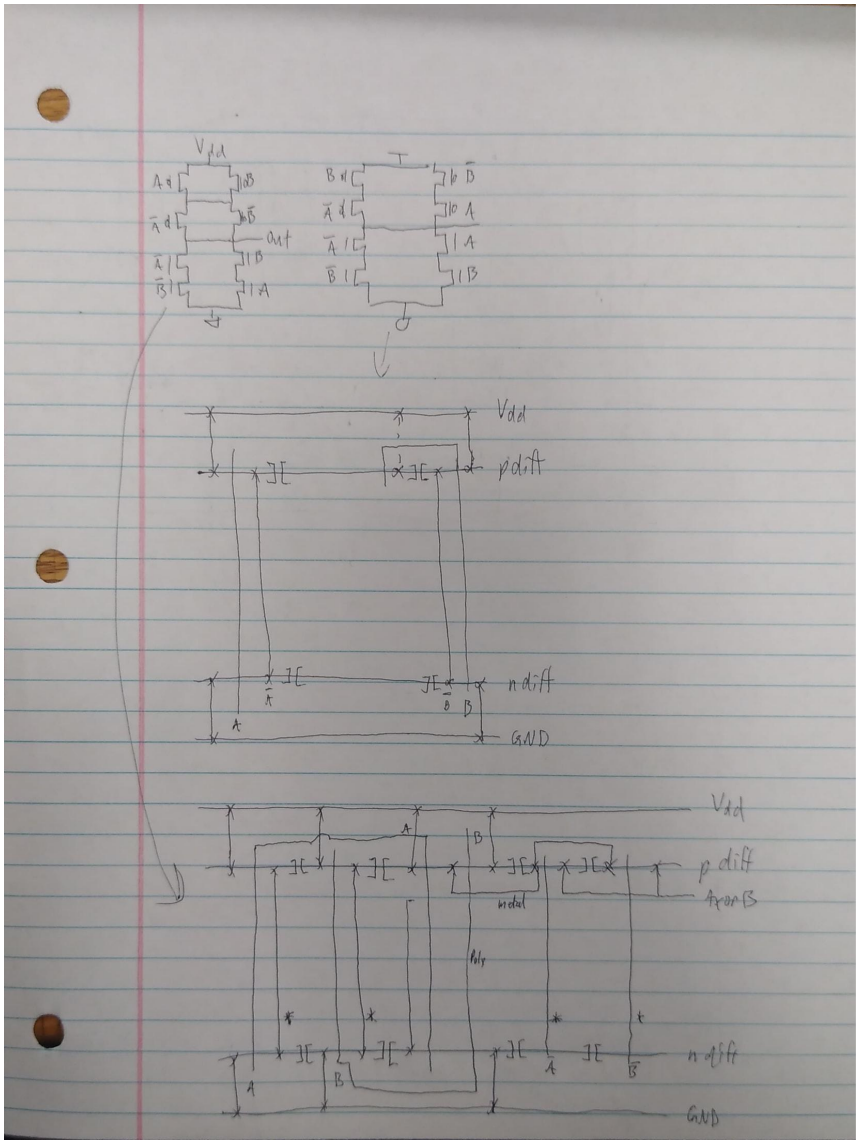
Closer look at the specific data point used to get t_{setup}



Plot showing t_{pcq}



XOR Schematic



XOR Layout Draft

Cadence files are also included in the DFF-MS folder contained in the same folder as this file. Read README.txt to properly use the Simulation files.

3. Work Distribution and Rationale

For this project, we split up the work fairly evenly between us, based on when we had time to work on it. I worked on the first sections, timing on the D flip flop and designing the XOR gate for the adder system. I took these parts because it is closer to the first third of the work, and I had time up front to work on this project. This work is important to this project because the timings of the D flip flop allow for us to make the most time efficient design for the overall system, and the XOR gate is required to make the full adder system.

Will took designing the full adder in CMOS logic as well as designing the full adder using transmission gates. The CMOS logic full adder also included taking the XOR gate that I designed on paper and creating the computer simulation of it, and adjusting the layout design as needed. Will took these parts because he had time throughout the assignment period to make sure that this is working properly. His part is important to this project because the end goal is to make a fully functional full adder that is as time efficient as possible. The full adder design is key to making the whole system efficient, and attempting to do this design in multiple design styles allows for more testing to get the highest speed we can.

Jonathan took working on putting the whole system of Flip Flops and the full adder together as well as optimizing the design. Jonathan also put together the team report, with input from me and Will. He took this part because he had a few assignments due in the early part of this assignment's work period, but knew he would have more time towards the end to put into it. So he took the part that required my and Will's work to be complete. The optimization process is very important to any system because time efficiency is a key element of design for any ASIC engineer, and making things run faster allows us to increase the clock speed of the whole system, which is a benefit for high performance machines.