EE6094
CAD for VLSI Design
Programming Assignment 5 Report

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一、題目描述

利用工作站練習操作 EDA Tools，並回答投影片中的問題。

二、實現過程

照著附件 ppt 的步驟在工作站上執行 Design Compiler、IC compiler(Design Setup、Design Planning、Placement、CTS、Route)等步驟。

Design Compiler：

把寫好的.v 檔讀進來，並且設定 clk，轉換出合法的 Verilog Netlist，並生成 SDF(Standard Delay Format)檔案跟 SDC(Synopsys Design Contraints)檔案。

☆SDF：紀錄每個 cell 跟 net 的 delay time[1]

☆SDC：包含 clk waveform、input/output delay 與 output load 等[2]

IC compiler-Design Setup：

在 IC 設計的介面中把原本做好的 design 的 verilog 設計(.v)引用進來，設定 library 還有 TLU+，然後把 SDC 也引用進來。

☆TLU+檔(.tluplus)：內容為各層 layer 的寄生 RC 值，mapping 檔(.map)為 tf 檔與 itf 檔的 layer 名稱對照表，利用 mapping 檔來將製程檔(.tf)與 TLU+檔(.tluplus)的名稱作對照。(itf 檔可以轉成 tluplus 檔)[3]

IC compiler-Design Planning：

加入 IO、P/G pad、POC pad 和 Corner pad，然後在 floorplan 中把 io.tdf 讀進來，建立 floor plan 並加入 pad filer。

設定 Power 的金屬層還有 Ring Constraints(約束)等等的 power network 然後 synthesize，產生 IR drop 並做 preroute 跟分析。

☆P/G pad：power 和 ground 的 pad

☆POC pad：Power-on Control Power Pad(POC)，power domain 的總開關[4]

☆IR drop：電流經過電阻的時候造成的壓降，也就是 IR=V 的 drop.[5]

☆.tdf：用 AHDL(Altera Hardware Description Language)寫成的一個 ASCII text file (with the extension .tdf) [6]

IC compiler-Placement：

核心的 palcement 設定，測量 power 還有 data arrive time

IC compiler-CTS[7]：

Clock Tree Synthesis，對 clock tree 做分析和優化

IC compiler-Route：

確認 Routing 的可行性並執行 auto routing

三、測資結果

Design Compiler

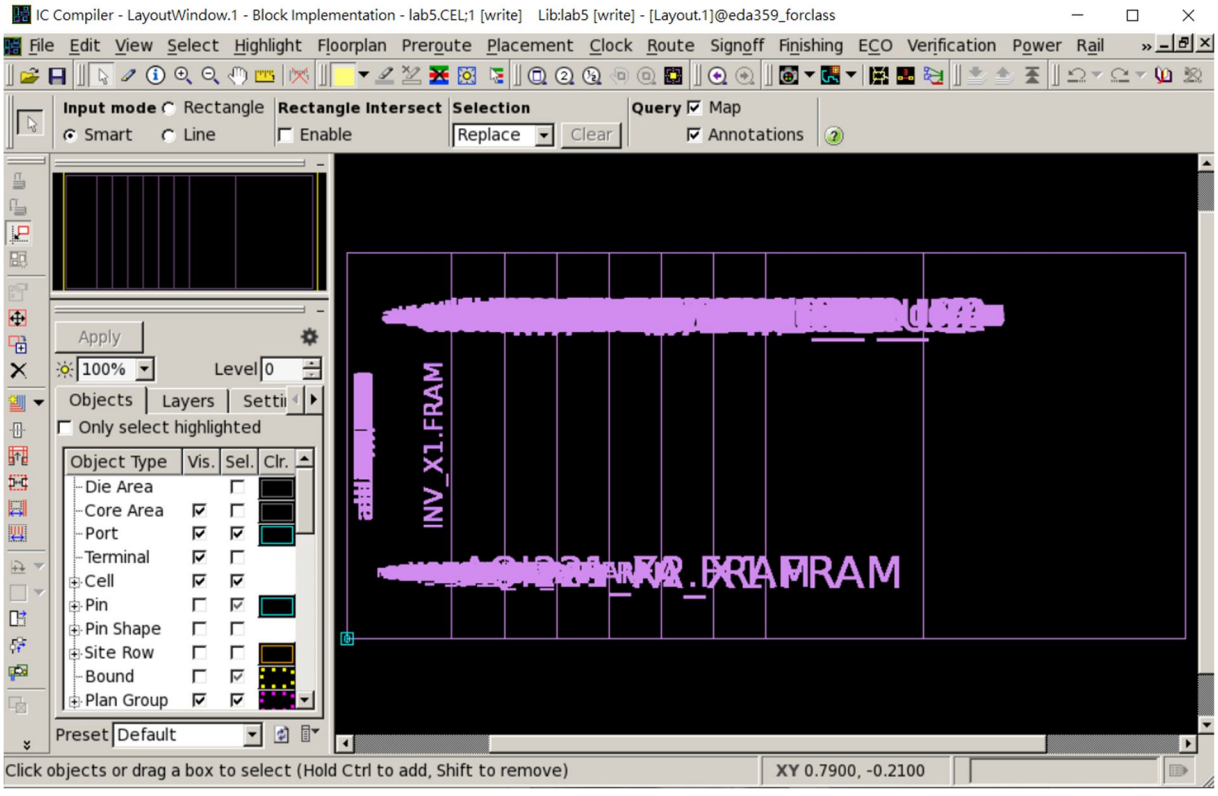
Q1. Area = __6554.239994__ , data arrive time =_3.61__

```
Number of sequential cells:                    0
Number of macros/black boxes:                  0
Number of buf/inv:                           768
Number of references:                         16

Combinational area:               6554.239994
Buf/Inv area:                      408.576004
Noncombinational area:               0.000000
Macro/Black Box area:                0.000000
Net Interconnect area:      undefined  (Wire load has zero net area)

Total cell area:                  6554.239994
Total area:                 undefined

***** End Of Report *****
```

```
alu15/U166/ZN (NAND2_X1)                 0.03       3.57 r
alu15/U167/ZN (OAI211_X1)                0.04       3.61 f
alu15/y[0] (alu_0)                       0.00       3.61 f
Y[120] (out)                             0.00       3.61 f
data arrival time                                   3.61
-----------------------------------------------------------
(Path is unconstrained)


**** End Of Report *****
```

IC compiler- Design Setup

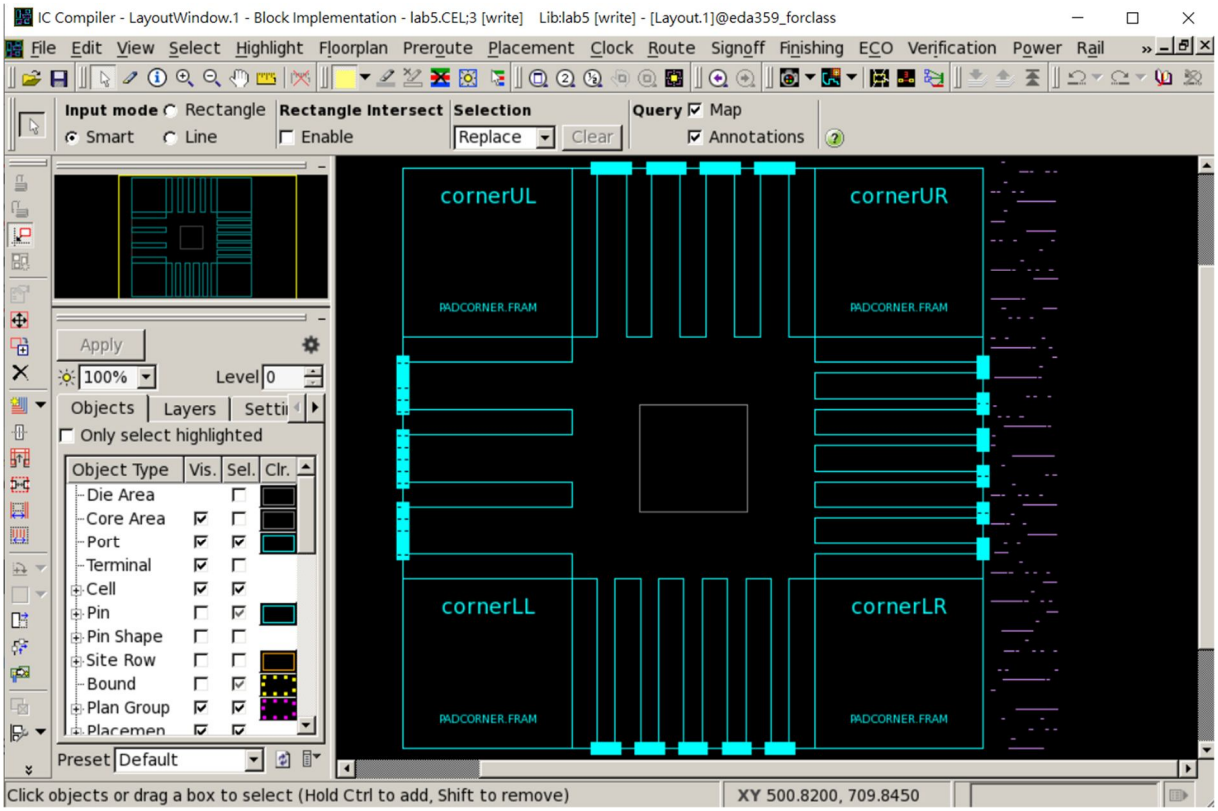
Q2. Please print screen of what you see in IC Compiler LatoutWindow.



IC compiler- Design Planning

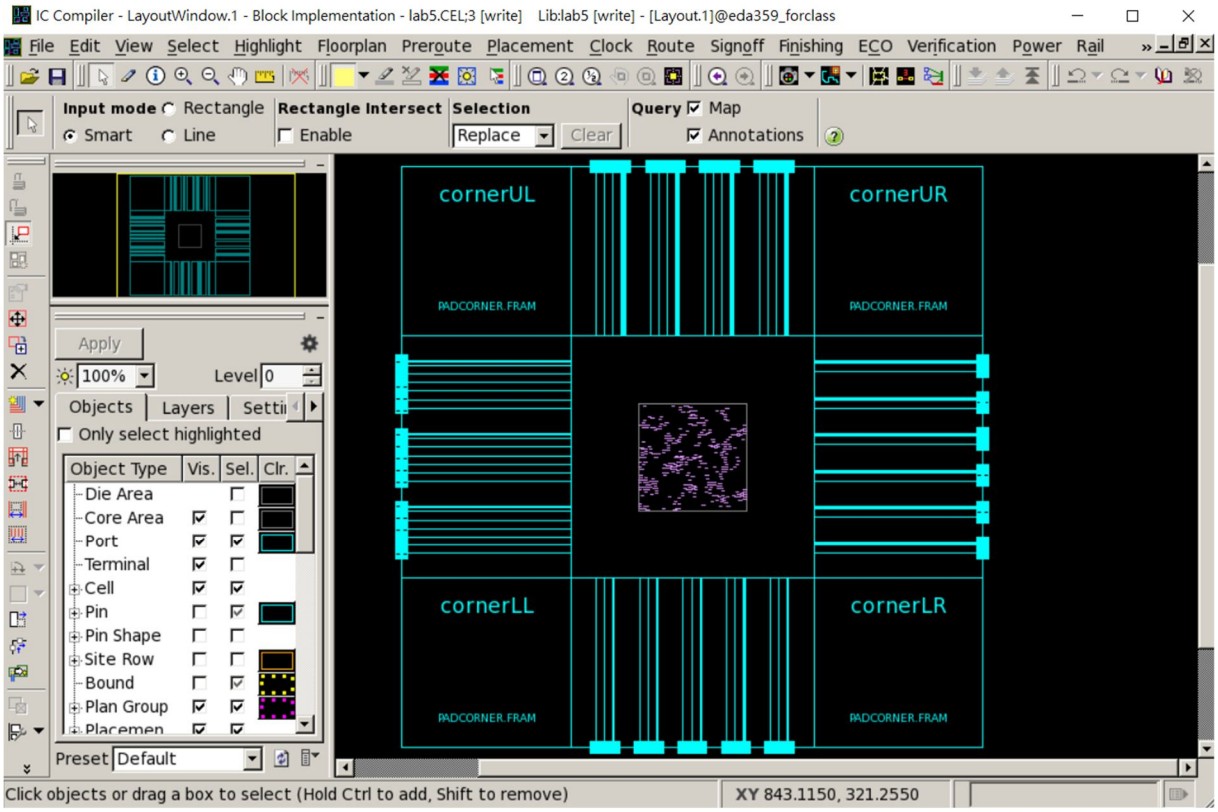
Q3. Please print screen of what you see in IC Compiler LatoutWindow.

What is the difference between Q2 and Q3? 建構出了 core 的形狀，把四個邊的 pin 位置還有 corner 標示出來



Q3. Please print screen of what you see in IC Compiler LatoutWindow.

What is the difference between Q2 and Q3?和上一個步驟不一樣的是已經把設計的部分擺進 chip 裡面

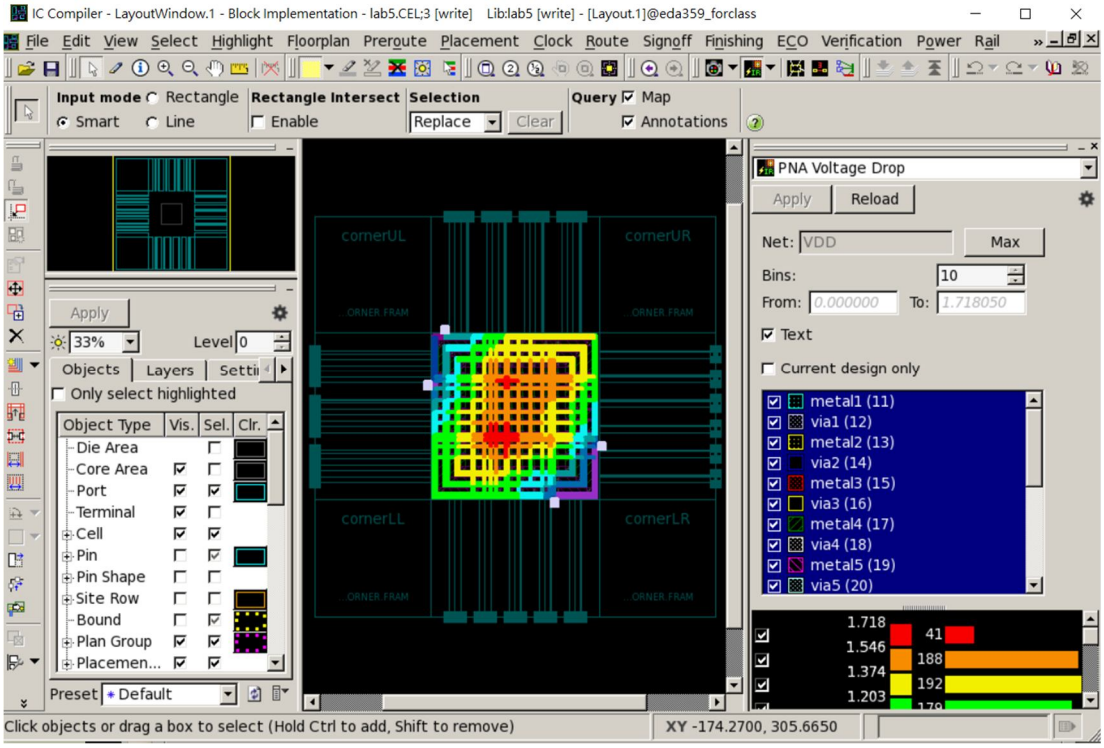


Q4. How many connected power ports and ground ports in this project? _5156_ , _5156_

```
Information: Saved design named before_PNS. (UIG-5)
1
icc_shell> derive_pg_connection -power_net {VDD} -ground_net {VSS} -power_pin {VDD} -ground_pin {VSS}
Information: connected 5156 power ports and 5156 ground ports
1
icc_shell>
```

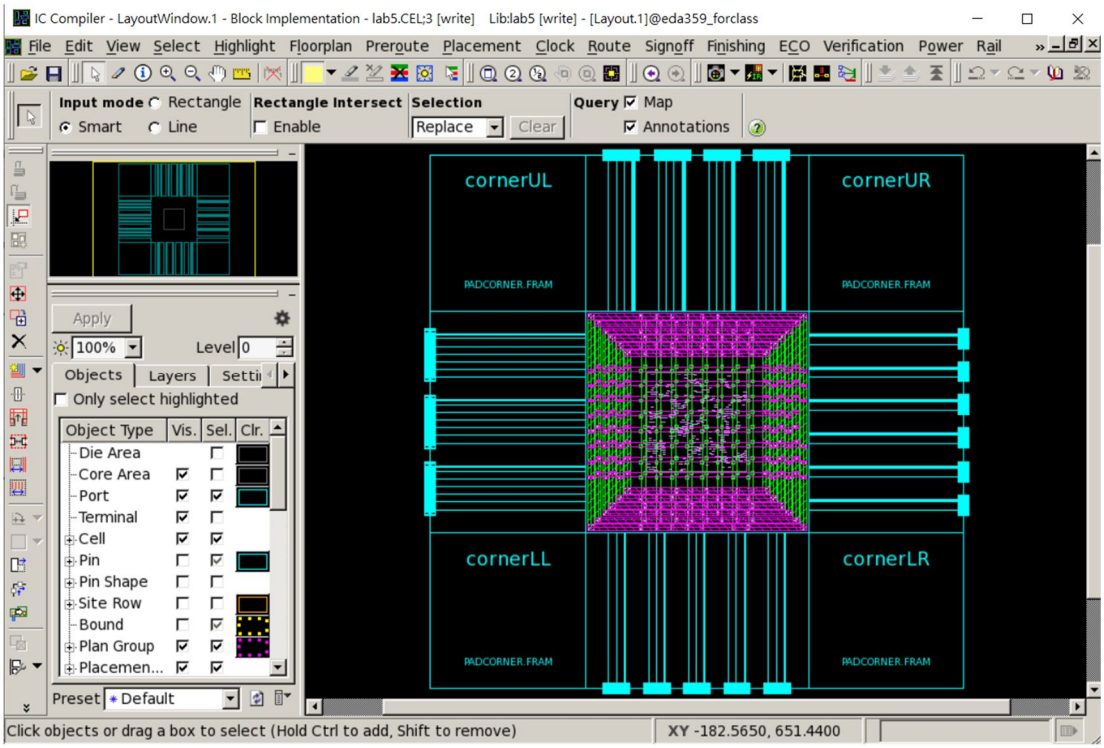
Q5. (a) Please print screen IR drop map.

(b) Explain IR drop 電流經過電阻的時候造成的壓降，也就是 IR=V 的 drop



Q6. Please print screen of what you see in IC Compiler LatoutWindow.

What is the difference between Q3 and Q6? 和 Q3 不一樣的是把每一層的高電壓、低電壓的 LAYER 做出來了



IC compiler- Placement

Q7.

Q8. Internal power = 192.8268uW Switching power =178.1194uW Leakage power = 146.03uW

```
Cell Leakage Power     = 146.0280 uW


                Internal         Switching           Leakage            Total
Power Group     Power            Power               Power              Power   (   %    )  Attrs
--------------------------------------------------------------------------------------------------
io_pad            0.0000           0.0000            0.0000           0.0000  (   0.00%)
memory            0.0000           0.0000            0.0000           0.0000  (   0.00%)
black_box         0.0000           0.0000            0.0000           0.0000  (   0.00%)
clock_network     0.0000           0.0000            0.0000           0.0000  (   0.00%)
register          0.0000           0.0000            0.0000           0.0000  (   0.00%)
sequential        0.0000           0.0000            0.0000           0.0000  (   0.00%)
combinational   192.8628         178.1194        1.4603e+05         517.0110  ( 100.00%)
--------------------------------------------------------------------------------------------------
Total           192.8628 uW      178.1194 uW     1.4603e+05 nW      517.0110 uW
1
icc_shell>
```

Q9. data arrival time = 3.08fs

```
alu1/U167/ZN (OAI211_X1)                0.04 *     2.89 r
alu1/y[0] (alu_14)                      0.00       2.89 f
U100/Z (CLKBUF_X1)                      0.17 *     3.06 f
Y[8] (out)                              0.02 *     3.08 f
data arrival time                                  3.08
-----------------------------------------------------------
(Path is unconstrained)


1
icc_shell>
```

Q10. Internal power =200.5396uW Switching power = 289.8362uW Leakage power =147.19uW

Are the answers of Q8 and Q10 different? Q8 和 Q10 的答案不一樣，在經過 placement 的優化之後可以減少 data arrival 所需的時間但會增加消耗的能量

```
                Internal         Switching           Leakage            Total
Power Group     Power            Power               Power              Power   (   %    )  Attrs
--------------------------------------------------------------------------------------------------
io_pad            0.0000           0.0000            0.0000           0.0000  (   0.00%)
memory            0.0000           0.0000            0.0000           0.0000  (   0.00%)
black_box         0.0000           0.0000            0.0000           0.0000  (   0.00%)
clock_network     0.0000           0.0000            0.0000           0.0000  (   0.00%)
register          0.0000           0.0000            0.0000           0.0000  (   0.00%)
sequential        0.0000           0.0000            0.0000           0.0000  (   0.00%)
combinational   200.5396         289.8362        1.4719e+05         637.5648  ( 100.00%)
--------------------------------------------------------------------------------------------------
Total           200.5396 uW      289.8362 uW     1.4719e+05 nW      637.5648 uW
1
icc_shell>
```

IC compiler-CTS

Q11. Have any error? NO

```
Date   : Wed Jun 16 17:28:32 2021
************************************************
Total messages: 0 errors, 30 warnings

----------------------------------------
Warning Summary for check_physical_design
----------------------------------------

  ------------------------------------------------------------------------
  ID            Occurrences     Title
  ------------------------------------------------------------------------
  PSYN-523      29              Geometries are not integer multiple of width or...
  TLUP-004      1               layer mis-match between TF and ITF (minWidth)
  ------------------------------------------------------------------------
dump check_physical_design result to file ./cpd_pre_clock_opt_2021Jun16172831_7700/index.html
1
icc_shell>
```

IC compiler-Route

Q12. Print Screen “Verify Summary”.

```
Verify Summary:

Total number of nets = 5901, of which 0 are not extracted
Total number of open nets = 0, of which 0 are frozen
Total number of excluded ports = 0 ports of 0 unplaced cells connected to 0 nets
                                 0 ports without pins of 0 cells connected to 0 nets
                                 0 ports of 0 cover cells connected to 0 non-pg nets
Total number of DRCs = 4497
Total number of antenna violations = no antenna rules defined
Total number of voltage-area violations = no voltage-areas defined
Total number of tie to rail violations = not checked
Total number of tie to rail directly violations = not checked

1
icc_shell>
```

四、結論

藉由這一次的作業了解了 EDA 的 tool 是如何把 verilog 檔案轉換成實際的 chip 設計，還有一些必須要設定的東西(例如 power 還有 floor 的繞線還有 layer 等等)、還有設計的部分的配置，要避開電源繞線的地方。
以及經過 ICC 的不同步驟之後對於設計有哪些影響，例如時間或是 FloorPlanning 等。
之前在 VLSI 導論的時候有學過一點點相關知識，也藉由這份作業將一些之前學過的知識串聯在一起。

五、參考資料

[1] https://timsnote.wordpress.com/digital-ic-design/ic-compiler/output-file/ OUTPUT FILE
[2]、[3] https://timsnote.wordpress.com/digital-ic-design/ic-compiler/desigh-setup/ DESIGH SETUP
[4] https://timsnote.wordpress.com/2017/08/09/pad-selection/ IO PAD 的選擇
[5] https://semiengineering.com/knowledge_centers/low-power/architectural-power-issues/ir-drop/ IR Drop
[6] https://stackoverflow.com/questions/30335142/tdf-file-conversion-to-vhdl TDF file conversion to VHDL
[7] https://timsnote.wordpress.com/digital-ic-design/ic-compiler/cts/ CTS