

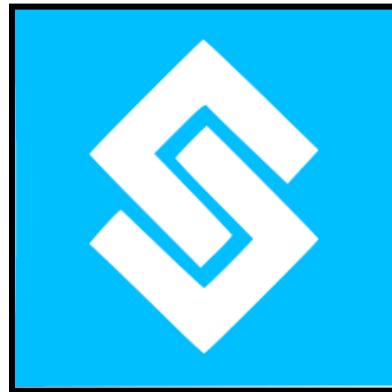
INTERNSHIP REPORT

**Design of Chip On Board (COB) PCB for IC validation
of GaN HEMT (650V/10A)**

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ABSTRACT

This report presents a comprehensive study on Gallium Nitride (GaN) devices and Chip-on-Board (COB) design, focusing on their integration in modern electronic systems.

GaN, a wide bandgap semiconductor, offers significant advantages over traditional silicon-based devices, including higher breakdown voltage, faster switching speeds, and better efficiency at high frequencies. The working principles of GaN transistors have been discussed in detail, highlighting their behavior and suitability for high-power and RF applications.

The second part of the report delves into the design aspects of COB technology, which enables direct mounting of bare GaN dies onto the substrate. This technique not only reduces interconnect length but also enhances electrical performance and thermal dissipation. Various layout strategies and material choices used in COB design are examined, along with the challenges involved in handling GaN devices due to their thermal sensitivity.

Finally, thermal analysis was conducted to evaluate the heat distribution and cooling requirements in COB-based GaN systems. Simulations and calculations were used to assess temperature profiles, enabling optimization of heat sinks, thermal vias, and interface materials. The combination of GaN technology with efficient COB packaging and proper thermal management demonstrates great potential in developing compact, high-efficiency power and RF modules.

ACKNOWLEDGEMENT

I would like to extend my sincere appreciation to all those who supported and guided me during the course of this project. Their encouragement and assistance played a crucial role in bringing this work to completion.

I am especially grateful to **Mr. Roshish Gupta** for his consistent support, insightful guidance, and expert advice throughout the project. His deep understanding of the subject and constructive suggestions were instrumental in navigating challenges and enriching the overall learning experience. Working under his mentorship has not only improved my technical proficiency but also fostered a greater sense of confidence and professional growth. It was truly a privilege to be part of such an encouraging and intellectually stimulating environment.

I would also like to thank **Mr. Jagjeet Singh (Head, VTAD)** and the entire team at the **VLSI Test and Application Development Division** for their cooperation, timely inputs, and access to essential knowledge and tools that were vital to the progress of this project.

Lastly, I am deeply thankful to my parents and friends for their unwavering support, motivation, and belief in me throughout this journey.

SAMVRIT KALA

CHAPTER 1: INTRODUCTION TO ORGANIZATION

1.1 Overview

Semi-Conductor Laboratory (SCL) is an R&D organization functioning under the Ministry of Electronics and Information Technology (MeitY), Government of India. It stands as the nation's only Integrated Device Manufacturing (IDM) facility, offering comprehensive, end-to-end solutions for the development of Application Specific Integrated Circuits (ASICs), MEMS, and opto-electronic devices. SCL encompasses all aspects of the semiconductor development cycle design, fabrication, assembly, testing, and reliability assurance within a single secure campus.

With its Class 100/1000 cleanroom environments and advanced fabrication lines, SCL supports both silicon and MEMS-based technologies and contributes significantly to the development of strategic and commercial electronics in the country.

1.2 Technical Activities

SCL's technical ecosystem includes a wide spectrum of specialized areas, with integrated facilities to support multiple stages of semiconductor production. The core activities include:

- VLSI Design & Process Development
- Fabrication of CMOS & MEMS Devices
- Device Assembly and Packaging
- Hi-Reliability Component Screening
- MEMS Process and Wafer Level Packaging
- Reliability Testing and Quality Assurance
- Technical and Engineering Support Services

These activities are supported by high-end EDA tools, sophisticated characterization labs, and advanced metrology infrastructure, enabling design-to-delivery capability in microelectronics.

1.3 Vision of SCL

SCL envisions itself as a Center of Excellence in microelectronics, striving to:

- Establish a robust R&D base in advanced semiconductor technologies.
- Design and develop cutting-edge microelectronic devices in CMOS, MEMS, and optoelectronics.
- Manufacture VLSI and MEMS-based systems and subsystems for strategic sectors.
- Promote self-reliance in semiconductor manufacturing and reduce dependence on foreign technologies.

Through its commitment to innovation and national service, SCL plays a critical role in strengthening India's capabilities in the microelectronics domain

CHAPTER 2: LITERATURE REVIEW

2.1 Fred Yue Fu, GaNPower International Inc.

Title: "*GaN Power HEMT Tutorial: GaN Basics, Design, Testing, and Applications*"

Published by: GaNPower International Inc., 2022

This comprehensive tutorial provides an in-depth overview of GaN High Electron Mobility Transistors (HEMTs), including their material characteristics, structural design with a comparison of wide bandgap semiconductors, specifically GaN, SiC, and traditional silicon, emphasizing GaN's superior breakdown field, electron mobility, and Baliga's figure of merit. Detailed cross-sectional views of E-mode and D-mode GaN HEMTs are presented, alongside substrate considerations like Si, SiC, and sapphire. The tutorial further explains the absence of avalanche breakdown in GaN and why p-type GaN HEMTs are not feasible due to poor hole mobility and challenges in Mg doping.

The fabrication section includes step-by-step process flows for GaN-on-sapphire HEMTs, using mesa etching, gate lithography, Schottky metal deposition, and SiN passivation. Transient simulations illustrate phenomena such as current collapse and dynamic $R_{DS(on)}$ degradation. Measurement methodologies for DC and dynamic parameters—such as threshold voltage, gate charge (Q_g), capacitances (C_{iss} , C_{oss}). The tutorial concludes with reliability testing standards (e.g., HTGB, HTRB, Temp Cycling) and modeling techniques using behavioral compact models.

The document served as a key reference for understanding the thermal limitations and integration challenges of GaN devices, especially relevant for my work on PCB-based thermal design and COB integration of GaN power devices.

Source: F. Yue Fu, *GaN Power HEMT Tutorial*, GaNPower International Inc., 2022.

2.2 Ander Udabe et al., University of Mondragon

Title: "*Gallium Nitride Power Devices: A State of the Art Review*"

Published in: IEEE Access, 2021

This paper provides a detailed state-of-the-art overview of Gallium Nitride (GaN) power devices, focusing on their structural, material, and performance characteristics in power electronics. It highlights GaN's superior wide bandgap properties, such as high breakdown field (3.3 MV/cm), electron mobility (1500–2000 cm²/V·s), and saturation velocity, which collectively make it suitable for compact, high-efficiency power converters. The review compares GaN with Silicon (Si) and Silicon Carbide (SiC), establishing GaN's potential in reducing on-resistance and increasing switching speed, although acknowledging its current limitations in standardization and commercial maturity.

The authors provide insights into GaN's crystal structure, particularly the wurtzite phase, and the role of spontaneous and piezoelectric polarization in forming the 2DEG channel, a critical feature of GaN HEMTs. The paper also explains why current GaN devices are based on lateral HEMT structures due to challenges in fabricating high-quality vertical GaN wafers. Several enhancement-mode (e-mode) and hybrid GaN transistor architectures are discussed, including p-GaN gate HEMTs.

One of the most valuable contributions of the paper is its deep dive into real-world challenges like dynamic on-resistance and output capacitance (C_{oss}) losses, which are critical for engineers during power converter design. The paper links these issues to crystal defects and trap states, offering guidance on temperature, voltage, and layout dependencies. Overall, this work provided me with strong foundational knowledge of the limitations and emerging design approaches for GaN in practical power electronics.

Source: A. Udabe et al., "*Gallium Nitride Power Devices: A State of the Art Review*," IEEE Access, 2021. DOI: 10.1109/ACCESS.2023.3277200

CHAPTER 3: GaN TECHNOLOGY

3.1 Overview of GaN technology

Gallium nitride (GaN) is a binary, polar III/V direct bandgap semiconductor that has revolutionized various electronic and optoelectronic applications.

Its unique properties because of its crystal structure, primarily the wurtzite (asymmetric hexagonal) form, which is stable at room temperature, though it can also exist in a metastable zinc blende (cubic) form. The lattice parameters are:

$$a=3.189 \text{ \AA}$$

$$c=5.185 \text{ \AA}$$

The direct bandgap of GaN is 3.4 eV and is significantly wider than that of traditional silicon (1.1 eV), allowing GaN to handle higher voltages, switch faster, and operate at higher temperatures with greater efficiency. This makes it an ideal material for next-generation power electronics, high-frequency devices, and advanced lighting solutions.

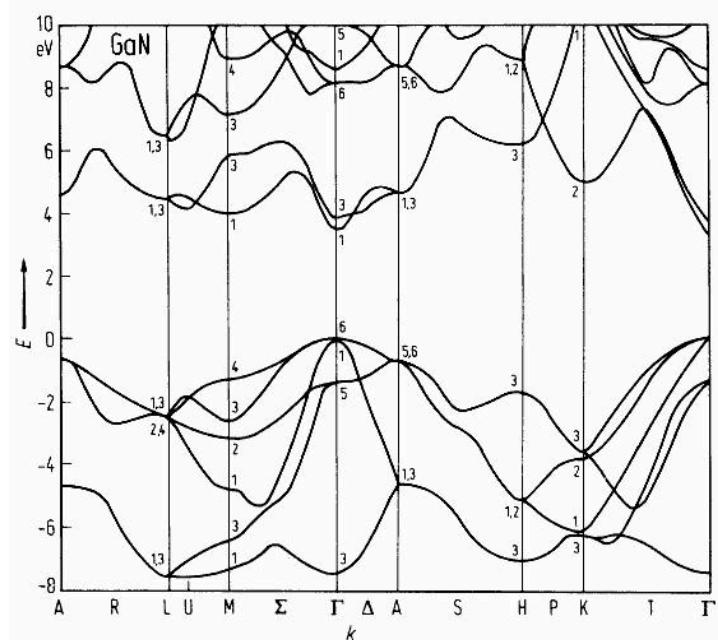


Figure 1 GaN Band Structure

3.2 Properties of GaN

- Wide Direct Band Gap: At approximately 3.4 eV, GaN's wide direct bandgap allows for efficient light emission (making it crucial for LEDs and laser diodes) and enables devices to withstand higher electric fields and operate at higher temperatures compared to silicon.
- High Electron Mobility: GaN exhibits high electron mobility (typically 900-2000 cm²/Vs), which translates to faster switching speeds and reduced energy losses in electronic devices.
- High Breakdown Voltage: With a critical electric field significantly higher than silicon, GaN devices can handle much higher voltages without experiencing electrical breakdown, making them suitable for high-power applications.
- Good Thermal Conductivity: GaN possesses good thermal conductivity (around 100-200 W/mK), which helps in dissipating heat efficiently, contributing to the reliability and longevity of GaN-based devices, especially in high-power scenarios.
- Radiation Hardness: GaN's inherent properties make it relatively immune to the effects of radiation, making it valuable for aerospace and defense applications.
- High Saturation Velocity: GaN has a high electron saturation velocity, further contributing to its ability to operate at high frequencies.

CHAPTER 4: TUNABLE WIDE BANDGAP MATERIALS

4.1 Aluminium Gallium Nitride

Aluminum Gallium Nitride (AlGaN) is a ternary compound alloy formed by combining Aluminum Nitride (AlN) and Gallium Nitride (GaN).

This alloy, with a mole fraction 'x' of aluminum and $(1-x)$ of gallium (represented as $\text{Al}_x\text{Ga}_{1-x}\text{N}$), holds immense significance in advanced semiconductor technologies. When grown epitaxially on GaN, it typically adopts the wurtzite crystal structure, similar to its GaN counterpart. The ability to tailor its properties by simply adjusting the aluminum content 'x' makes AlGaN an incredibly versatile material for applications ranging from deep-ultraviolet (UV) optoelectronics to high-power and high-frequency electronic devices.

4.2 Bandgap tuning and bowing effect

Tunable Direct Bandgap: One of the most remarkable features of AlGaN is its widely tunable direct bandgap. It ranges nonlinearly from 3.4 eV (for pure GaN, when $x=0$) to 6.2 eV (for pure AlN, when $x=1$). This nonlinearity is a result of the bowing effect.

Bowing Effect: In many semiconductor alloys, including AlGaN, the bandgap energy does not vary linearly with the composition (mole fraction 'x') but instead exhibits a downward deviation from linearity. This deviation is known as the "bowing effect." It is attributed to various factors, including:

- Disorder in the crystal lattice
- Differences in atomic size and electronegativity: The differing atomic sizes and electronegativities of Al and Ga atoms create strain and charge transfer effects that influence the electronic band structure.

The bandgap of AlGaN can generally be described by the following quadratic equation:

$$E_g(x) = x \cdot E_g(\text{AlN}) + (1-x) \cdot E_g(\text{GaN}) - b \cdot x \cdot (1-x)$$

Where: $E_g(x)$ is the bandgap of $\text{Al}_x\text{Ga}_{1-x}\text{N}$, $E_g(\text{AlN})$ is the bandgap of AlN (6.2 eV), $E_g(\text{GaN})$ is the bandgap of GaN (3.4 eV), and 'b' is the bowing parameter. For AlGaN, the bowing parameter 'b' typically falls in the range of 0.8 to 1.3 eV, indicating the extent of the nonlinearity.

4.3 Crystal Structure and Lattice Parameters

Crystal Structure: Primarily wurtzite (hexagonal) structure, especially when grown epitaxially on GaN substrates. This maintains the advantageous properties associated with the wurtzite form, such as spontaneous and piezoelectric polarization.

Lattice Parameters (following Vegard's Law): The lattice parameters of $\text{Al}_x\text{Ga}_{1-x}\text{N}$ approximately follow Vegard's Law.

- $a = x \cdot 3.112 \text{ \AA} + (1-x) \cdot 3.189 \text{ \AA}$
- $c = x \cdot 4.982 \text{ \AA} + (1-x) \cdot 5.185 \text{ \AA}$

Vegard's Law: This is an empirical rule in materials science that states that for a solid solution of two components, the lattice parameter (or other physical properties like density or refractive index) varies linearly with the mole fraction of the constituents.

In essence, it suggests that if you mix two materials, A and B, to form an alloy A_xB_{1-x} , then a property 'P' of the alloy can be approximated as a weighted average of the properties of the pure components:

$$P(A_xB_{1-x}) = x \cdot P(A) + (1-x) \cdot P(B)$$

High Electron Mobility Transistors (HEMTs): The formation of AlGaN/GaN heterostructures is critical for creating two-dimensional electron gas (2DEG). This 2DEG forms at the interface due to spontaneous and piezoelectric polarization effects, leading to high electron mobility and high electron density, which are essential for high-power, high-frequency, and high-temperature operation in HEMTs.

CHAPTER 5: DEVICE PHYSICS

5.1 Heterojunctions

A heterojunction is created by bringing together two distinct semiconductor materials, each possessing different band gaps, electron affinities, or lattice constants.

- This unlocks a powerful degree of control over band alignment, carrier transport, and charge confinement.
- This capability to "engineer" the band structure allows for significant improvements in device performance, enabling the formation of advanced structures like quantum wells and two-dimensional electron gases (2DEGs), which are vital for confining charge carriers.

To achieve a high-quality heterojunction, several critical criteria must be met:

- Lattice Matching: A primary consideration is the similarity in lattice constants between the two semiconductor materials. A significant mismatch can lead to the formation of defects, specifically dislocations, which severely degrade device performance by acting as recombination centers for charge carriers or scattering centers that impede their flow. However, it's worth noting that a controlled amount of lattice strain can be intentionally utilized to engineer the heterojunction for improved mobility or to modify the band structure in a desirable way, provided that the strained layer remains thin and below its critical thickness, beyond which dislocations would form.
- Epitaxial Growth: The layers must be grown atom-by-atom, precisely following the crystal structure of the underlying substrate. This atomic-level control is crucial for forming a planar and uniform crystalline interface, which is absolutely essential for efficient carrier transport and reliable device operation. To achieve such precise and high-quality layers, sophisticated growth techniques are employed, predominantly Metal-Organic Chemical Vapor Deposition (MOCVD) and Molecular Beam Epitaxy (MBE). These methods offer atomic-level control over the composition and thickness of each layer, a capability that is critical for intricate bandgap engineering and precise doping profiles.

- Clean and Sharp Interface: The interface between the two materials must be impeccably clean and atomically sharp. Any contamination or roughness at this critical boundary can introduce undesirable traps and scattering centers, which reduce carrier mobility and recombination efficiency. Furthermore, good thermal and chemical compatibility between the materials is essential to ensure that they do not degrade or react adversely during the often high-temperature growth processes.

The transition between the two semiconductor materials in a heterojunction can be realized in different ways, leading to distinct electrical characteristics:

1. Abrupt Heterojunction: In an abrupt heterojunction, the material composition changes very sharply, ideally within one or two atomic layers. This results in a sudden, step-like discontinuity in the band edges (conduction band and valence band). Abrupt heterojunctions are simpler to grow and are commonly used to create sharp potential steps for carrier confinement, such as in quantum wells and the channel of HEMTs where a 2DEG is formed at the interface due to the abrupt change in properties and often strong polarization fields. The sudden change can, however, present a barrier to carrier transport if the band offset is large.
2. Graded Heterojunction: A graded heterojunction features a gradual change in the material composition over a certain thickness, typically tens or hundreds of nanometers. This gradual change in composition leads to a smooth, sloped transition in the band edges rather than an abrupt step.

Graded heterojunctions are designed for smooth carrier transport, reduce interface states, provide built-in electric fields (built-in electric field that can accelerate carriers in a desired direction, further enhancing device performance)

5.2 Band alignment

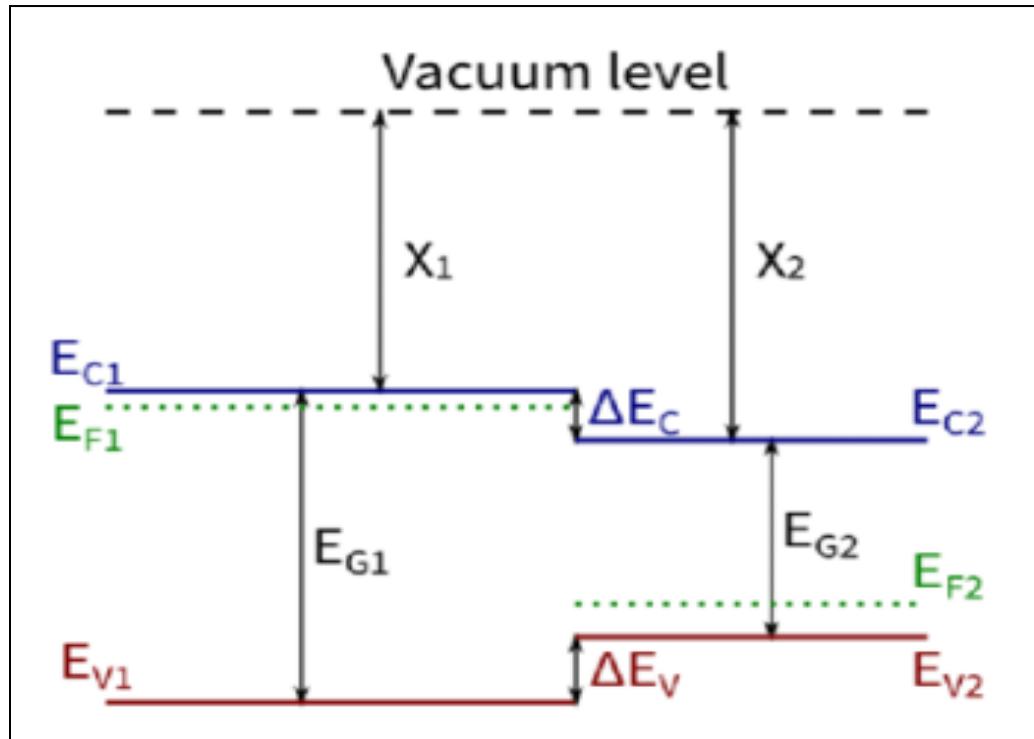


Figure 2 Band alignment and bending before contact of AlGaN and GaN

- This diagram shows the energy band diagrams of two isolated semiconductors, labeled 1 and 2 (e.g., AlGaN and GaN), before physical contact.

Electron affinities: χ_1 and χ_2 Bandgaps: E_{G1} , E_{G2}

Conduction and valence band offsets: $\Delta E_C = E_{C1} - E_{C2}$ $\Delta E_V = E_{V2} - E_{V1}$

- The Fermi levels E_{F1} , E_{F2} are not yet aligned.

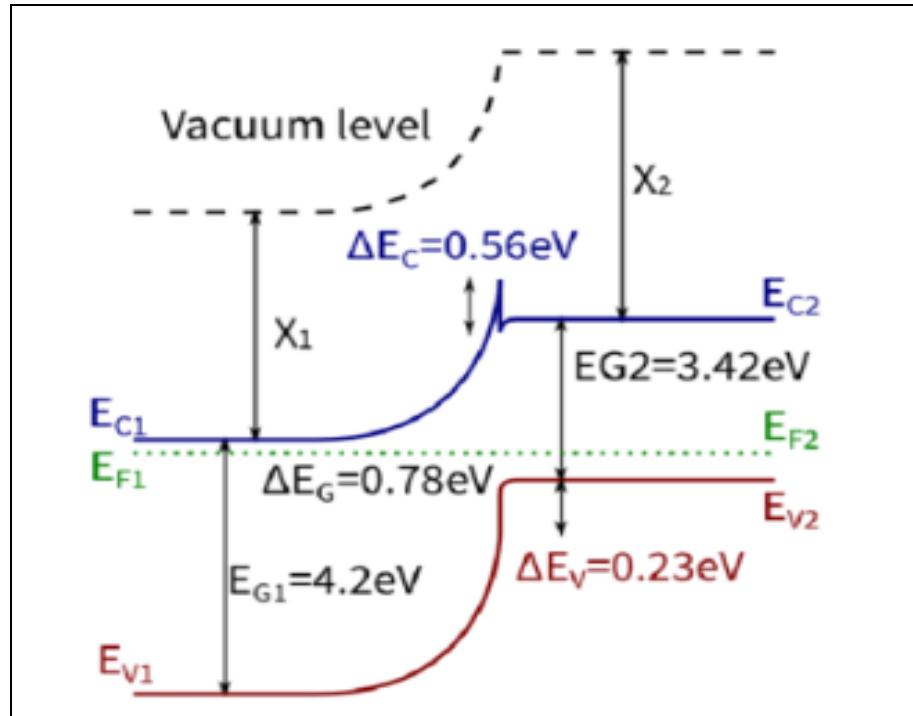


Figure 3 Band alignment and bending after contact of AlGaN and GaN

- After contact, Fermi levels align at equilibrium, causing band bending.
- This represents a typical heterojunction band alignment , assuming non polarization effects.
- The material on the left (AlGaN) has higher band gap: $E_{G1}=4.2 \text{ eV}$
- The material on the right (GaN) has smaller band gap: $E_{G2}=3.42 \text{ eV}$

5.3 Spontaneous polarization in AlGaN/GaN

GaN is polar in nature due to:

- A large electronegativity difference between Ga (less electronegative) and N (more electronegative).
- Its non-centrosymmetric wurtzite crystal structure, which lacks symmetry along the c-axis (Z-direction).

In the wurtzite structure, atoms are arranged in an asymmetric hexagonal pattern, creating a built-in polarization vector pointing from Ga to N.

This leads to a net spontaneous polarization along the Z-axis:

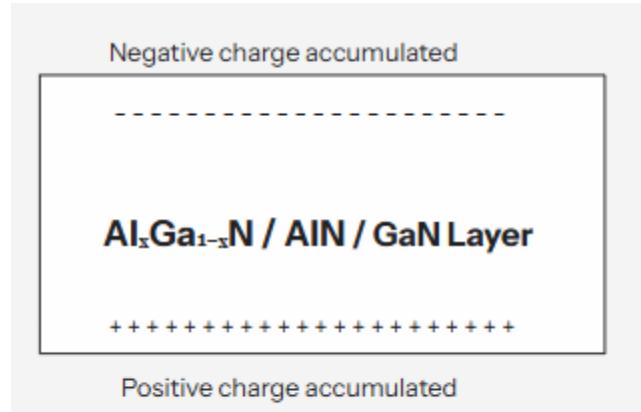


Figure 4 Spontaneous Polarization

- -0.029 C/m^2 for GaN
- -0.081 C/m^2 for AlN

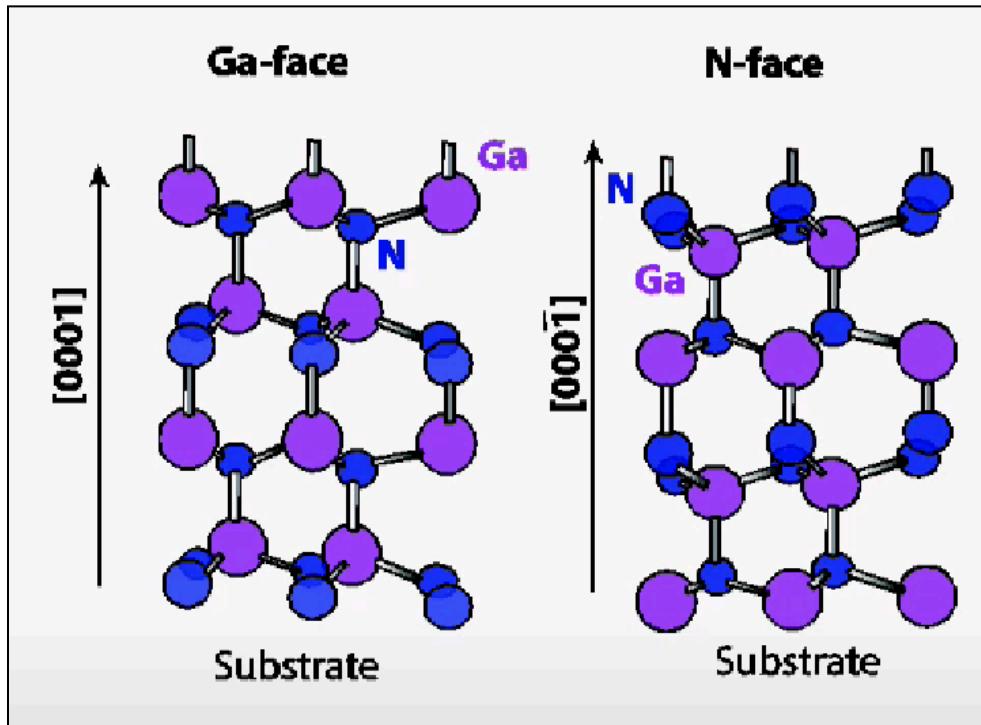


Figure 5 Ga polar and N polar GaN

- The negative sign indicates that the polarization vector points from substrate (bottom) to surface (top) in Ga-polar GaN.

In Ga-polar GaN: Negative polarization charge builds up at the top surface and positive charge at the bottom. As a result, an electric field is set up pointing downward (top to bottom).

In N-polar GaN: The atomic orientation is reversed (N at bottom, Ga at top). This reverses the direction of polarization and thus the surface charge and electric field direction, which significantly affects device physics.

5.4 Piezoelectric polarization in AlGaN/GaN

In addition to spontaneous polarization (caused by crystal asymmetry and dipole alignment in wurtzite GaN), GaN-based heterostructures also exhibit piezoelectric polarization due to strain at the heterojunction.

- AlGaN has a smaller lattice constant than GaN. So, when a thin AlGaN layer is grown on a thicker GaN substrate, it undergoes tensile strain (stretched to match the GaN lattice).

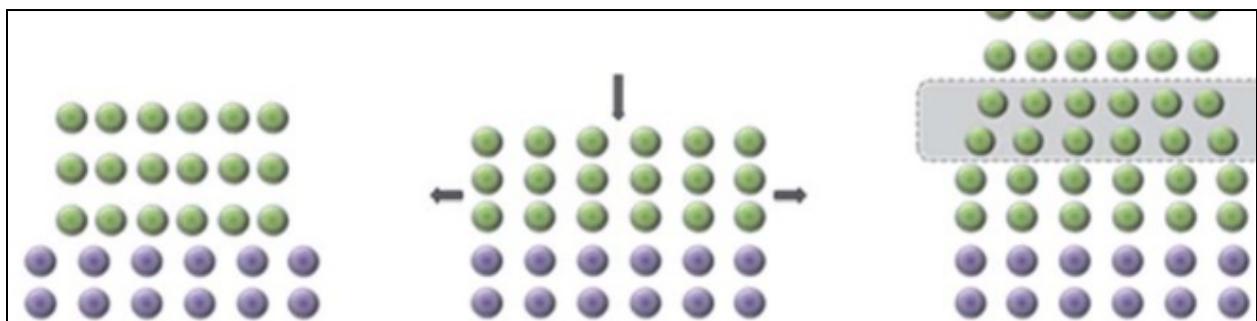


Figure 6 Tensile Strain in AlGaN layer

- This tensile strain induces piezoelectric polarization in the same direction as spontaneous polarization (from Ga to N, i.e., from substrate to surface in Ga-polar orientation).

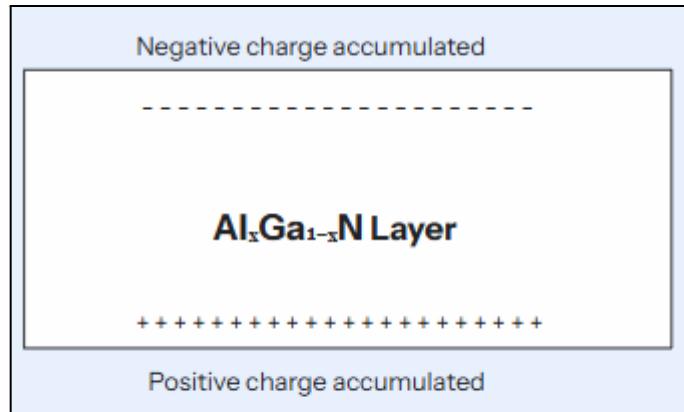


Figure 7 Piezoelectric polarization in AlGaN

- The reason for the same polarity is that when the AlGaN is stretched, it distorts the tetrahedral bonds in a way that further shifts charge centers in the same direction as the existing dipole alignment of the wurtzite structure—thereby reinforcing the built-in spontaneous polarization.
 - In contrast, in materials like InGaN, where InN has a larger lattice constant than GaN, the strain is compressive (InGaN tries to shrink to match GaN), which causes the piezoelectric polarization to oppose the spontaneous polarization direction.

Thickness Considerations and Critical Thickness:

- The more tensile strain, the stronger the piezoelectric polarization, but only up to a certain limit.
 - If the AlGaN layer becomes too thick, the strain energy builds up and eventually exceeds the critical thickness, beyond which the layer relaxes by forming cracks or dislocations.
 - For typical GaN/AlGaN systems, the critical thickness for AlGaN is a few tens of nanometers, depending on composition (Al content). Usually, 20–30 nm is safe for HEMT applications.
 - The GaN layer, being much thicker, absorbs no stress and remains relaxed, so no piezoelectric polarization is induced in the GaN substrate.

5.5 Formation of 2DEG in AlGaN/GaN

- In Ga-polar AlGaN/GaN HEMTs, both spontaneous and piezoelectric polarization vectors point in the same direction (from Ga to N).
- This causes the total polarization charge at the interface to be the sum of the two, leading to a stronger built-in electric field.

The electric field enhances conduction band bending. When the conduction band dips below the Fermi level, electrons begin to accumulate in that region. This leads to formation of a quantum well and 2DEG within a depth of 20–22 nm.

Once the conduction band reaches the Fermi level, further bending is screened by the accumulated electrons, causing the bands to flatten.

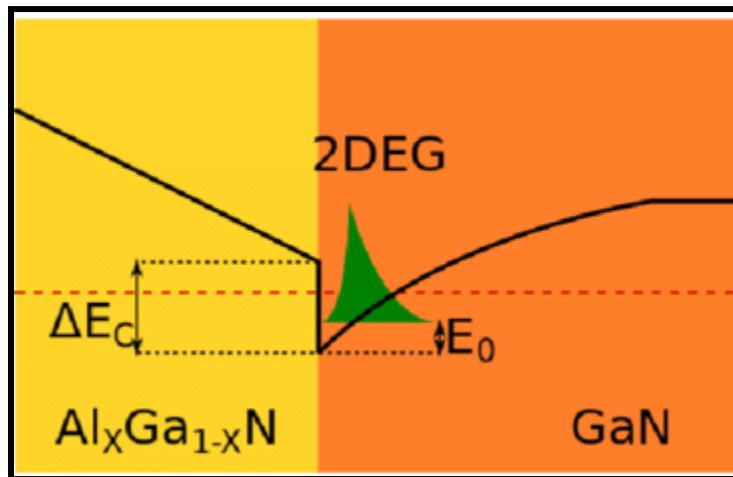


Figure 8 Band diagram of GaN HEMT

- Bottom of GaN Layer: It's usually canceled out by the material underneath (like a conductive substrate or a thick GaN buffer layer). So, it generally doesn't impact how the device works.
- AlGaN/GaN Interface: The AlGaN layer creates positive polarization charges at its lower side. The GaN layer creates negative polarization charges at its upper side. These charges at the interface are crucial because they significantly influence the device's electrical properties.
- Top Surface of AlGaN Layer: At the very top surface of the AlGaN, there's a net negative polarization charge. This negative charge is partially balanced by positive free charges that accumulate at the surface. These positive charges come

from things like dangling bonds (atoms with unsatisfied connections), adsorbed moisture, and other surface defects (collectively called "surface donors"). They act like positive charges that help neutralize the negative polarization charge on the AlGaN.

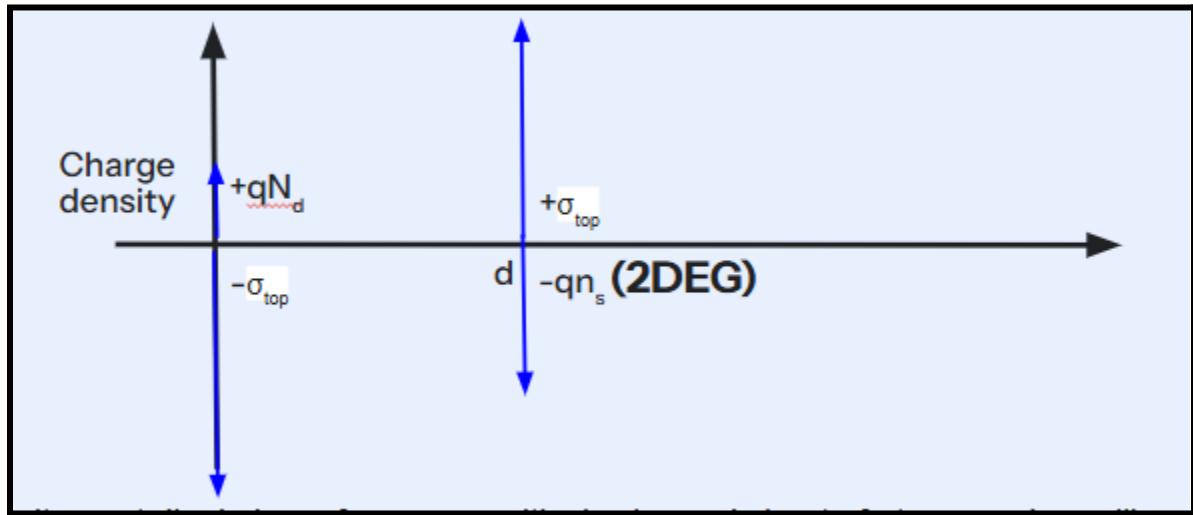


Figure 9 Charge density at various depth starting from top of AlGaN layer

At the top surface of the AlGaN, there is a localized negative charge density ($-\sigma_{\text{top}}$) from the AlGaN polarization. Counteracting this is a positive charge density ($+qN_d$) representing the accumulated surface donors.

At the AlGaN/GaN interface, there is a sharp spike representing a positive sheet charge density ($+σ_{\text{top}}$) on the AlGaN side, immediately followed by an equally sharp spike representing a negative sheet charge density ($-qN_s$) on the GaN side.

Electric Fields from Maxwell's Law:

$$\nabla \cdot \mathbf{E} = \frac{\rho}{\epsilon_0}$$

Where : E is the electric field

ρ is the charge density.

Thus, electric field graph will be:

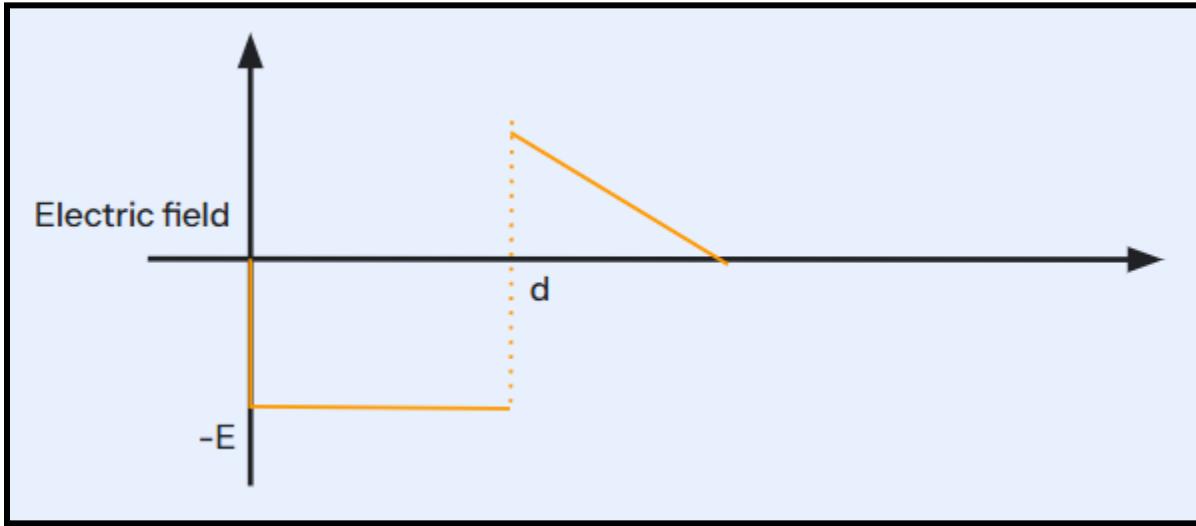


Figure 10 Electric field at various depth starting from top of AlGaN layer

Consequence: Band Bending

The intense electric fields generated by these polarization charges have a profound effect on the electronic band structure of the semiconductor materials. This phenomenon is known as band bending.

In AlGaN/GaN heterostructures, the specific direction and magnitude of the electric field due to the polarization charges lead to a significant downward bending of the conduction band at the AlGaN/GaN interface.

This band bending creates a triangular potential well at the interface, which effectively confines electrons to form a highly dense, two-dimensional electron gas (2DEG). This 2DEG is the operational heart of many high-electron-mobility transistors (HEMTs) based on AlGaN/GaN.

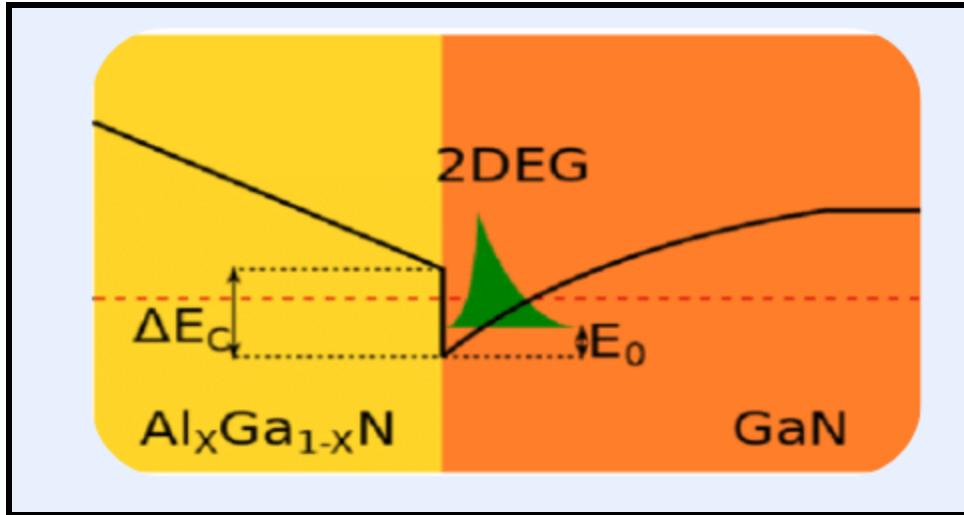


Figure 11 Band bending and formation of 2DEG

In a High Electron Mobility Transistor (HEMT) built with an AlGaN/GaN heterostructure, the formation of a Two-Dimensional Electron Gas (2DEG) is central to its operation.

The spontaneous and piezoelectric polarization lead to a strong electric field which directly influences the energy bands. The conduction band in the GaN layer bends sharply downward as it approaches the interface. This downward bending creates a distinctive "dip" or a triangular-shaped potential well in the conduction band energy.

When the conduction band edge (the lowest energy level available for electrons) dips below the Fermi level in this triangular well region within the GaN, it becomes energetically favorable for electrons to occupy these low-energy states.

Electrons from the surrounding material (e.g., unintentionally doped GaN or even supplied by surface donors at the AlGaN surface) will spontaneously accumulate and fall into this potential well. Because this well is incredibly narrow (on the order of a few nanometers) and confined strictly to the interface.

The 2DEG is :

- Confined in the vertical direction: Cannot move freely up or down.
- Free to move in the lateral directions: Can move parallel to the interface.

This confinement in one dimension, while allowing free movement in the other two, is precisely what defines a Two-Dimensional Electron Gas (2DEG). It's a high-density sheet of electrons with extremely high mobility, making it ideal for high-speed device operation.

5.6 GaN Normally ON device

The formation of the 2DEG at the AlGaN/GaN interface is an intrinsic property of the material system, driven by the polarization charges and band alignment. This means that:

- Even with zero voltage applied to the gate ($V_{GS} = 0V$), the 2DEG already exists and acts as a highly conductive channel.
- Therefore, the device is inherently "ON" (i.e., it conducts current) by default.

To turn off a normally ON HEMT, you must apply a negative voltage to the gate. This negative gate voltage pushes the electrons out of the 2DEG channel by raising the conduction band above the Fermi level, thereby depleting the channel of carriers and stopping the current flow.

Implications and Safety Concerns

The "normally ON" characteristic, while offering certain advantages in some circuit designs, presents significant drawbacks for many applications:

- Safety Concerns: In critical systems, a device that automatically conducts current upon power-up (even at 0V gate bias) can be a major safety hazard.
- Circuit Complexity: Designing circuits with normally ON devices often requires additional components or more complex control schemes to ensure the device is safely in the "OFF" state before operation begins.
- Standby Power: Even in a standby mode, if not properly biased with a negative voltage, a normally ON device could draw some leakage current.

Due to these reasons, there's significant research and development focused on creating "normally OFF" (enhancement-mode) GaN HEMTs, which require a positive gate voltage to turn them ON, thus providing a safer and often simpler operation for power electronics and switching applications.

CHAPTER 6: DEVICE ENGINEERING

6.1 p-GaN doping and Threshold control

p-GaN stands for p-type Gallium Nitride. It is created by doping undoped (intrinsic) GaN with acceptor atoms. The most common acceptor dopant for GaN is Magnesium (Mg). When Mg atoms are incorporated into the GaN crystal lattice, they create holes as the majority charge carriers. This makes the GaN material conductive via holes, rather than electrons.

To achieve enhancement-mode operation, a thin layer of p-GaN is strategically grown on top of the AlGaN barrier layer in the AlGaN/GaN heterostructure.

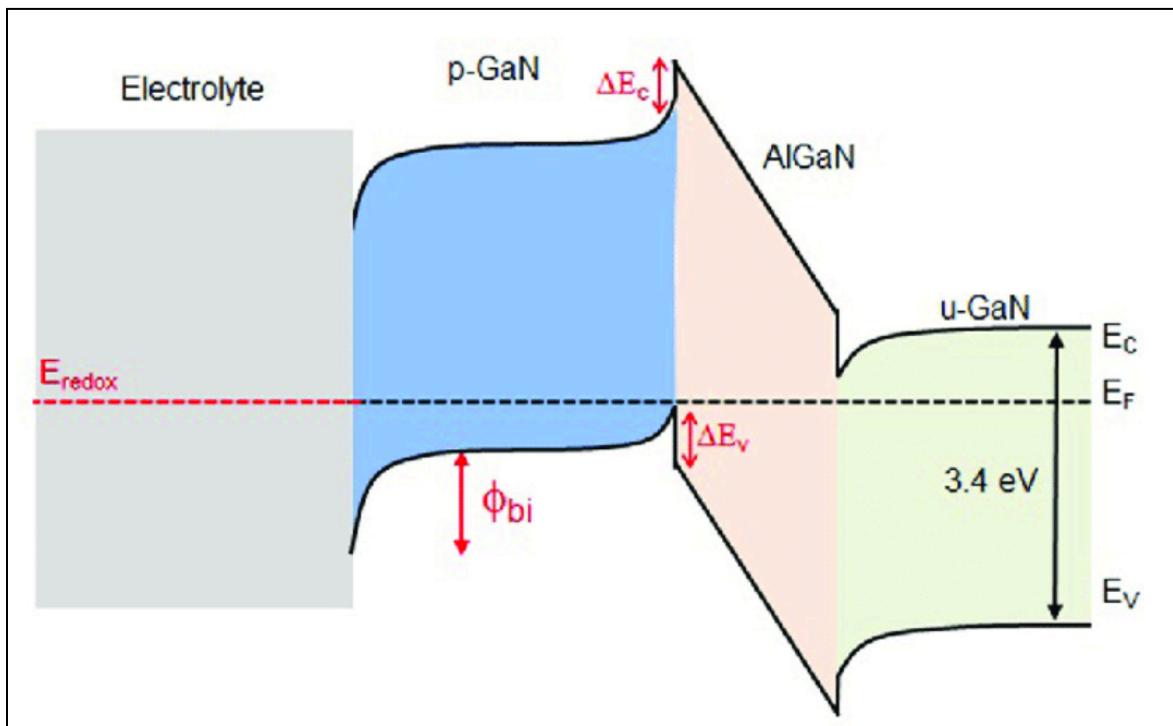


Figure 12 Band diagram of p-GaN

Band Bending and 2DEG Depletion at Zero Bias: The p-GaN layer, being p-type, has a Fermi level closer to its valence band. When this p-GaN layer is placed in contact with the AlGaN barrier, the difference in work functions and band alignment causes the energy bands to bend significantly.

The presence of the p-GaN layer (with its ionized acceptor impurities) pulls up the conduction band in the underlying AlGaN/GaN channel region. This upward shift of the conduction band at the AlGaN/GaN interface is designed so that, at zero gate voltage ($V_{GS} = 0V$), the conduction band edge is lifted above the Fermi level.

When the conduction band is above the Fermi level, there are no energetically favorable states for electrons to occupy at the interface. Therefore, the 2DEG is completely depleted or at least significantly suppressed. This effectively "blocks" or "pinches off" the channel, making the device "normally OFF."

Achieving Conduction with a Positive Gate Voltage:

- To turn the device ON and allow current to flow, a positive voltage (V_{GS}) must be applied to the gate.
- This positive gate voltage attracts electrons towards the interface and pushes the conduction band downward, back below the Fermi level.
- Once the conduction band dips below the Fermi level, electrons can once again accumulate in the triangular potential well, forming the 2DEG channel and enabling current flow.

6.2 Characteristics of p-GaN

- Normally OFF (Enhancement mode): The primary advantage is that the device does not conduct current at 0V gate bias, providing inherent safety and simpler circuit design compared to depletion-mode devices.
- Positive Gate Threshold Voltage (V_{TH}): The gate voltage required to turn the device ON is positive. Typically, the threshold voltage for p-GaN HEMTs ranges from around +1.0V to +2.5V, although research continues to push this higher for better noise immunity and wider operating margins (some advanced designs aim for >3V or even >7V). Achieving a robust and stable positive V_{TH} is a key design consideration, influenced by factors like p-GaN thickness, doping concentration, and the AlGaN barrier properties.

- Safety and Simplicity: The normally OFF behavior eliminates the need for negative biasing at startup, simplifying power converter designs and improving overall system safety.
- Control over Threshold Voltage: The thickness and doping concentration of the p-GaN layer provide a degree of control over the threshold voltage, allowing for device optimization.

CHAPTER 7: PACKAGING AND DESIGN INTEGRATION

7.1 Introduction to Chip on Board

Chip-on-Board (COB) is an advanced electronic packaging technique where a bare semiconductor die is directly mounted and wire-bonded onto a printed circuit board (PCB). The connections are then encapsulated with epoxy for protection.

7.2 Key features

- Direct bonding: The silicon chip is placed directly on the substrate, eliminating traditional packaging.
- Wire bonding: Tiny gold or aluminum wires connect the chip to the PCB traces.
- Encapsulation: An epoxy resin is applied over the chip and bonds to protect from moisture, dust, and mechanical damage.
- Compact size: Reduces overall dimensions, suitable for miniaturized electronics.
- Better thermal management: Heat spreads efficiently due to direct contact with the board.
- Cost-effective: Fewer packaging steps compared to traditional ICs.
- High performance: Shorter interconnects reduce signal loss and inductance.

7.3 GDS File: The blueprint for making chips

GDS file (specifically, GDSII) is exactly the master blueprint for manufacturing a chip. It's used by chip designers and chip factories (foundries) about details of an IC's physical layout, universally.

A GDS file is a binary file format. This format is specifically designed to store all the information needed to build an Integrated Circuit.

Key Characteristics:

1. Binary Format (Efficient Blueprint) makes them extremely efficient for storing vast amounts of complex geometric data and for quickly transferring that information

between different software programs and manufacturing equipment. If it were text, the files would be enormous and slow to process.

2. Hierarchical Structure: Repeating patterns or circuits (like memory cells or logic gates) are defined once and then referenced multiple times. This makes the file size much smaller and the design process more manageable.

3. Industry Standard for IC Layouts (Universal Language):

- GDSII has been the undisputed standard for exchanging IC layout data for decades. This is crucial because different companies use different design software (EDA tools), and chips are often manufactured by specialized foundries.
- The GDS format acts as a universal format that ensures everyone involved in the chip design and manufacturing process can understand and correctly interpret the layout information, regardless of the specific tools they use.

A GDS file contains all the components for building a chip layer by layer:

- Layers: Chips are built up in many thin layers of different materials (conductors, insulators, semiconductors). The GDS file precisely defines what material goes where on each layer.
- Geometric Shapes: This is the bulk of the data. It includes the exact shapes, sizes, and positions of all the features – transistors, wires, pads, etc. using polygons, rectangles, paths, and other geometric primitives.
- Text Labels: Sometimes, labels are included for identification, debugging, or documentation purposes within the layout.
- Other Relevant Data: This might include information about the design's origin, creation date, or specific processing instructions.

The GDS file sits at a critical juncture in the entire chip creation process:

1. Design Creation:

- IC designers use sophisticated Electronic Design Automation (EDA) tools (like Cadence Virtuoso, Synopsys Custom Compiler, or Mentor Graphics Calibre) to draw and arrange all the tiny components of the chip.
- This is where they define the transistors, connect them with metal wires, and arrange them into functional blocks.

- Once the design is complete and verified, it is saved as a GDS file. This GDS file is the ultimate output of the design phase.

2. Data Exchange:

- The GDS file then serves as the medium to transfer this intricate layout data.
- It can be sent to other EDA tools for further verification (e.g., checking for design rule violations or electrical issues).
- Most importantly, it's sent to the foundries (chip manufacturing plants) that will actually produce the physical silicon chip.

3. Mask Generation:

- Foundries receive the GDS file and use specialized equipment to translate its geometric data into a series of photomasks.

7.4 Our GaN chip

The figure illustrates the top view of a Gallium Nitride (GaN) power transistor die, designed for Chip-on-Board (COB) integration. The outermost square ($2.2\text{ mm} \times 1.9\text{ mm}$) represents the die boundary.

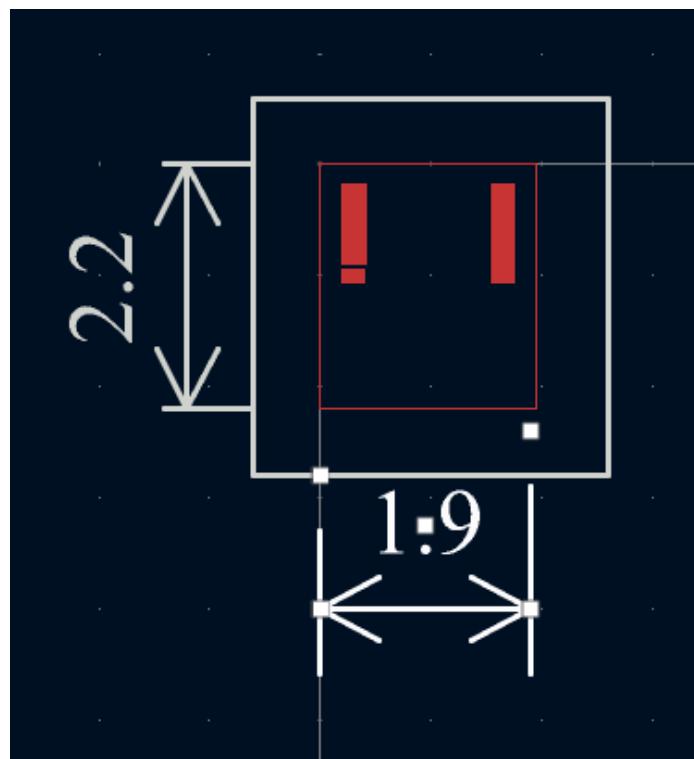


Figure 13 Top View of GaN Power Device Chip with Source, Gate, and Drain Layout

Inside this, the active regions are precisely defined as follows:

- **Drain Contact (Right):**

Positioned on the right-hand side, the drain region measures 0.21 mm × 0.72 mm, offering a wide area for high-current conduction and thermal dissipation.

- **Source Contact (Left-Top):**

The source pad is located on the top-left, with dimensions 0.21 mm × 0.882 mm. This region is elongated to support multiple parallel wire bonds for effective current handling and reduced resistance.

- **Gate Contact (Left-Bottom):**

Situated directly below the source pad, the gate measures 0.19 mm × 0.12 mm. Its smaller area is optimized for low gate capacitance and efficient switching behavior.

The central red box within the die boundary demarcates the active bonding area, reserved for fine-wire interconnects.

This compact and symmetric layout ensures:

- Efficient lateral current flow
- Minimal parasitic inductance
- Thermal spreading over the die area

Such a layout is ideal for high-efficiency, high-frequency GaN power applications.

7.5 GBR File: The blueprint for making circuit boards

A Gerber file (often simply called a GBR file) is the master blueprint for manufacturing a Printed Circuit Board (PCB).

A Gerber file is a digital file format that contains all the precise instructions for manufacturing each individual layer of a PCB. It's the language that PCB designers use to communicate their design to PCB manufacturers.

Key Characteristics:

1. ASCII Vector Format: The Gerber files are typically ASCII text files. They use vector graphics, meaning they describe shapes (like lines, circles, and polygons) using mathematical points and commands, rather than pixels. This ensures high precision and scalability. While human-readable, it's still complex. You'd typically use special Gerber viewer software to see the actual visual representation of the PCB layer, rather than just raw text.

2. Layer-Specific: For every unique layer of PCB design, there is a separate Gerber file. For a common two-layer PCB, there are many files for layers like:

- One Gerber file - top copper layer (traces, pads)
- One Gerber file - bottom copper layer.
- One Gerber file - top solder mask
- One Gerber file - bottom solder mask.
- One Gerber file - top silkscreen (text, symbols)
- One Gerber file - bottom silkscreen
- A separate drill file, which complements the Gerber files by specifying all the holes

3. De Facto Standard for PCBs (Universal Language):

- Gerber is the universal standard for PCB manufacturing data exchange. This ensures that no matter what PCB design software (like Altium Designer, KiCad, Eagle, Cadence Allegro) a designer uses, and no matter which PCB factory (fabrication house) builds the board, they can all understand each other's files and accurately produce the board. Each Gerber file defines specific elements of a PCB layer:

- Copper layers: These files define the exact pathways for electrical signals (traces), the areas where components are soldered (pads), and large areas of copper for grounding or power distribution.
- Solder mask layers: These define the areas that will not be covered by a solder mask. This is usually where component pads are exposed so they can be soldered.
- Silkscreen layers: These files contain all the non-electrical markings.

- Board outline: This file defines the precise physical shape of the PCB, including any cutouts, slots, or non-rectangular edges
- Drill File (usually Excellon): Although not a Gerber file itself, this file is always included in the Gerber package. It specifies the precise location, size, and type (plated through-hole for components, non-plated for mounting screws) of every single drill hole on the board.

The Gerber files are at the heart of the PCB manufacturing process:

1. Design Export: A PCB designer uses their Electronic Design Automation (EDA) or Computer-Aided Design (CAD) software to lay out the PCB. This involves placing components, routing traces, defining layers, etc. Once the design is finalized and checked for errors, the software exports each individual layer of the design into its corresponding Gerber file (along with the drill file).
2. Data Package for Fabrication: The designer then bundles all these Gerber files and the drill file into a complete manufacturing data package. This package is then sent directly to a PCB fabrication house.
3. Manufacturing Instructions (The Factory's Guide):
 - At the factory, engineers load these Gerber files into their Computer-Aided Manufacturing (CAM) systems. These systems are essentially software programs that translate the Gerber data into instructions for automated machinery:
 - Photoplotters or Direct Imagers: These machines use the Gerber data for copper layers to precisely create the patterns of traces and pads. They either draw on photographic film to create masks or directly expose light-sensitive material on the copper-clad board panels.
 - Drilling Machines: These highly accurate robotic drills use the Excellon drill file to drill all the necessary holes in the correct locations and sizes.
 - Solder Mask and Silkscreen Printers: These machines use the respective Gerber files to apply the protective solder mask and the informational silkscreen text onto the board.

4. Quality Control and Verification:

- Gerber files are also vital for quality control. Automated Optical Inspection (AOI) machines use the Gerber data as a reference to optically scan the manufactured boards and compare them against the original design, ensuring there are no defects or deviations.
- Both designers and manufacturers use Gerber viewer software to visually inspect each layer, ensuring that everything looks correct before and during production.

CHAPTER 8: PCB DESIGN CONSIDERATIONS

8.1 Copper thickness

In the Printed Circuit Board (PCB) industry, unlike typical thickness measurements in millimeters or inches, copper thickness is most commonly expressed using a unit of weight: ounces (oz)

When 1 ounce (oz) of copper (which weighs approximately 28.35 grams) is rolled out to completely cover an area of 1 square foot (ft^2) (which is 0.0929 square meters), the resulting thickness of that copper foil is precisely defined.

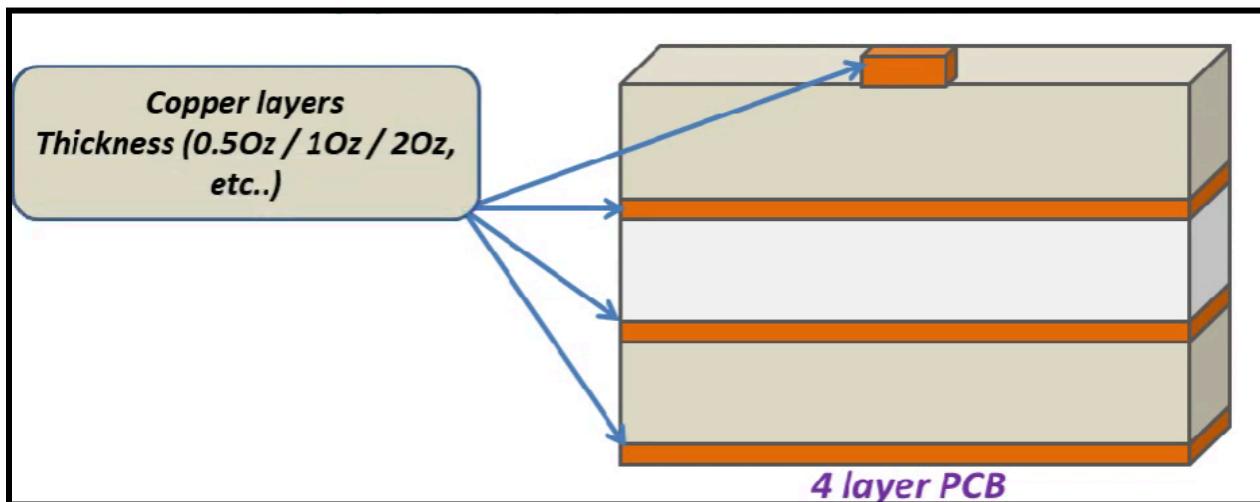


Figure 14 Thickness of Copper in oz/ft^2

$$1 \text{ oz}/\text{ft}^2 \approx 1.37 \text{ mils} \approx 0.035 \text{ mm}$$

1. Heavier copper (e.g., 2 oz, 3 oz, or more) allows for the flow of higher electrical currents without experiencing excessive temperature rise as thicker copper offers less resistance for the same cross-sectional area of a trace. Alternatively, for a given current requirement, using heavier copper allows designers to use narrower traces while still maintaining acceptable temperature limits. This can be advantageous for creating more compact PCB designs.
2. Heavier copper can also contribute to the mechanical robustness of the PCB, especially for larger boards or those subjected to vibrations.
3. While advantageous for electrical performance, heavier copper can negatively affect etching precision. The etching process removes unwanted copper. When the

copper is thicker, it becomes more challenging to etch very fine lines and spaces accurately without over-etching or under-etching. This is because the etchant can undercut the resist, leading to narrower traces than designed, or it might struggle to fully remove copper from tight spaces.

4. Impact on Design Rules: This means that PCBs with heavier copper typically require larger minimum trace widths and larger minimum spacing between traces compared to boards with standard 1 oz or 0.5 oz copper. Achieving very fine features becomes more difficult and costly with thicker copper

Common Copper Thicknesses:

- 0.5 oz (0.0175 mm): Used for very fine line applications where signal integrity and high density are paramount, and current is low.
- 1 oz (0.035 mm): The most common and standard copper thickness for general-purpose PCBs, offering a good balance of current carrying capacity and manufacturability.
- 2 oz (0.070 mm): Used for moderate power applications where higher current handling is needed, but still allowing for relatively good feature sizes.
- 3 oz and above (0.105 mm+): Reserved for high-power applications, power planes, and robust industrial boards, where large currents and enhanced thermal performance are critical. These boards will have significantly relaxed design rules for traces and spaces.

8.2 Trace width

Trace width, a critical parameter in Printed Circuit Board (PCB) design, refers to the physical width of a copper conductor that carries electrical current. Its significance lies in its direct impact on the PCB's ability to safely and efficiently transmit power without compromising the integrity of the circuit or the board itself.

$$1 \text{ mil} = 0.001 \text{ inches} = 0.025 \text{ mm}$$

The appropriate trace width is determined by a complex interplay of several factors, primarily current capacity, copper thickness, and the permissible temperature rise.

If a trace is too narrow for the current it carries, it can overheat, leading to potential damage to components, board delamination, or even fire.

Factors Influencing Trace Width and Current Relationship:

The relationship between trace width and the current it can safely carry is not linear and is influenced by a multitude of design and environmental factors. A thorough understanding of these factors is essential for any PCB designer to ensure reliable and long-lasting electronic products.

1. Current Carrying Capacity: This is the most fundamental factor. A wider trace offers a larger cross-sectional area for current flow, thereby reducing its electrical resistance. According to Ohm's Law ($V=IR$) and Joule's Law ($P=I^2R$), a lower resistance for a given current results in less power dissipated as heat. Therefore, to carry higher currents, a broader trace is required to prevent excessive heat generation. While a broader track can be made more "bulky" (in terms of copper volume), this increased bulk directly contributes to its ability to handle higher current loads without overheating.

2. Temperature Rise : Every trace, due to its inherent resistance, will generate some heat when current flows through it. The "temperature rise" refers to the increase in the trace's temperature above the ambient temperature. This rise must be kept within acceptable limits, as excessive temperatures can degrade component performance, shorten their lifespan, or even lead to catastrophic failure. High temperatures can cause solder joints to weaken, insulation materials to break down, and the PCB substrate itself to delaminate. The maximum allowable temperature rise is often specified by design standards or component manufacturers.

3. Copper Thickness: The thickness of the copper layer used for the traces is a crucial determinant of current capacity. Thicker copper traces inherently possess a larger cross-sectional area for a given width, leading to lower resistance and thus greater current-carrying capability. Standard copper thicknesses on PCBs range from 0.5 oz/ft² to 2 oz/ft² or even higher for power applications. A copper trace layer with

greater thickness is preferable as it offers better conductivity and can withstand higher current loads for the same width.

4. Trace Length: Longer traces, by their very nature, have a greater total resistance compared to shorter ones of the same width and thickness. This increased resistance in longer traces means that for a given current, more heat will be generated along their length. Therefore, for long traces carrying significant currents, designers might need to slightly increase the trace width to compensate for the cumulative resistance and prevent localized hotspots. Speaking of traces, the longer they are, the more they act like "official resistors" and can even generate considerable heat.

5. Ambient Temperature: The surrounding environmental temperature (ambient temperature) directly impacts the thermal performance of the PCB. If the ambient temperature is already high, the trace has a smaller temperature differential available to dissipate the heat it generates before reaching its maximum allowable operating temperature. The thermodynamic performance of the structure decrements due to high temperature surrounding it, leading to reduced heat dissipation capabilities. Consequently, the structure might not be able to thermalize efficiently, requiring wider traces for the same current capacity in hotter environments.

6. Layer Placement: The location of a trace within the PCB stack-up significantly affects its ability to dissipate heat. Outer layers (top and bottom) have better access to the surrounding air and can radiate heat more effectively. Conversely, inner layers are sandwiched between other layers of insulating material, making heat dissipation more challenging. Heat loss dissipates faster from outward surfaces than from inner areas. Therefore, a trace on an inner layer will generally require a wider dimension to carry the same current as an equivalently sized trace on an outer layer, assuming the same temperature rise limit.

Trace Width Formula:

Trace width is calculated as:

$$W = \frac{I}{k \cdot (\Delta T)^{0.44}} \cdot \left(\frac{t}{1 \text{ oz/ft}^2} \right)^{0.725}$$

Where I = current that can pass through it

ΔT = increase in temperature in ($^{\circ}\text{C}$)

t = thickness of copper traces 2 oz/ ft^2

Constant K = 0.048 (external layer)

0.024 (internal layer)

Current in A	Trace Width for 2 oz/ ft^2 (mils)
0.5	6
1	12
2	24
3	36
5	60
10	120
15	180
20	240
30	360
40	480

Table 1 Trace width table

- For I = 10A and $\Delta T = 10^{\circ}\text{C}$

$$W = 120 \text{ mil} = 3.048 \text{ mm}$$

- For I = 20A and $\Delta T = 10^{\circ}\text{C}$

$$W = 240 \text{ mil} = 6.096 \text{ mm}$$

8.3 Trace spacing

Trace spacing refers to the critical distance maintained between two adjacent copper traces on a Printed Circuit Board (PCB). This parameter influences the board's electrical performance, manufacturability, reliability, and even its safety. Spacing is typically measured in mils (thousandths of an inch) or millimeters (mm).

The adherence to proper trace spacing design rules is paramount in electronic circuit design due to its wide-ranging effects:

1. Electrical Isolation & Safety: If traces are placed too close together, especially when carrying high voltages, the insulating material (dielectric) between them can break down. This can lead to an electrical short circuit, or worse, arcing.
2. Signal Integrity: When two signal traces run parallel and too close to each other, the electromagnetic field of one trace can induce unwanted signals (noise) onto the adjacent trace. This phenomenon is called crosstalk. Adequate spacing effectively reduces this electromagnetic coupling, thereby minimizing interference between signals and preserving the integrity and quality of the intended signals.
3. Impedance Control: For high-frequency signals, PCB traces behave as transmission lines. The characteristic impedance of these lines must be carefully controlled to prevent signal reflections and ensure maximum power transfer. By precisely following trace spacing design rules, designers can achieve the desired impedance, ensuring optimal signal quality and minimizing reflections that can distort signals.
4. Manufacturing Reliability: PCB fabrication involves chemical etching, plating, and other precise processes. These processes have inherent capabilities and tolerances. If traces are designed too close, it pushes the limits of manufacturing. Design rules for trace spacing take these manufacturing capabilities into account. Following these guidelines significantly increases the likelihood of the precise and dependable manufacture of the PCB, thereby decreasing the possibility of common manufacturing defects like short circuits (due to incomplete etching) or open circuits (due to over-etching).

5. **EMI/EMC Compliance:** Closely spaced traces, particularly those carrying high-frequency signals, can act as unintended antennas, radiating electromagnetic energy and causing electromagnetic interference (EMI) to other electronic devices. Electromagnetic Compatibility (EMC) ensures that the electronic device functions as intended in its electromagnetic environment without generating or being susceptible to excessive interference.
6. **Heat Dissipation:** Spacing allows for better airflow or better thermal pathways to spread heat across the board, preventing localized hot spots and ensuring the reliability and longevity of the circuit and its components.
7. **Design for Manufacturing (DFM):** Trace spacing rules are a cornerstone of Design for Manufacturing (DFM). By adhering to DFM guidelines, designers ensure that the PCB can be reliably and cost-effectively produced by a chosen fabricator. Reducing the chances of short circuits, opens, or other manufacturing-related issues due to insufficient spacing directly translates to higher manufacturing yields and lower production costs.
8. **Design for Testability (DFT):** Sufficient trace spacing provides enough room for test probes to contact specific points on the PCB without accidentally shorting adjacent traces. This is vital during the manufacturing (In-Circuit Testing) and debugging stages.
9. **Design for Serviceability:** Adequate spacing between traces and components makes it easier for technicians to access, desolder, replace, or repair components on the PCB if needed. This enhances the overall serviceability and maintenance of the circuit, extending its useful life.
10. **Design Consistency:** Following established trace spacing design rules ensures a level of consistency in PCB layout across different projects or within large design teams.

Trace Spacing calculation

Voltage Between Conductors	B1 Internal Conductors	B2 External, uncoated ($\leq 3050\text{m}$)	B3 External, uncoated ($> 3050\text{m}$)	B4 External, with polymer coating	A5 Conformal coating (assembly)	A6 Uncoated termination (assembly $\leq 3050\text{m}$)	A7 Conformal coating termination
0–15 V	0.05 mm	0.1 mm	0.1 mm	0.05 mm	0.13 mm	0.13 mm	0.13 mm
16–30 V	0.05 mm	0.1 mm	0.1 mm	0.05 mm	0.13 mm	0.13 mm	0.13 mm
31–50 V	0.1 mm	0.13 mm	0.4 mm	0.13 mm	0.13 mm	0.13 mm	0.13 mm
51–100 V	0.2 mm	0.25 mm	0.6 mm	0.13 mm	0.13 mm	0.13 mm	0.13 mm
101–150 V	0.3 mm	0.5 mm	1.5 mm	0.2 mm	0.4 mm	0.4 mm	0.4 mm
151–170 V	0.4 mm	0.6 mm	1.8 mm	0.25 mm	0.4 mm	0.4 mm	0.4 mm
171–250 V	0.7 mm	1.25 mm	3.2 mm	0.4 mm	0.4 mm	0.4 mm	0.4 mm
251–300 V	1.2 mm	2.29 mm	5.1 mm	0.8 mm	0.8 mm	0.8 mm	0.8 mm
301–500 V	2.0 mm	2.58 mm	6.4 mm	1.25 mm	1.25 mm	1.25 mm	1.25 mm
>500 V	0.025 mm/volt	0.025 mm/volt	0.05 mm/volt	0.025 mm/volt	0.00305 mm/volt	0.00305 mm/volt	0.00305 mm/volt

Table 2 Trace spacing table

We chose B4: External Conductors with permanent polymer coating (any elevation) as our design includes coated external traces.

For voltage as high as 1000V, the required trace spacing is calculated as:

$$0.00305 \text{ mm/Volt} \times 1000 \text{ V} = 3.05 \text{ mm}$$

8.4 Wire bonds

Wire bonding is a method of making interconnections between a semiconductor die and its package or between two substrates using very fine wires. It is the most

common and cost-effective method used in microelectronics packaging.

Key Features:

- Types of wire materials: Gold (Au), Aluminum (Al), Copper (Cu)
- Typical wire diameters: Ranges from 15 μm to 75 μm (0.6–3 mils)
- Bonding methods:
 - Thermosonic bonding (for gold)
 - Ultrasonic bonding (for aluminum)
 - Thermocompression bonding (rare)

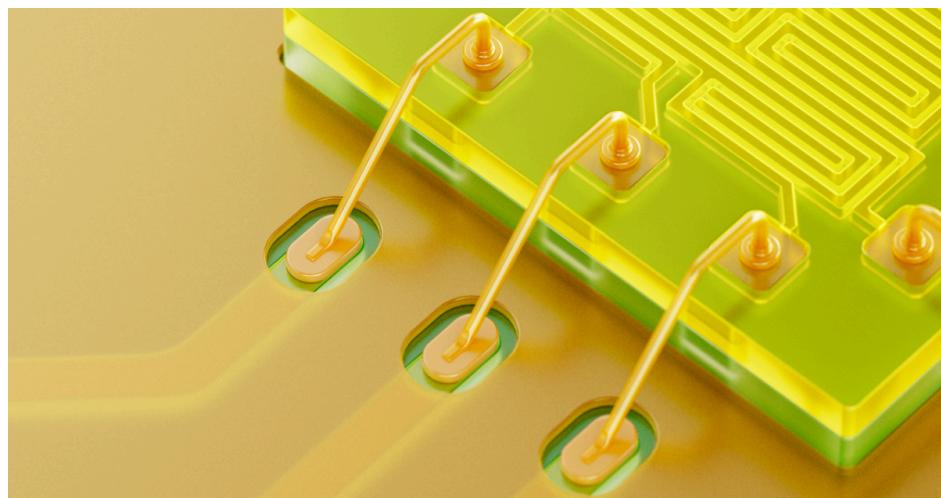


Figure 15 Wire bonds

Wire bonds also play a critical role in current conduction, signal transmission, and thermal management, especially in high-power modules where multiple parallel wire bonds are used to share the load current.

In our design, we are using 1 mil (25.4 μm) diameter Aluminum wire bonds. Aluminum is commonly chosen due to its excellent electrical conductivity, low cost, and compatibility with ultrasonic bonding techniques. Aluminum wire bonding is especially preferred in power electronics, where high current capacity is required, and the bonding environment allows for oxide layer formation to be managed.

The maximum current handling capability of a single 1 mil aluminum wire is

approximately 500 mA. This limit is determined by the wire's resistance, allowable temperature rise, and electromigration threshold.

For a total current of 10 A, we perform the following calculation:

- Max current per wire bond = 0.5 A
- Total current = 10 A
- Minimum number of wire bonds required = 20

Thus, to safely conduct 10 A, we must use at least 20 parallel 1 mil Al wire bonds. In practical applications, an additional safety margin (e.g., 10–20%) is often added to account for variation in bond resistance and thermal conditions.

8.5 Electromigration in Copper

Electromigration is a degradation mechanism in conductive materials, particularly copper traces on a Printed Circuit Board (PCB), where the flow of electrons itself causes a physical movement of metal atoms. It's essentially the mass transport of metal atoms driven by the "electron wind".

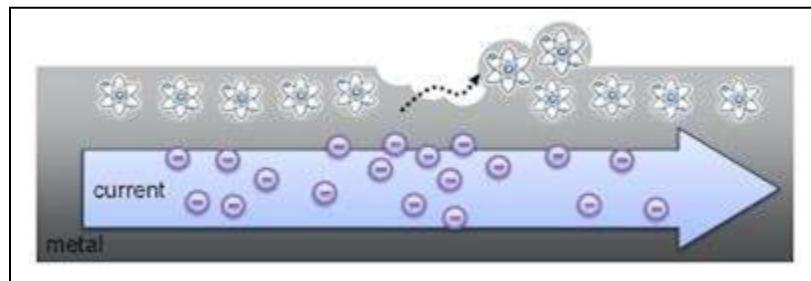


Figure 16 Electromigration in Copper

When the current density becomes sufficiently high, these electron collisions impart enough force on the metal atoms to dislodge them from their lattice positions.

This atomic movement doesn't happen uniformly. Instead, it leads to:

- Material thinning: Atoms are pushed away from certain areas, creating vacancies or voids in the trace, effectively thinning the conductor. This thinning often occurs "upstream" in the direction of electron flow.

- Build-up elsewhere: The dislodged atoms then accumulate "downstream" in other areas, forming tiny bumps or growths called hillocks.

Over time, with continued electromigration, these physical changes can lead to catastrophic failures:

- Open circuits: Severe line thinning can eventually lead to a complete break in the trace, causing an open circuit and stopping current flow.
- Short circuits: Conversely, if electromigration is large enough, it can bridge the gap between adjacent traces, leading to an unwanted short circuit.

Electromigration is particularly critical and a significant concern in:

- Fine copper traces: Where the cross-sectional area is small, leading to higher current densities for even moderate currents.
- Narrow vias: Vias also represent constricted conductive paths where current density can become very high.
- High-current paths: As the name suggests, any part of the board designed to carry substantial current is susceptible.

These conditions are frequently encountered in modern electronics, especially in

- Chip-on-Board (COB) technology: Where unpackaged ICs are directly mounted and wire-bonded to a PCB, leading to very fine interconnections.
- Power electronics: Which inherently deals with high currents and power dissipation.

8.6 Electroless Nickel Immersion Gold

An Electroless Nickel Immersion Gold (ENIG) surface finish is often employed.

Composition:

- Electroless Nickel Layer: This is the primary functional layer, deposited directly onto the copper. It provides a hard, robust and highly solderable surface. Crucially, it acts as an effective diffusion barrier, preventing the underlying copper from migrating into the solder joint, which helps to prevent electromigration.
- Immersion Gold Layer: A very thin layer of gold is deposited on top of the nickel. Its main purpose is to protect the nickel from oxidation prior to soldering,

ensuring its solderability over time. This gold layer also helps in preventing copper exposure, further contributing to reduced surface electromigration effects.

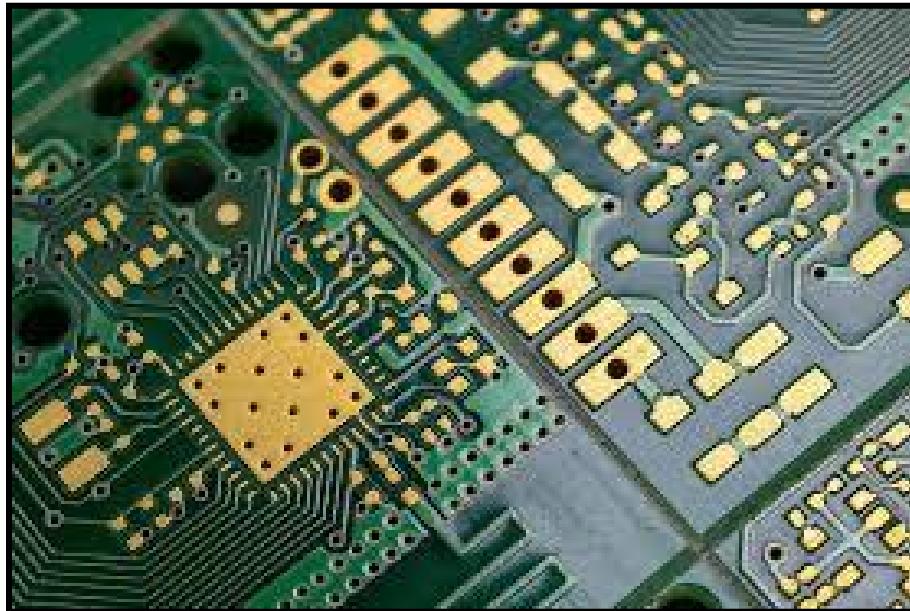


Figure 17 ENIG layer

Key Benefits:

- Electromigration Resistance: The nickel barrier is key to preventing copper atom movement, especially in high-current density areas like fine traces and vias.
- Corrosion Resistance: Inside vias and on pads, the ENIG finish significantly improves resistance to corrosion and current-induced damage.
- Stable Contact Resistance: It helps maintain consistent and low electrical contact resistance, vital for reliable performance in high-frequency or high-current applications.
- Flat and Smooth Surface: ENIG provides an exceptionally flat and smooth surface, which is critical for fine-pitch component assembly (like BGAs) and ensures consistent solder joint quality.
- Excellent Shelf Life: Boards with ENIG finish have a long storage life without degradation of solderability.
- Lead-Free Compliance: It's fully compatible with lead-free soldering

processes, meeting modern environmental regulations.

8.7 CoBs designed

The figure shows a $20.5\text{ mm} \times 22.2\text{ mm}$ Chip-on-Board (COB) layout intended for the integration of a GaN power die in OrCAD. The layout follows a two-layer PCB configuration, with the top copper layer (blue) carrying all major signal and power paths.

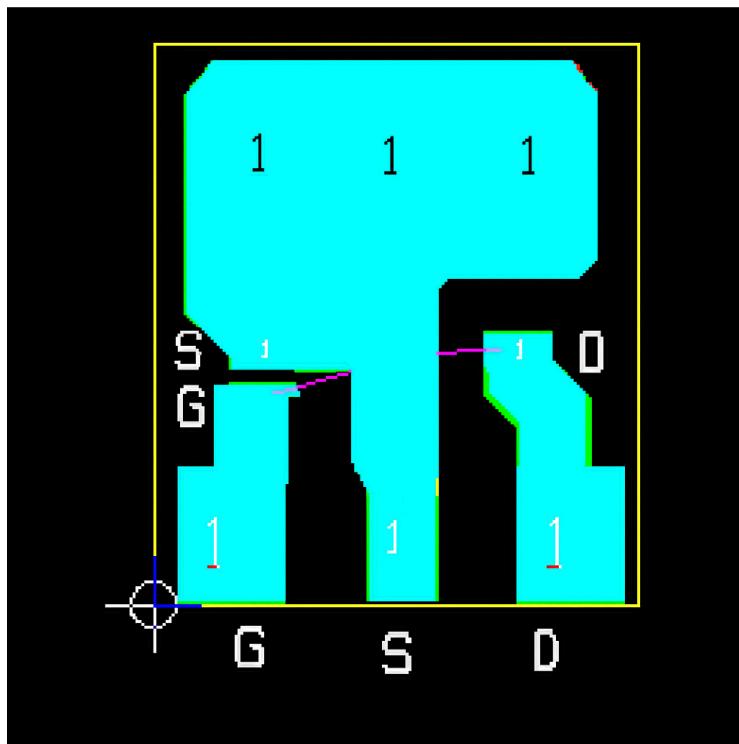


Figure 18 Two-Layer COB Layout for GaN Die

A corresponding bottom copper layer (not shown) supports current flow and aids in heat dissipation through plated through holes (PTHs). The design includes three clearly labeled copper pads:

- **G (Gate)** – positioned at the left, connected to the control signal
- **S (Source)** – centrally located, providing a large pad area for die attach and current return
- **D (Drain)** – on the right, forming the high-current output path

The pink outline traces indicate wire bonds for electrical connectivity and

boundaries within the design.

Trace spacing is maintained at a minimum of 3.05 mm, ensuring adequate clearance for high-voltage operation and improved electrical isolation.

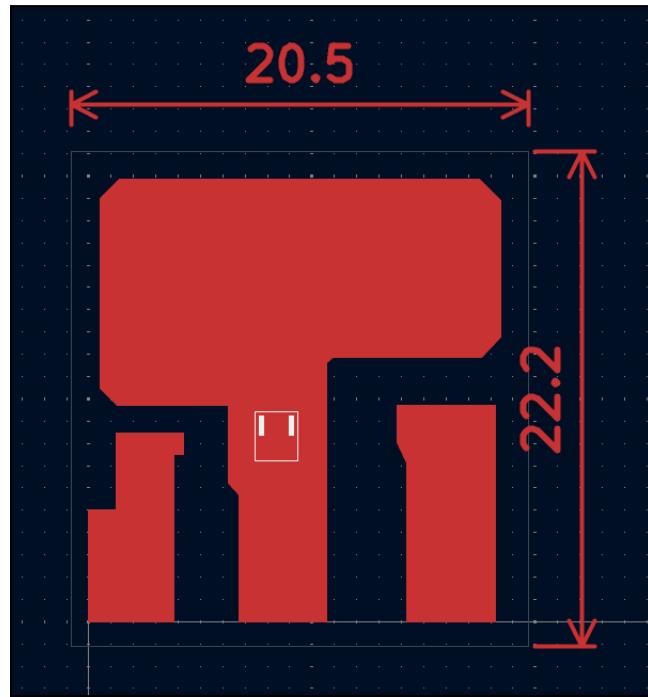


Figure 19 Two-Layer COB Layout for GaN Die in 2D

Track widths for all terminals (Gate, Source, and Drain) are set to greater than 3 mm, enabling robust current handling and minimizing resistive losses.

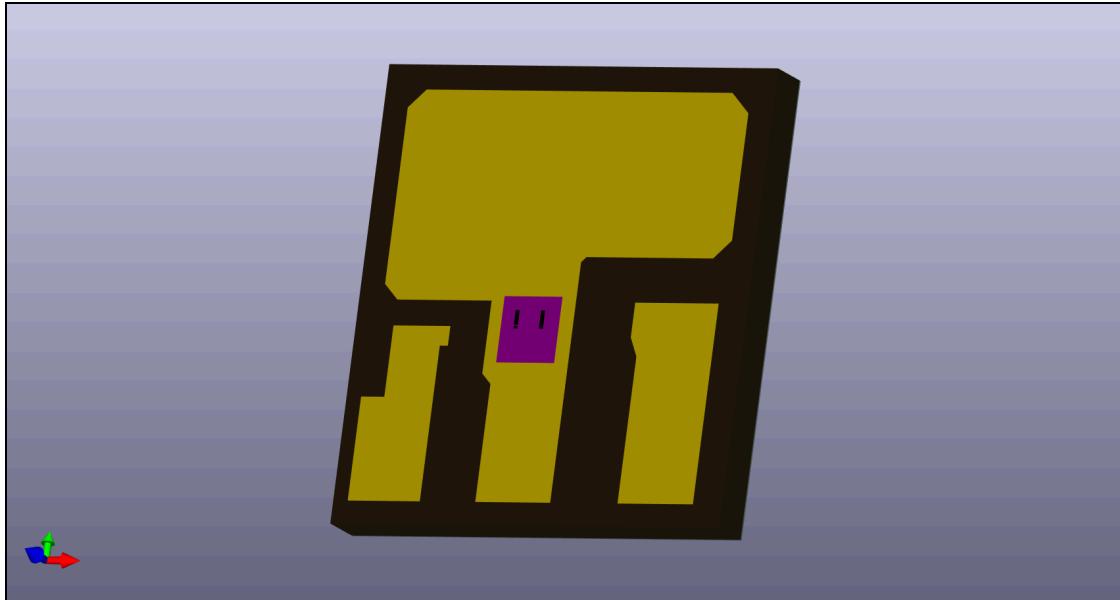


Figure 20 Two-Layer COB Layout for GaN Die in 3D

The geometry supports standard packaging alignment, allowing smooth placement of die and wire bonding or flip-chip attachment.

This COB layout is optimized for compact integration, low parasitic inductance, and enhanced thermal performance, making it well-suited for switching power converters, RF amplifiers, and other high-frequency GaN applications.

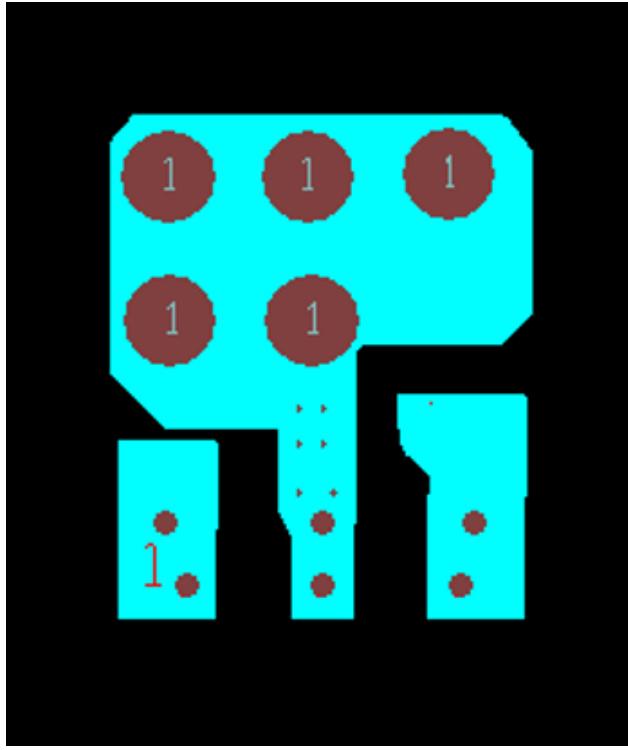


Figure 21 Top View of Two-Layer COB Layout for GaN Power Die Integration

This figure presents a Chip-on-Board (COB) layout created in OrCAD for integrating a GaN power die. The blue areas are the top copper layer, which carries high-current traces and signal paths. The bottom copper layer (not shown here) mirrors the top for enhanced electrical routing and acts as a thermal sink, forming a two-layer PCB optimized for power applications.

The layout includes a central die attach pad, positioned over a dense via array. These plated-through holes (PTHs) shown as grey circles facilitate both vertical electrical interconnection and thermal conduction from the top surface down to the bottom copper and the PCB substrate. This ensures effective heat dissipation during high-power operation.

The pad configuration is designed to match the TO-220 package footprint:

- Left pad – Gate
- Middle pad – Source (which also hosts the GaN die)
- Right pad – Drain

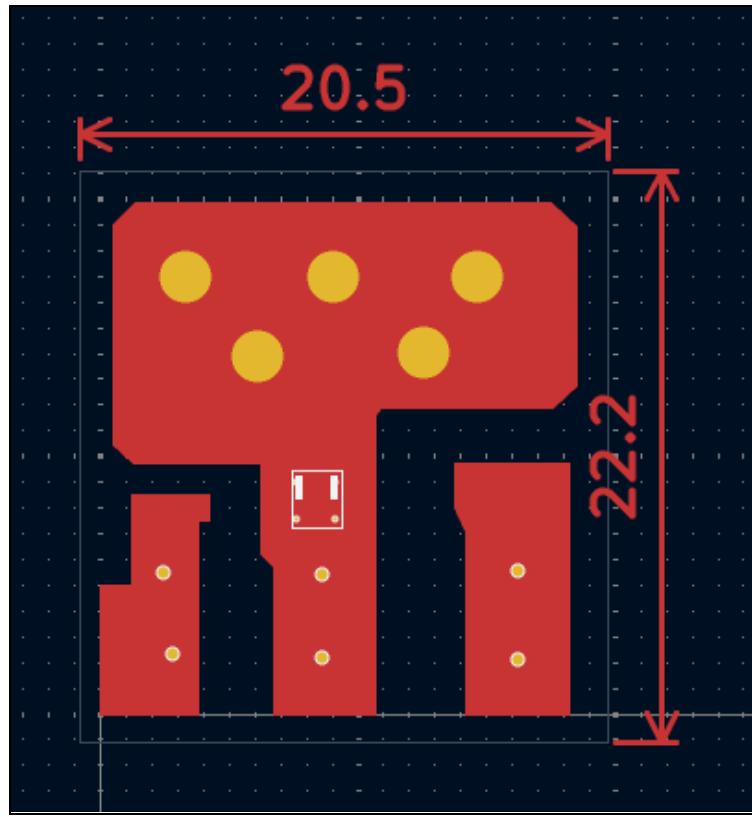


Figure 22 Top View of Two-Layer COB Layout for GaN Power Die Integration in 2D

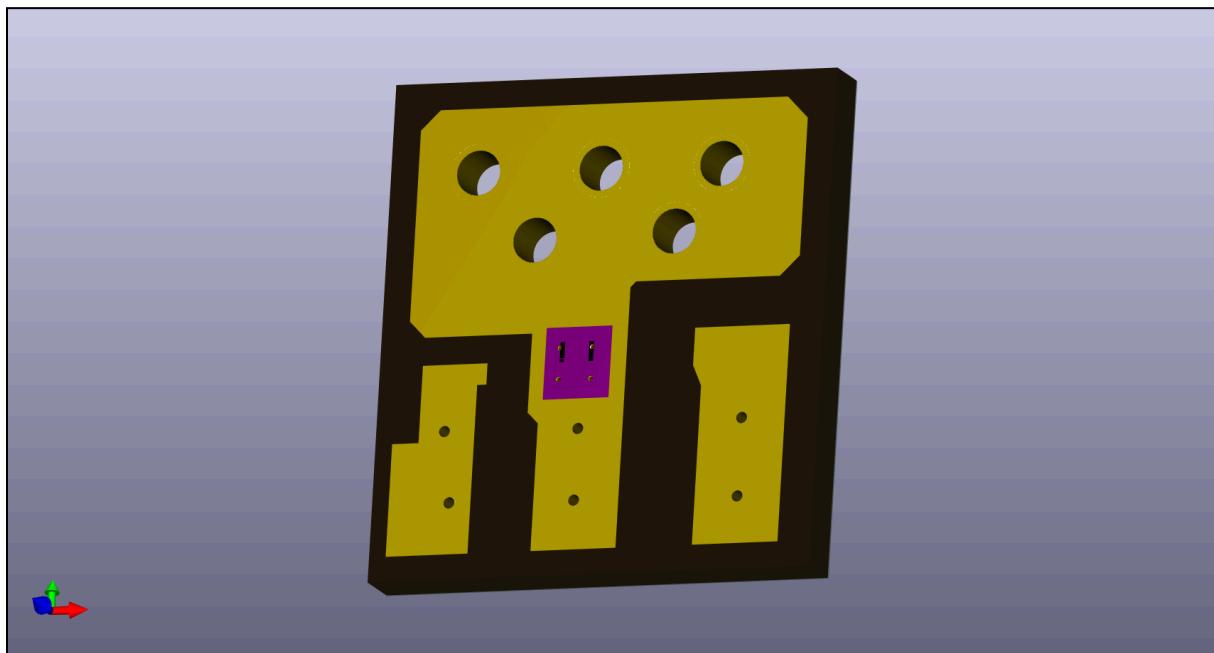


Figure 23 Top View of Two-Layer COB Layout for GaN Power Die Integration in 3D

The PTH spacing in the lower section is carefully maintained at 2.54 mm, matching the standard TO-220 lead pitch for direct pin soldering. The signal trace spacing is designed with a minimum clearance of 3.05 mm to prevent arcing or shorting under high voltage conditions, ensuring safe operation in power circuitry. Furthermore, all track widths are kept above 3 mm, providing sufficient current-carrying capacity and minimizing resistive losses.

The via system includes:

- Upper thermal vias: large, with 2.0 mm diameter, for bulk heat removal
- Standard PTHs: 0.5 mm diameter
- Fine vias: 0.3 mm diameter, used for additional thermal stitching below GaN die

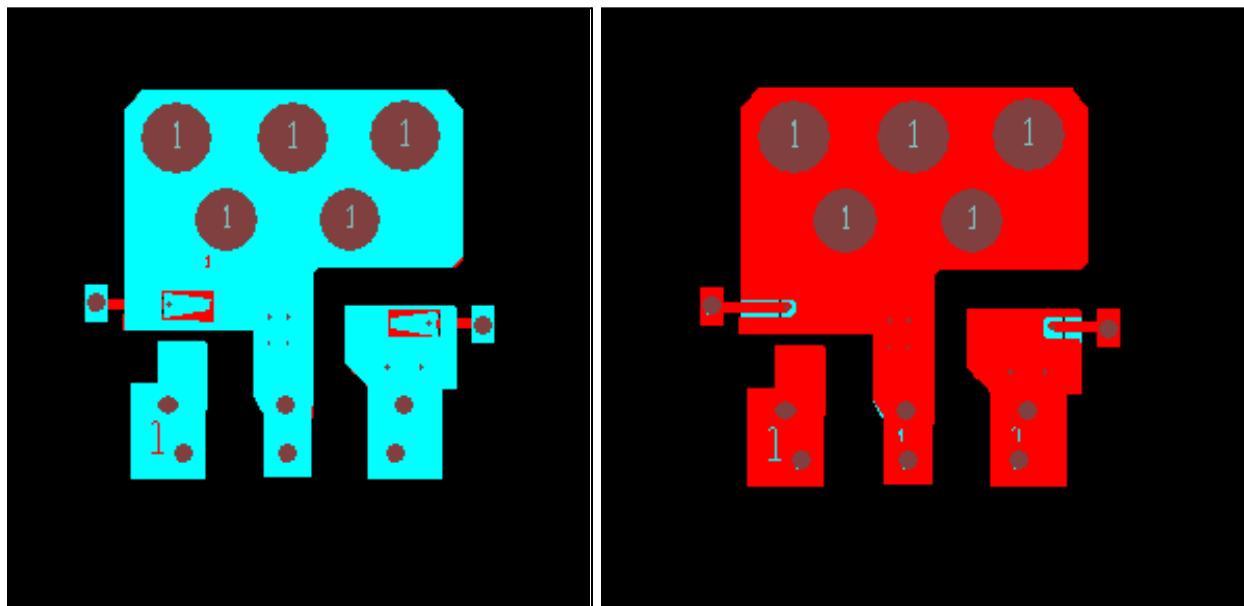


Figure 24 COB Layout with Integrated Force and Sense Pads for Accurate GaN Die Characterization

This layout builds upon the basic two-layer Chip-on-Board (COB) structure for a GaN power die by incorporating dedicated force and sense pads to enhance measurement accuracy during electrical characterization. The top copper layer

(shown in blue) contains the primary routing, while the bottom copper layer (shown in red) includes mirrored connections and additional pads used for 4-wire (Kelvin) measurements.

To support precise characterization:

- Two additional copper pads are introduced adjacent to the Source and Drain terminals.
- These are connected through vias to corresponding force and sense pads on the bottom layer, enabling external probe access or soldering for measurement equipment.
- The force pads carry the operating current, while the sense pads measure voltage directly at the die location, eliminating voltage drop errors caused by interconnect resistance.

This Kelvin connection strategy ensures:

- Improved accuracy during on-resistance ($R_{DS(on)}$) and threshold voltage measurements
- Elimination of parasitic errors introduced by trace or contact resistance

The rest of the design retains critical features from the previous COB model:

- Thermal vias (2 mm, 0.5 mm, and 0.3 mm diameters) for effective heat transfer
- TO-220 compatible 2.54 mm pin spacing
- Track spacing of 3.05 mm minimum and trace widths >3 mm for safe high-current operation.

This enhanced structure provides both power integration and precise characterization capability, making it suitable for lab testing, reliability validation, and accurate parameter extraction of GaN power devices.

CHAPTER 9: KEY CHALLENGES IN HIGH CURRENT PCB DESIGN

9.1 High heat in PCBs

Designing Printed Circuit Boards (PCBs) for high-current applications introduces several critical challenges:

1. Excess Heat and Electrostatic Energy: High currents inherently generate significant excess heat due to power dissipation. This heat can lead to component degradation, reduced lifespan, and even board damage. High currents can also lead to the accumulation of electrostatic energy, increasing the risk of electrostatic discharge (ESD) related failures if not properly managed.

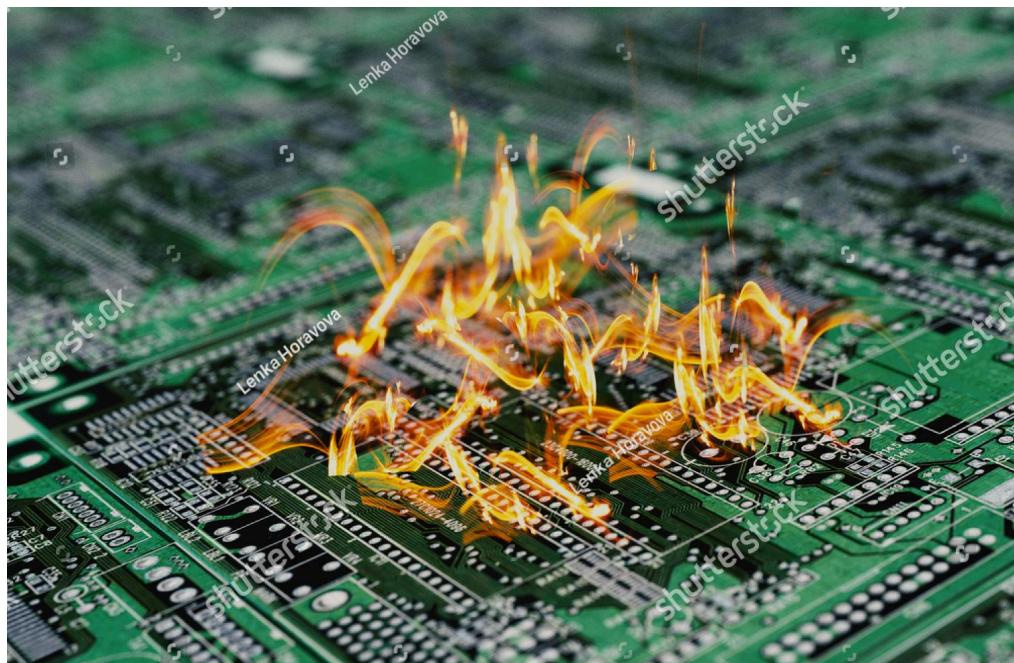


Figure 25 High heat in high current PCBs

2. Trace Damage: If PCB traces are not wide and thick enough for the current they carry, their electrical resistance (R) will be too high. The resulting heat (I^2R) can cause the copper trace to literally burn out or melt, leading to an open circuit. Thus, thick and wide traces (or copper pours/planes) are absolutely essential for high-current paths, ensuring sufficient metal to safely conduct the current without

overheating or damage.

3. Low Inductance Requirement: Maintaining low inductance in the power delivery network (PDN) is crucial, especially in high-speed or high-current switching applications. High inductance can cause voltage spikes (ground bounce, V_{cc} droop) during rapid current changes, disrupting circuit operation and damaging components.

4. Thermal Management: PCBs are made of materials like FR-4, which have a specific glass transition temperature (130°C for standard FR-4). Above this temperature, the material loses its structural stability, softens, and can even start to melt or delaminate.

5. Electromagnetic Interference (EMI): High-current paths, particularly those with rapidly changing currents (e.g., switching power supplies), act as efficient antennas, generating strong electromagnetic interference (EMI). This radiated noise can couple into nearby sensitive circuits, causing signal integrity issues, false triggers, or data corruption. Thus, proper shielding, careful routing strategies (e.g., minimizing loop areas, differential routing), and appropriate filtering are required to minimize EMI effects and ensure the PCB complies with electromagnetic compatibility (EMC) standards.

9.2 Thermal simulation of CoB

To evaluate the thermal performance of the Chip-on-Board (COB) layouts, thermal convection analysis was carried out using SimScale, a cloud-based multiphysics simulation platform. SimScale was selected due to its accessibility, robust thermal solver, and ease of integration with standard CAD tools such as KiCad.

The analysis modeled natural convection with ambient temperature set at 22°C, and convection boundaries were applied to both the top and bottom surfaces of the PCB. The heat source was defined at the die attach region to simulate self-heating of the GaN device under typical operating conditions.

A volumetric heat flux of $5.9 \times 10^9 \text{ W/m}^3$ was applied to the die area. This value corresponds to a current load of 10 A flowing through a small GaN device footprint, resulting in high localized power density. The analysis helped visualize the temperature gradient across the PCB and assess how effectively each layout with and without thermal vias dissipates heat under these conditions.

SimScale's finite element solver enabled real-time visualization of temperature rise, allowed comparison between configurations, and provided insight into how design modifications (e.g., via placement and density) impact the thermal path and equilibrium temperature. This data was critical in confirming the effectiveness of thermal vias in reducing junction temperature and improving thermal performance in power-dense GaN applications.

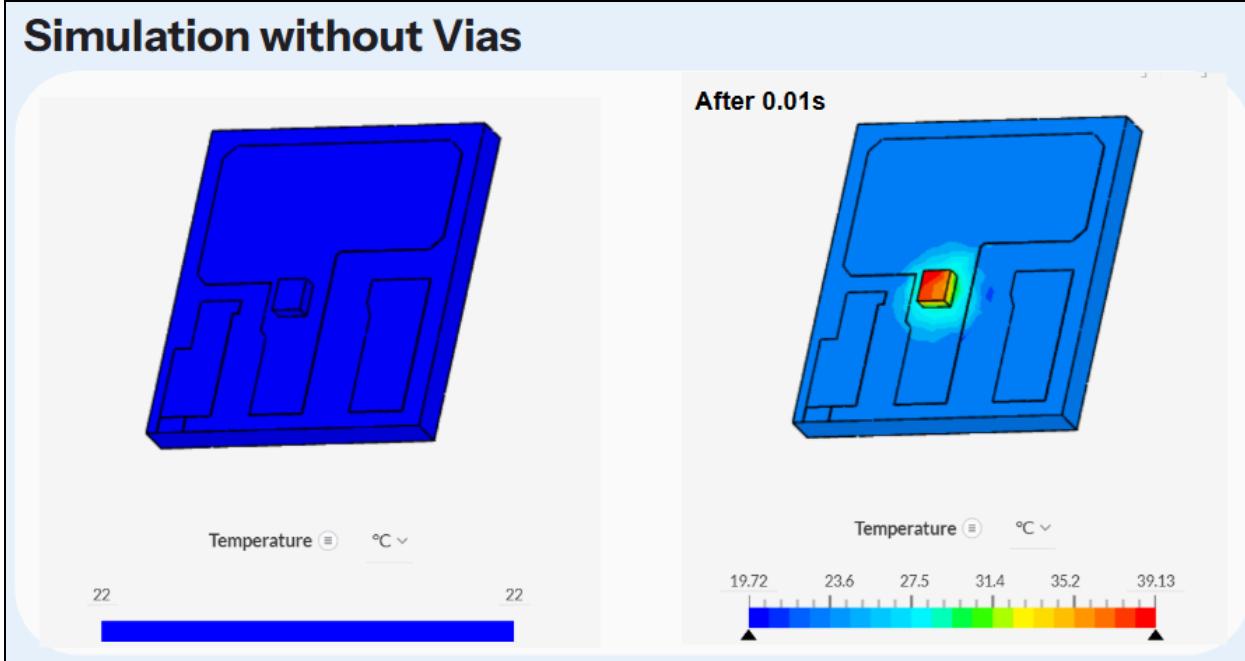


Figure 26 Thermal Analysis of COB without via at different time stamps($t=0s$ and $t=0.01s$)

Simulation without Vias

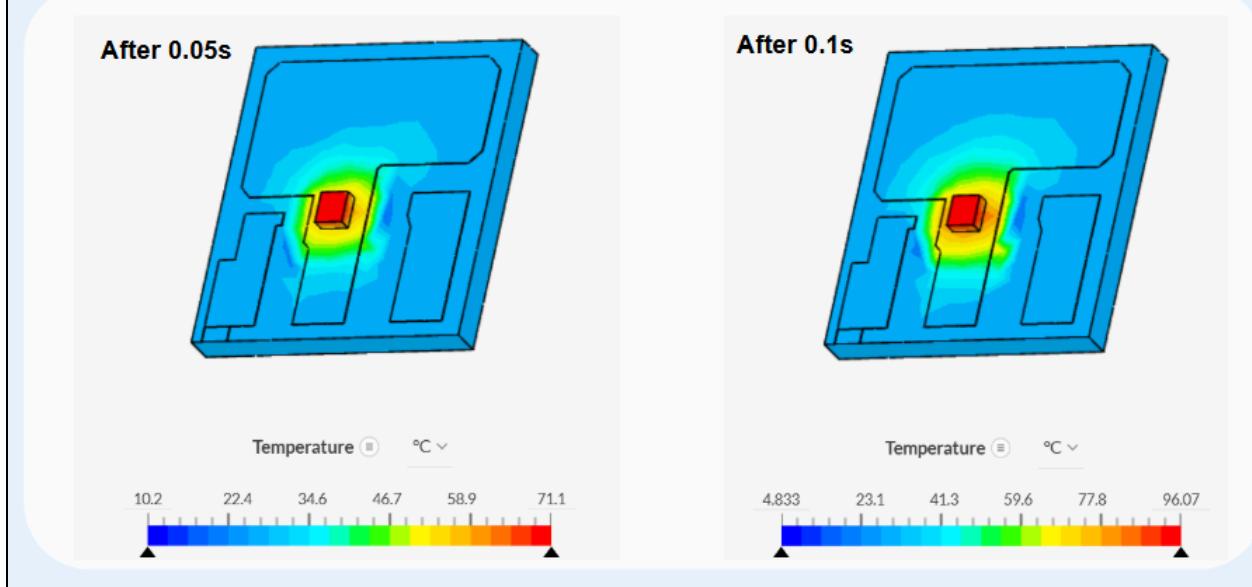


Figure 27 Thermal Analysis of COB without via at different time stamps($t=0.05s$ and $t=0.1s$)

Simulation without Vias

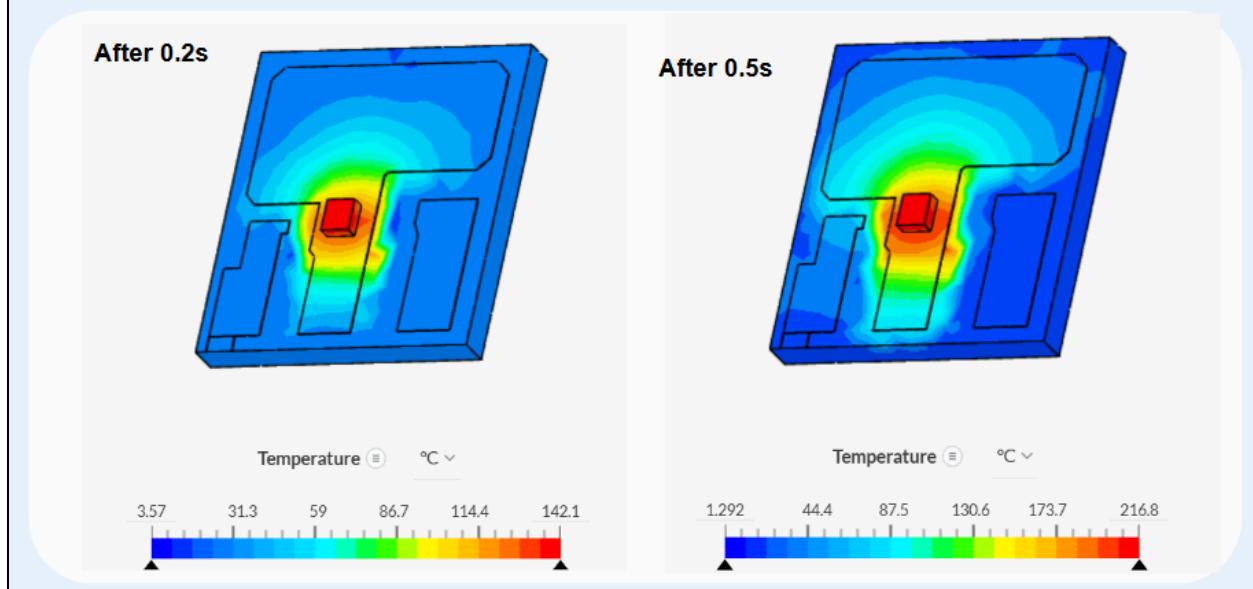


Figure 28 Thermal Analysis of COB without via at different time stamps($t=0.2s$ and $t=0.5s$)

The above results represent the simulation output for the COB layout without incorporating any pin through-holes or vias. This configuration was analyzed to observe the baseline electrical and thermal behavior of the board in its simplest form, without any care taken for thermal management.

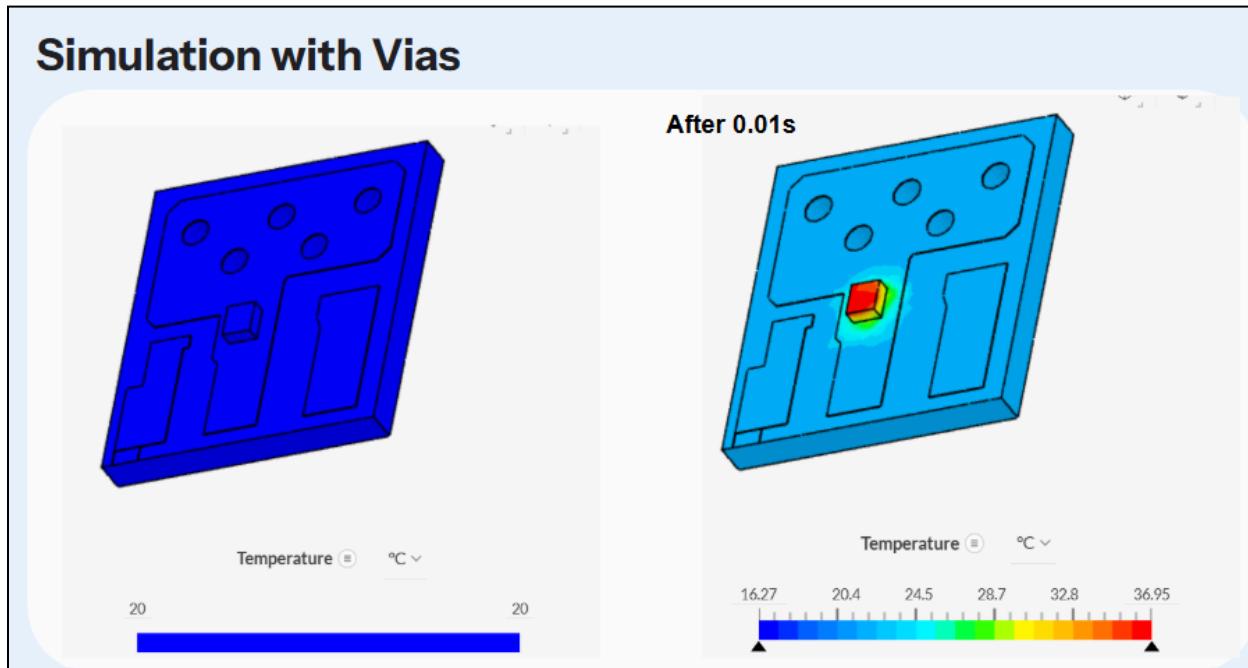


Figure 29 Thermal Analysis of COB with via at different time stamps($t=0s$ and $t=0.01s$)

Simulation with Vias

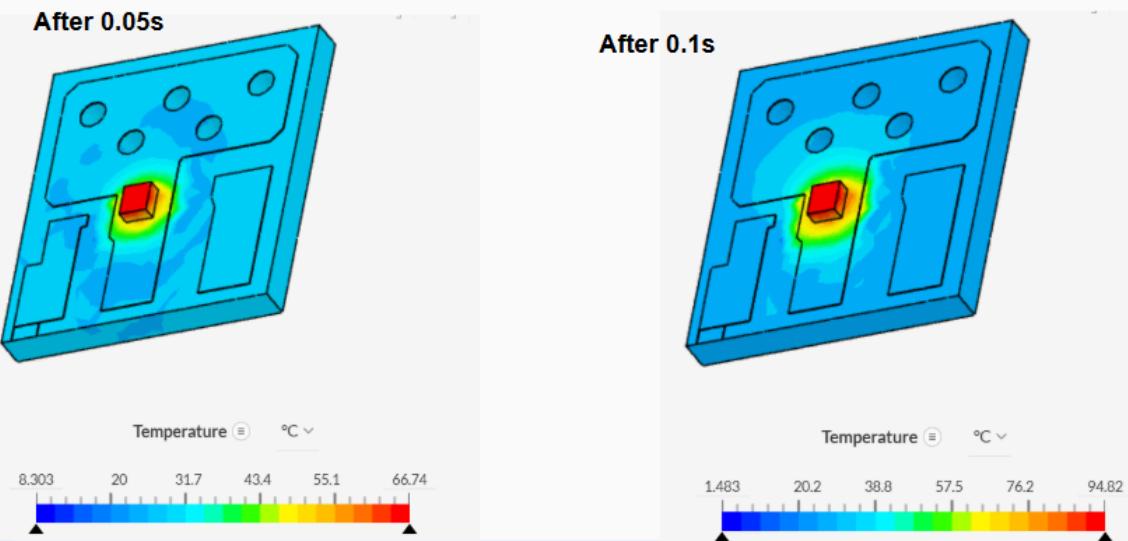


Figure 30 Thermal Analysis of COB without via at different time stamps($t=0.05s$ and $t=0.1s$)

Simulation with Vias

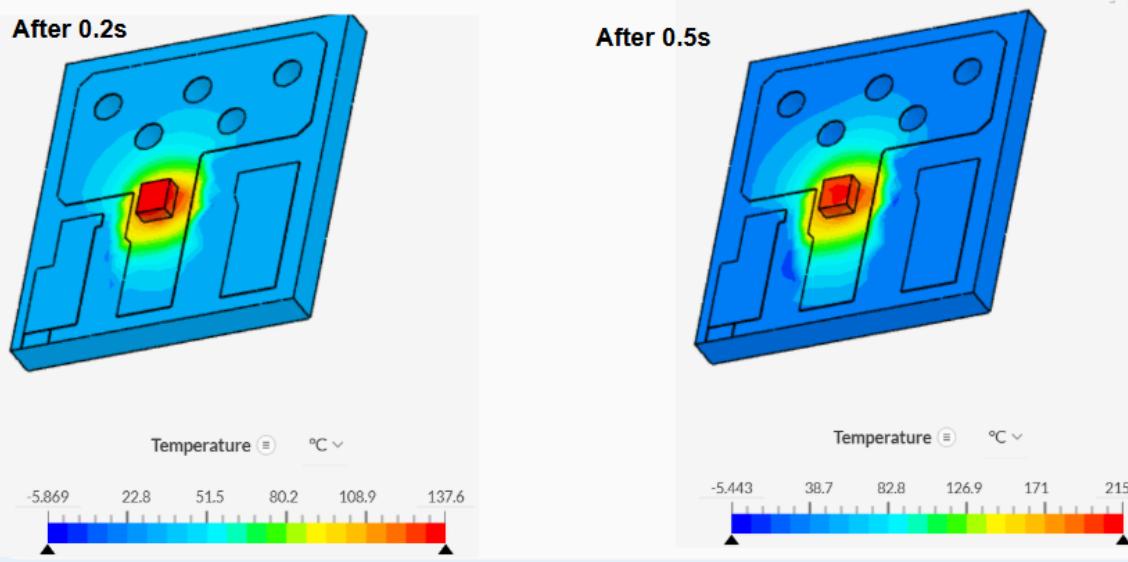


Figure 31 Thermal Analysis of COB without via at different time stamps($t=0.2s$ and $t=0.5s$)

The above results represent the simulation output for the PCB layout with Vias and Plated Through Holes included. This configuration was analyzed to observe the electrical and thermal behavior of the board with Plated through holes for dissipation of heat.

9.3 Heat dissipation techniques

There are various design techniques for managing heat within PCBs, depending on design constraints, environmental conditions, and the power density of the application.

- 1) High Thermal Conductivity Prepreg and Dielectric Materials: Advanced prepreg materials with enhanced thermal conductivities are used to optimize heat flow within the PCB.
- 2) Thick Copper Layers: Increasing the copper weight on internal and external layers (e.g. 2 oz to 4 oz) allows for higher current carrying capacity and improved heat spreading. This is crucial for power electronics and high-current designs where Joule heating must be minimized.
- 3) Via Array: Thermal vias provide vertical heat transfer paths from surface-mounted components to external heat sinks. This technique is particularly effective when combined with bottom-side heat sinks.
- 4) Post-Bonded Metal Backing: A thick metal plate, often copper or aluminum, is bonded to the PCB's backside after fabrication. This enhances both thermal mass and spreading, and is suitable for boards with asymmetrical heating or where large-area dissipation is needed. Thermal adhesives offer stable performance across a wide range of operating temperatures and are effective in rigid and rigid-flex PCB

configurations.

- 5) Embedded metal layers (Internal solution) Embedded metal layers are internal, usually, copper or aluminum planes integrated within the PCB stack-up to enhance in-plane heat spreading and vertical heat conduction.
- 6) Embedded Metal Coins (T-coin, I-coin, U-coin) Metal coins, typically made of copper or aluminum, are embedded within the PCB stack-up directly beneath heat-generating components. They function as localized thermal spreaders, quickly conducting heat away from critical areas. The shape and size of the coin (T, I, or U profiles) are selected based on thermal simulation and board layout constraints.

CHAPTER 10: ELECTRICAL, THERMAL AND MECHANICAL STABILITY

10.1 Vias : The interlayer connections of PCBs

Vias are essentially conductive pathways that act as vertical bridges, establishing electrical connections between different copper layers of a multilayer PCB. Without vias, all circuitry would be confined to a single plane, severely limiting design complexity and functionality.

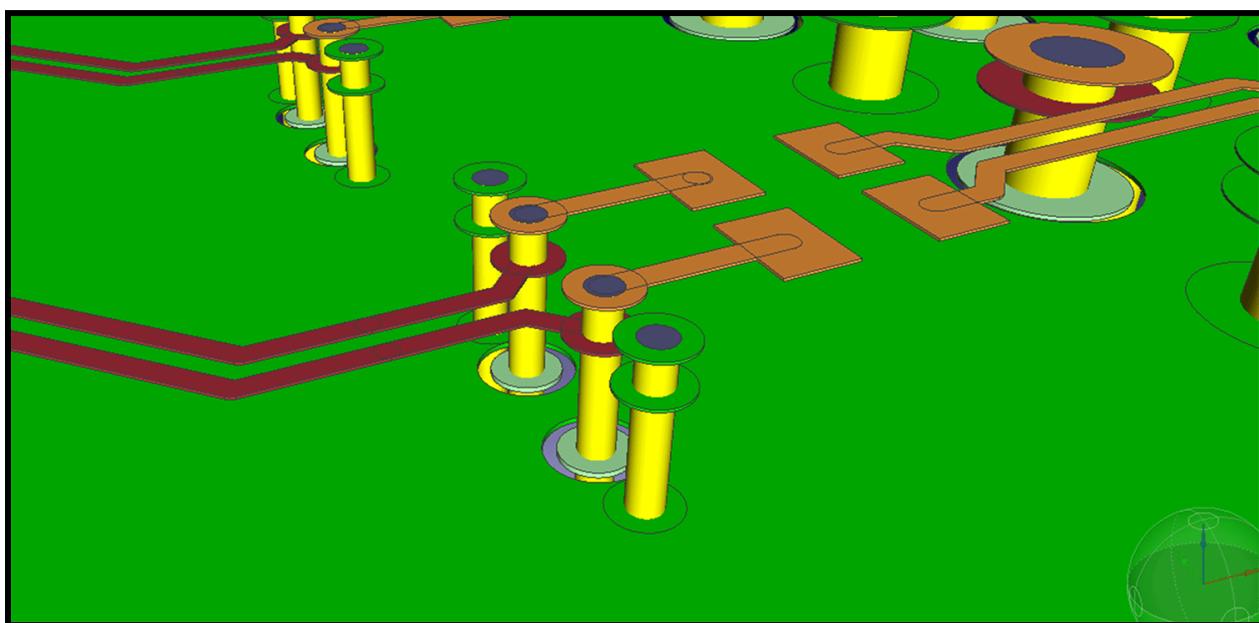


Figure 32 Vias in a PCB

Vias are crucial for various aspects of PCB performance, especially in high-current applications:

1. Power Distribution Through Multiple Layers: A single copper layer might not provide enough width or cross-sectional area in its traces to carry these large currents without excessive voltage drop or overheating. Vias enable designers to route power across multiple layers. By connecting traces or power planes on different layers using vias, the total copper cross-section available for current flow increases. This effectively reduces trace resistance and minimizes voltage drop along the power delivery paths.

2. Grounding and EMI Shielding: Vias are indispensable for creating robust grounding schemes. Via stitching is widely used to connect large copper pours or ground fills on various layers to internal or external ground planes. This creates multiple, parallel paths of low resistance and low inductance for return currents. A solid ground network is vital for stable power delivery, reducing noise, and providing effective EMI shielding by creating a continuous conductive barrier.

3. Heat Dissipation and Thermal Management: High-current traces and active components generate considerable heat. If this heat isn't effectively removed, it can lead to component damage, reduced reliability, or even structural failure of the PCB material. Thermal vias are specifically designed to address this, they are placed strategically to connect hot areas (e.g., under power components) to internal copper planes (which act as heat spreaders) or to external heat sinks. These vias act as efficient thermal pathways, allowing heat to conduct away from the source and spread throughout the board or to a dedicated cooling solution.

4. Mechanical Strength: Vias also contribute to the structural integrity of multilayer PCBs. By creating numerous interconnecting points across layers, especially in areas with large copper pours or high-current traces, they help to bind the layers together more firmly. This reduces the tendency for flexing and delamination (separation of layers), which is particularly important for boards subjected to vibration, mechanical stress, or frequent thermal cycling.

10.2 Types of Vias

- **Via-in-Pad:** Placed directly within (or under) a component's solder pad. It's found under the central pads of heat-generating integrated circuits (ICs) like power MOSFETs, microprocessors, and voltage regulators. The advantage is direct heat transfer.

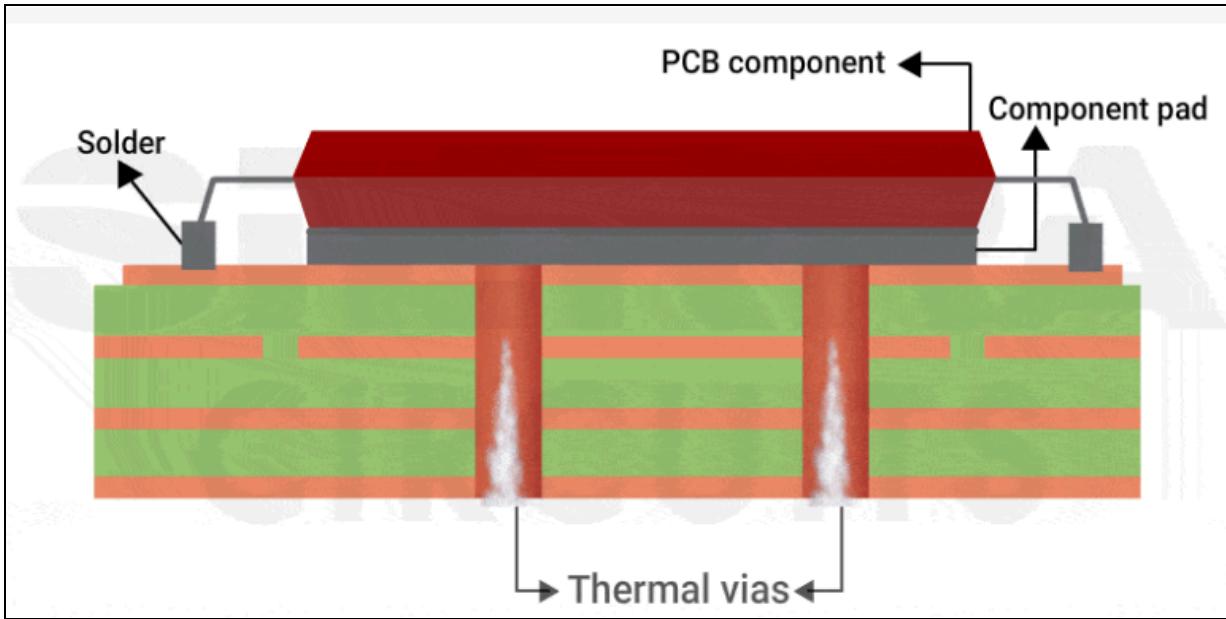


Figure 33 Via in pad

Heat generated by the component flows straight down through the via(s) into internal copper layers (like power or ground planes) or to the bottom side of the board for connection to a heat sink. This heat transfer is mainly through conduction, but it also aids convection when the heat reaches larger heatsink surfaces. This direct thermal path is highly efficient.

- **Filled Vias:** These are vias that, after drilling and plating, are filled with a material, which can be either conductive (copper, silver-filled epoxy) or non-conductive (epoxy resin). They are often then plated over (capped) to create a smooth, sealable surface, allowing components to be directly soldered on top without solder wicking into the via barrel.

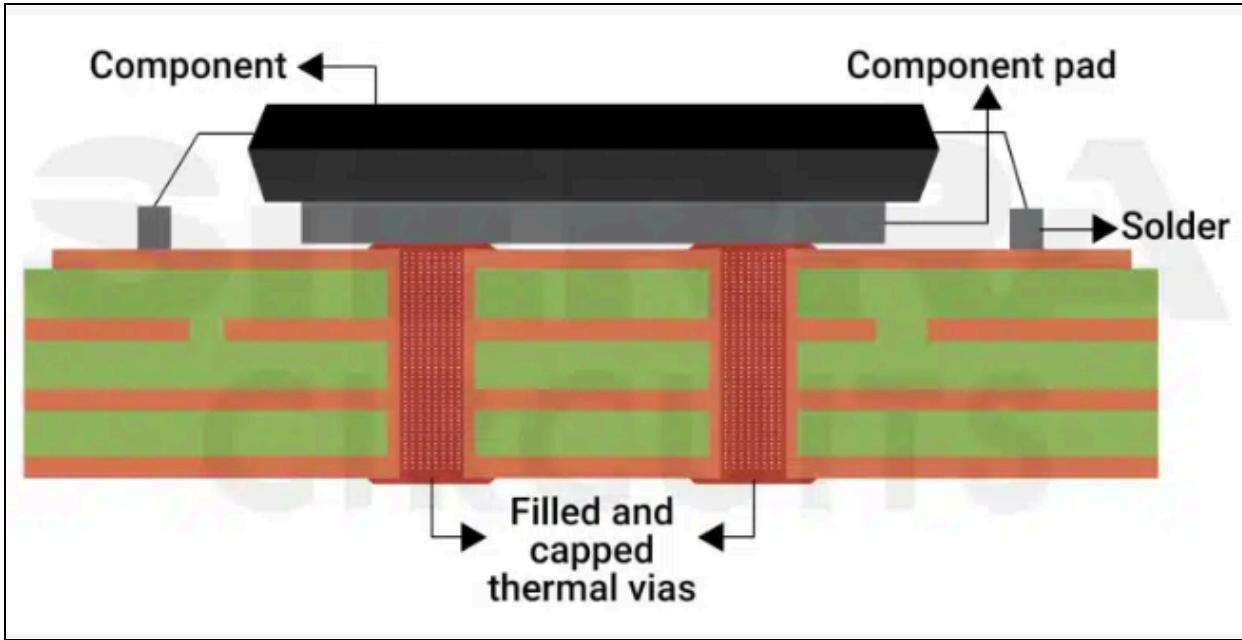


Figure 34 Capped via

If filled with conductive materials (especially metals), filled vias significantly enhance heat dissipation primarily through conduction, offering a superior thermal path compared to standard annular vias. Non-conductive fills improve mechanical stability and prevent solder wicking, but their thermal conductivity is lower than metal fills.

10.3 TO220 package

The TO-220 is a widely recognized and industry-standard through-hole package specifically designed for moderate to high-power electronic components. Its robust design makes it a popular choice for applications where significant heat dissipation is required.

TO-220 = Transistor Outline style #220, per JEDEC standard.

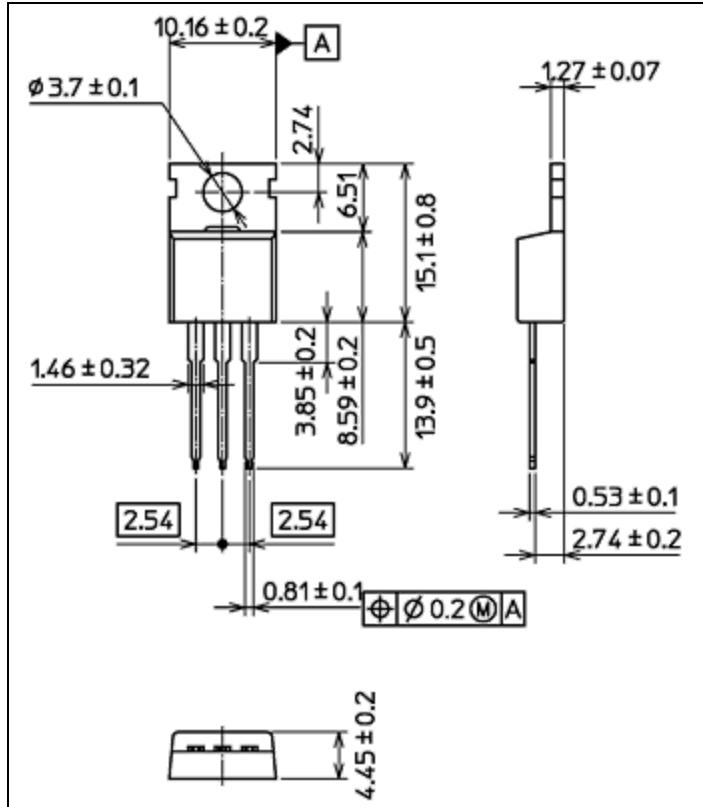


Figure 35 TO-220 package dimensions

Key Features:

- Structure: It typically features a rectangular plastic body from which three electrical leads (pins) emerge, spaced 2.54 mm apart, for mounting through holes on a PCB. While three leads are common, variants with more (up to seven) also exist.
- Metal Mounting Tab: A distinctive characteristic is its integrated metal tab, often with a pre-drilled mounting hole. This tab is crucial for efficient heat transfer.

Thermal Design & Heat Dissipation:

- The primary advantage of the TO-220's metal tab is its ability to be securely bolted or clamped to an external heatsink. This direct mechanical connection provides an excellent thermal pathway, allowing the device to effectively dissipate tens of watts of heat away from the component. This is critical for preventing overheating and ensuring the component's reliability and lifespan.

Electrical Isolation and Versatility:

- The metal tab is often electrically connected to one of the internal component leads (e.g., the drain of a MOSFET). This allows for flexible electrical isolation options:
 - It can be mounted directly to a heatsink if electrical isolation isn't required.
 - Alternatively, an insulating pad or washer can be placed between the tab and the heatsink to provide electrical isolation while still maintaining thermal contact.

Industry Standard:

- The TO-220 boasts an industry-standard footprint, meaning its dimensions and pin layout are widely recognized and supported by design tools and manufacturing equipment. This standardization greatly simplifies board design and streamlines the manufacturing process for devices utilizing this package.

CHAPTER 11: RESULTS AND DISCUSSIONS

The project involved the design and thermal analysis of Chip-on-Board (COB) layouts for GaN power devices. Two versions of the same layout were created: one incorporating plated-through holes and another without any vias. Both layouts shared the same two-layer PCB stack-up, trace widths, clearances, and die placement to ensure a fair comparison based solely on thermal behavior.

The objective of this thermal analysis was to understand how via placement affects heat dissipation from the GaN die and to validate the effectiveness of thermal vias in practical PCB-level thermal management.

In the design with vias, an array of PTHs was placed directly beneath the central die attach pad and surrounding copper region. These vias act as vertical thermal channels, enabling efficient heat conduction from the top copper layer to the bottom layer and into the PCB substrate. The via diameters were varied ranging from 2.0 mm to 0.2 mm. The spacing of the vias was also maintained to align with TO-220 compatible pin pitch (2.54 mm), allowing device leads to be soldered directly onto the board without layout modifications.

In contrast, the via-less version relied solely on lateral heat spreading through the top copper layer and PCB dielectric, which inherently offers higher thermal resistance. Without a vertical conduction path, thermal energy remains localized around the die, increasing the risk of thermal hotspots and slower cooling rates. This design, while simpler to fabricate, presents thermal limitations for power-dense applications.

Simulation tools were used to apply a constant heat flux of $5.95 \times 10^9 \text{ W m}^{-3}$ at the die region and observe temperature distribution and transient thermal behavior over time. The results clearly indicated that the design with vias reached thermal equilibrium at a lower temperature compared to the via-less version. This confirms that PTHs play a vital role in enhancing thermal conductivity, reducing the junction temperature, and improving long-term reliability of the GaN device.

Additionally, the via-enabled layout included dedicated force and sense pads connected through vias to the bottom layer. This allowed for Kelvin (4-wire) measurement, which isolates voltage sensing from the main current path and

eliminates the effect of parasitic resistance in the traces. This feature is particularly valuable during electrical characterization of GaN devices, where high accuracy is essential for capturing dynamic behavior and threshold voltage shifts under varying load conditions.

CHAPTER 12: CONCLUSION

The presented project effectively highlights the critical role of design optimization in Chip-on-Board (COB) packaging for GaN-based power devices. Through detailed implementation and evaluation, it was demonstrated that:

- Thermal vias play a vital role in managing heat dissipation, significantly minimizing temperature rise during high-current operation.
- The integration of 4-wire measurement capabilities greatly improves electrical characterization accuracy, ensuring reliable benchmarking and test repeatability.
- Careful attention to pad layout, trace width, and via sizing ensures a robust balance between thermal management and electrical performance, particularly in high-frequency applications.

Overall, the findings reinforce that thermal and electrical co-design is essential in modern power electronics packaging. In particular, via integration should be regarded as a standard design practice, not only for enhancing thermal performance but also for enabling precision measurements. These principles are especially critical in realizing the full potential of GaN devices in compact, high-efficiency power modules.

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APPENDICES

Appendix A: Glossary

- Chip-on-Board (COB): A packaging method where the bare die is directly mounted and wire bonded onto the PCB.
- Gallium Nitride (GaN): A wide bandgap semiconductor known for high efficiency, fast switching, and high voltage handling.
- High Electron Mobility Transistor (HEMT): A transistor structure utilizing heterojunctions (commonly AlGaN/GaN) to form a high-speed, high-power

2D electron gas (2DEG) channel.

- Two-Dimensional Electron Gas (2DEG): A confined layer of electrons at the heterojunction interface, offering high mobility and conductivity.
- Plated-Through Hole (PTH): A via with copper plating that connects PCB layers and allows for electrical or thermal conduction.
- Kelvin Sensing (4-Wire Method): A precision measurement technique using separate force and sense lines to eliminate voltage drop errors.
- Trace Width: The physical width of a copper trace on a PCB; affects current handling capability and thermal performance.
- Trace Spacing: The distance between adjacent copper traces; crucial for isolation, impedance, and safety.
- Electroless Nickel Immersion Gold (ENIG): A surface finish used to protect copper, improve solderability, and resist electromigration.
- Thermal Vias: Vias placed to conduct heat from the component to internal planes or the backside of the PCB.
- TO-220 Package: A standard through-hole package for power components, featuring a metal tab for heatsinking and pin spacing of 2.54 mm.
- GDSII File: A binary layout file format used in IC manufacturing to define geometric structures layer-by-layer.
- Gerber File: A standard file format for defining PCB layer data used in fabrication (traces, masks, silkscreen, etc.).
- SimScale: A cloud-based simulation platform supporting thermal, structural, and CFD simulations for engineering models.

- Heat Flux: The rate of thermal energy applied per unit volume or area; used to simulate internal heat generation in components.
-

Appendix B: Simulation and Analysis Details

- Thermal analysis was performed using SimScale, a cloud-based multiphysics simulation platform.
- The simulation modeled steady-state convection with ambient temperature set to 25°C.
- Heat was applied to the central copper pad representing the GaN die region.
- A volumetric heat flux of $5.9 \times 10^9 \text{ W/m}^3$ was used, corresponding to 10 A current passing through a small die.
- Boundary conditions were set as natural convection on both top and bottom surfaces.
- Two PCB configurations were analyzed:
 - One with thermal vias placed under and around the die attach pad.
 - One without vias, acting as a thermal baseline.
- The board stack-up included 2-layer copper planes (top and bottom) using standard FR-4 dielectric.
- Results showed:
 - The via-enabled layout exhibited better heat conduction and lower steady-state temperature.
 - The via-less design had increased thermal resistance and localized heat accumulation.

- Additional Kelvin (force and sense) pads were connected using vias in the via-based design to enhance measurement accuracy.
- The simulations confirmed that thermal vias significantly improve thermal management in COB-based GaN device layouts.