# EE230: Project
# Class D Amplifier

Shubhang Bhatnagar, 160020019
Akash Kumar , 160020009

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## 1 Goal of the project

The goal of the project is to make a class D amplifier, which is one of the most efficient kinds of audio amplifier used today.The goal of the simulation is to test out our design on a simulator so that we can ensure that there are no major flaws in our design.

## 2 Simulation Setup

I am using the software ngspice for simulating the circuit. The simulation is being used to find out whether the ratings of the components we plan to use are appropriate or not. Also it would help us to determine whether our circuit can work satisfactorily for various input frequencies. It would also helpus decide the approximate range of bias voltages neede in the circuit(especially the MOSFETs)The ngspice based simulation is being used by me to first independently test if all the components (with their rated speed etc.) are working correctly individually and then I combined them all to make a single class D amplifier where I tested if all the components perform well when working simultaneously.
The main blocks into which we divided the class D amplifier are-

- Sinusoidal Pulse Width Modulation Circuit
- Amplification stage

- Low pass filter

Each of them is elaborated about in the following section-

## 2.1 Sinusoidal Pulse Width Modulation Circuit

The basic principle of a class D amplifier involves pulse width modulation. It helps in making the class D amplifier more efficient as then the MOSFETs in the amplificaton stage are not always ON and they rapidly turn ON and OFF(as required by the input), thus minimizing the power losses.

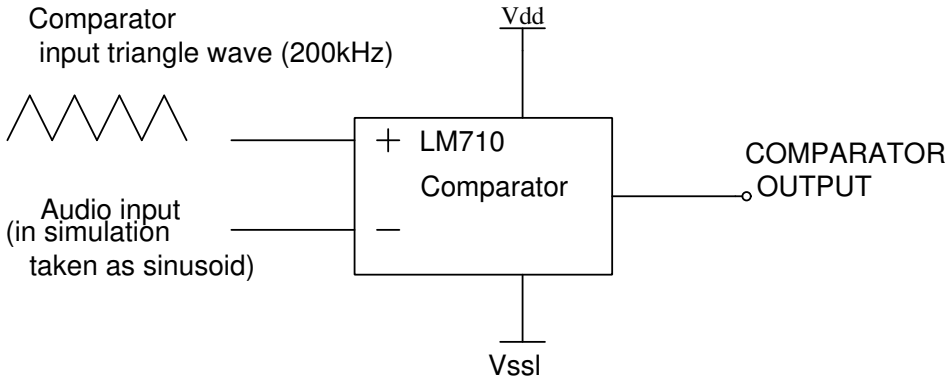


Figure 1: The PWM comparator

The PWM technique involves comparing the input audio signal with a high frequency triangular carrier wave using a high speed comparator. The resulting output, which would be in the form of pulses (whose width would vary continuosly) is given as input to the MOSFET amplifier stage, after appropriately passing it through the MOSFET driver circuit. The triangular wave frequency used is at almost 10 times the frequency of the input audio signal(which is usually in the 20 Hz- 20 kHz range). Also, we used 2 comparators to produce 2 different control signals(almost complementary) for the 2 output NMOS.

The 2 control signals produced for the 2 NMOS in the amplifier stage should be **non overlapping**, as otherwise there would be a condition called 'shoot

through'. Shoot through implies that when the 2 MOS switches are on together , the positive and negative supplies are connected directly, leading to a very high flow of current damaging the MOSFETs. So, we need to ensure 2 non overlapping signals for the 2 NMOS.

We achieve this by providing a small positive DC offset to one of the 2 triangular waves being input to the one of the 2 comparator's. This would help in implementing a slight urn on delay and a slightly early turn off for the MOS receiving the PWM signal generated by the triangular wave with a DC offset, thus preventing shoot through.

## 2.2 Amplification stage

The amplification stage consists of 2 power MOSFETs ( I have used IRF530, available in the WEL lab) connected as-

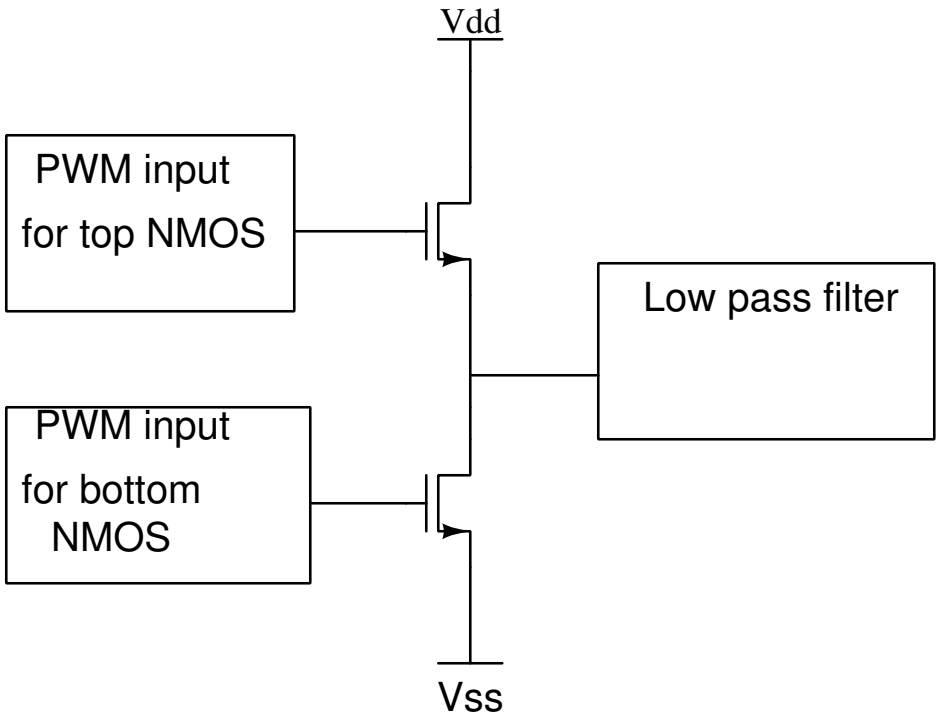


Figure 2: The amplifier stage circuit

The power NMOS's amplify the given PWM signal with the only losses being the switching losses(while charging the gate capacitor) and the small loss due to the $R_{ds}$ of the NMOS. This helps in giving the amplifier high efficiency. But this leads to a high frequency harmonic( of freq near the traiangular wave frequency used) in the output, making the use of a low pass filter necessary.

Also, here it can be clearly seen that the 2 MOSFETs should not be ON together, so we provide them 2 non overlapping signals, generated using the method described in the previous section.

## 2.3 Low pass filter

We use a second order butterworth filter to filter out the high frequency harmonics generated due to the PWM. We use a passive LC filter for it (as components for an active filter are not available in WEL lab for this power rating).

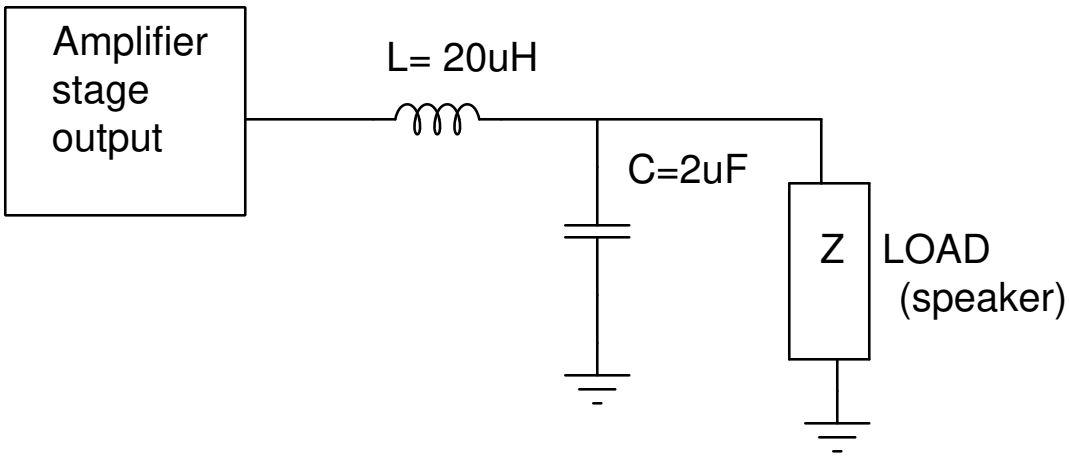


Figure 3: circuit used for LC second order low pass filter

The cut off frequency for such a low pass filter=
$f_o = \frac{1}{2\pi\sqrt{LC}}$
So, we design a filter with a cut off frequency of approximately= 25 kHz for which

L=20 $\mu$H
and C= 2 $\mu$F
which gives a cut off frequency of 25.177 kHz.

# 3 Simulation Results

## 3.1 Sinusoidal PWM results

I used a 200 kHz triangular wave fo the simulation and tested it with various sinusoidal inputs(representing various audio frequency inputs)

The resultant output and the sine wave(of freq= 2kHz) are plotted in the figure-

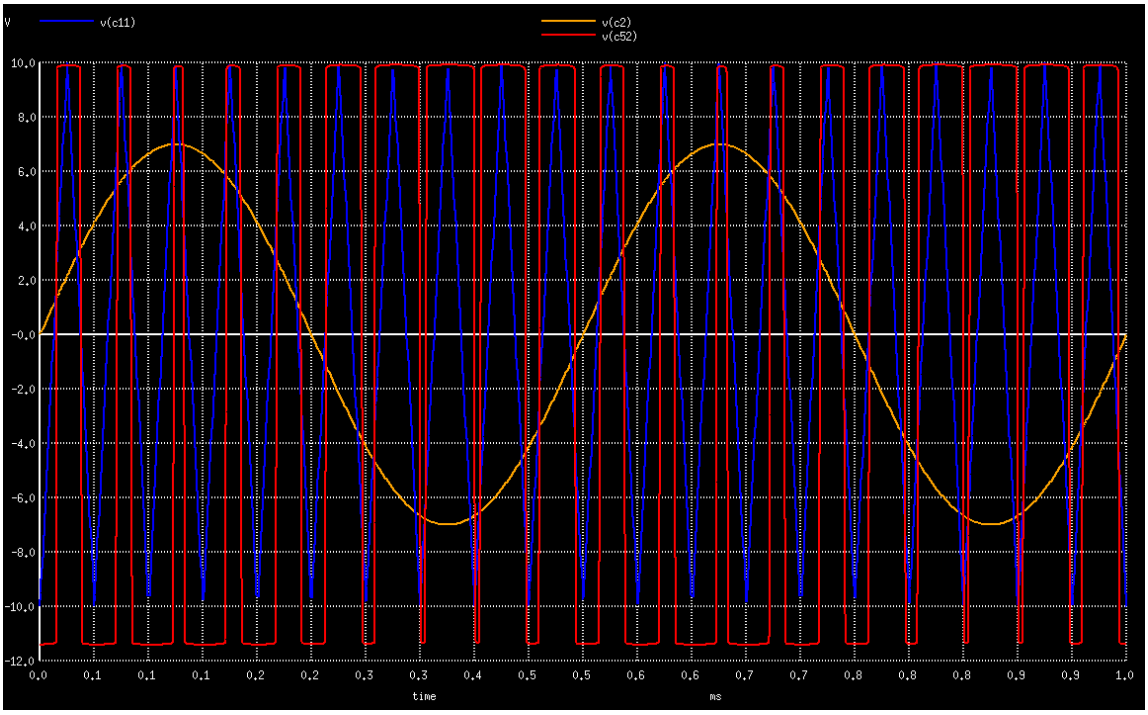


Figure 4: The pulse width modulated waveform along with the triangular wave and audio signal

The 2 triangular waves I used had one of them varying from -10 V to 10 V and the other with a DC offset of 1 V varying from -9 V to 11V to prevent

the problem of shoot through as explained in the previous section.

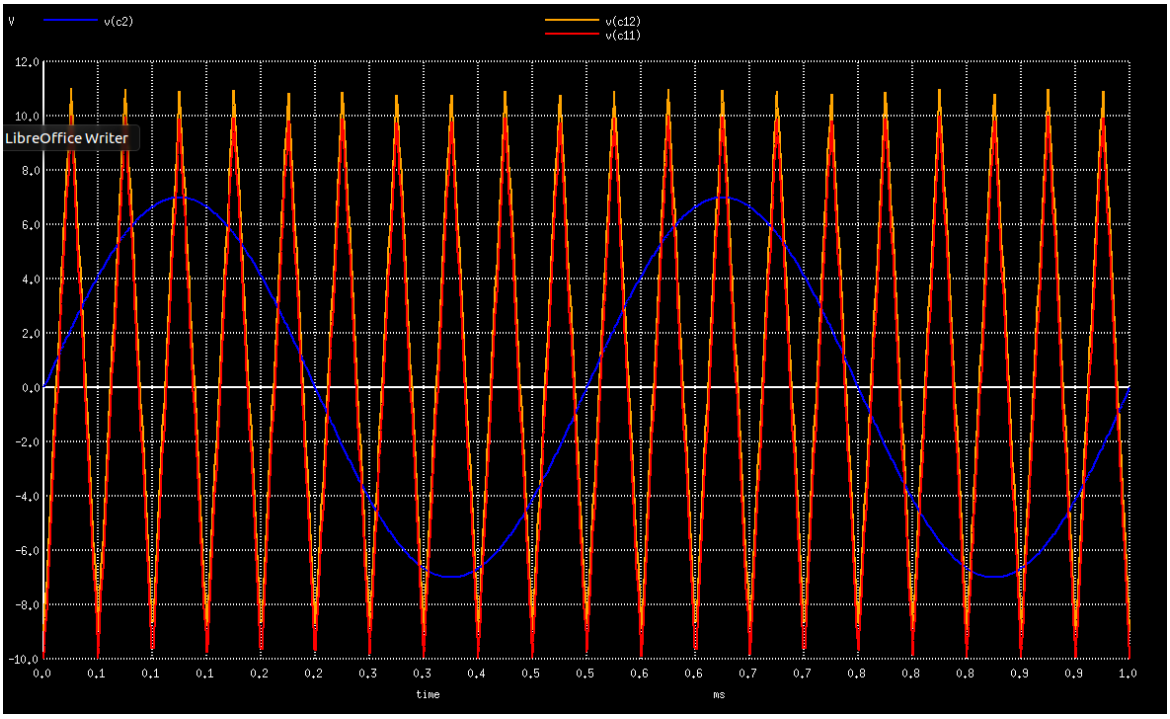


Figure 5: The 2 triangular waves along with the sinusoidal waves

This produces 2 non overlapping almost complementary signals which are used as the switching signals. This part of the simulation helped me to ensure that 2 non overlapping signals are really being generated and the comparator is working as expected.

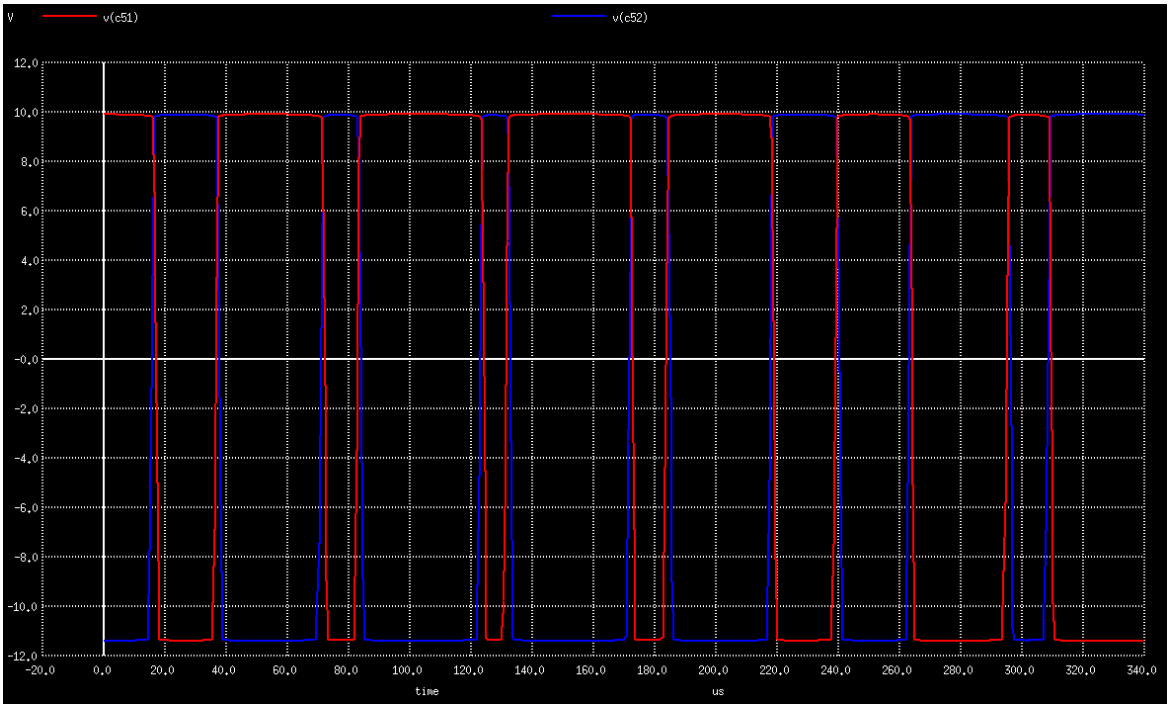


Figure 6: The 2 non overlapping signals produced

## 3.2 Amplifier stage

The 2 MOSFETs being used are 2 NMOS's and their amplification is the one which makes the amplifier work. The output by them is given in the form of an amplified version of their input signal and has voltage pulses.

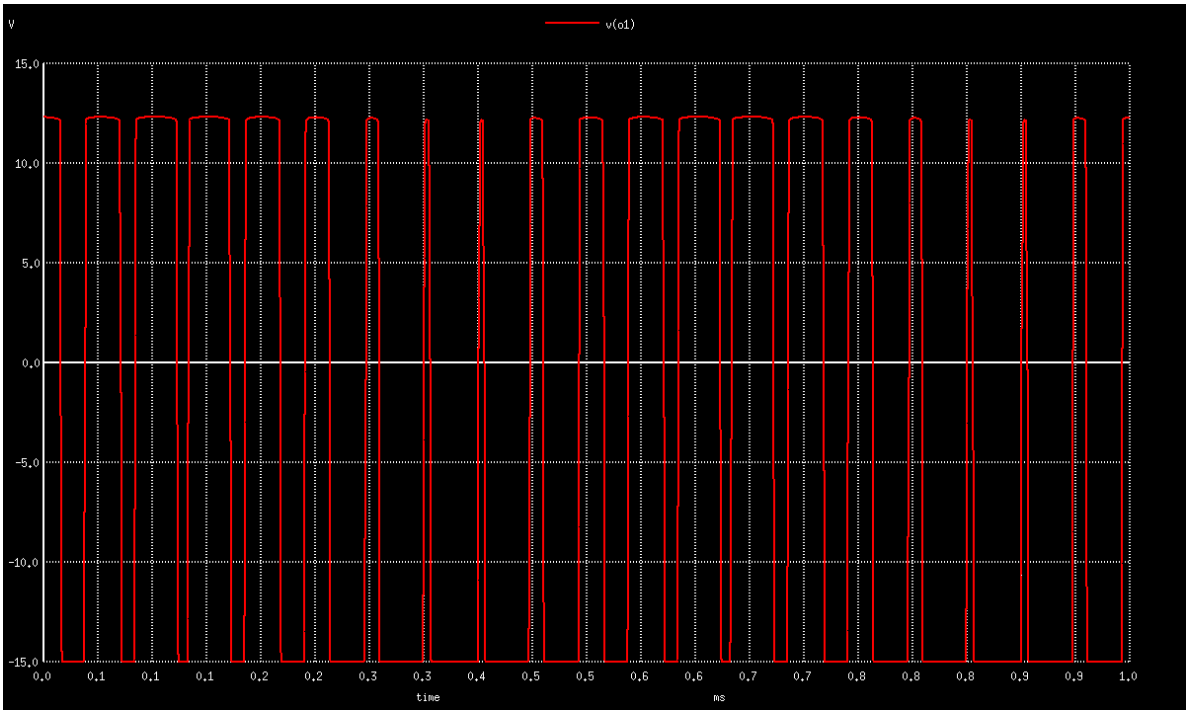


Figure 7: The output of the amplifier stage which is an amplified PWM

## 3.3 Low pass filter

The low pass filter we designed has a cut off frequency of 25.177 kHz and is a second order butterworth filter. Its bode plot/transfer function plot of V out vs V in is-

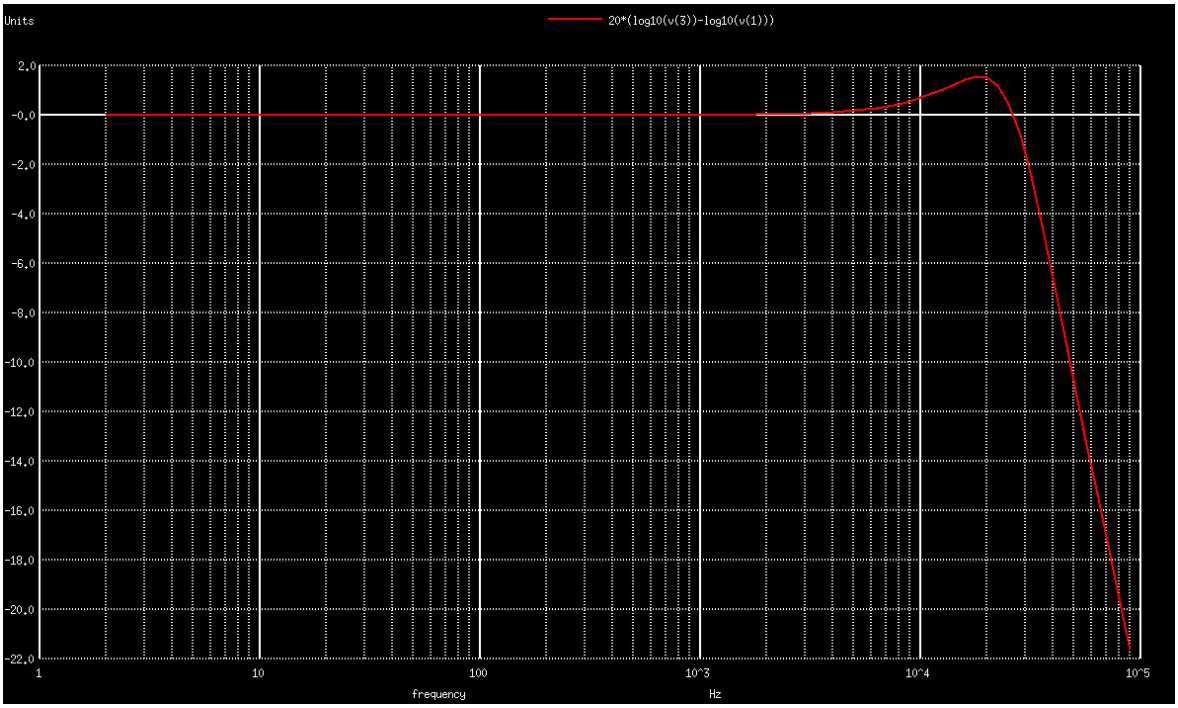


Figure 8: The transfer function of our LC filter

I have used a inductor of $20\mu$H and a capacitor of $2\mu$F in the simulation. Also I have assumed a series resistance of $3\Omega$ of the inductor o account for its non ideality.

# 4 Observations and inferences

## 4.1 Sinusoidal PWM

The PWM output controls when the MOSFETs are on or off. As seen in the simulation, they are not always ON and hence The 2 control signals produced for the 2 NMOS in the amplifier stage should be **non overlapping**, as otherwise there would be 'shoot through'.

We achieve this by providing a small positive DC offset to one of the 2 triangular waves being input to the one of the 2 comparator's. This would

help in implementing a slight turn on delay and a slightly early turn off for the MOS receiving the PWM signal generated by the triangular wave with a DC offset, thus preventing shoot through.As seen in the above results plot, this leads to 2 non overlapping clocks, without which our amplifier could have got seriously damaged due to the high current.

### 4.2 Amplifier stage

The power NMOS's amplify the given PWM signal with the only losses being the switching losses(while charging the gate capacitor) and the small loss due to the $R_{ds}$ of the NMOS. This helps in giving the amplifier high efficiency. The simulation helpsus verify the gain of the MOSFETs and tune it by changing the bias voltages appropriately.

### 4.3 Low pass filter

This is important for the experiment as it helps designing a filter with the appropriate cut off frequency, which will allow our audio signal to pass without significant attenuation. The 20 Hz-20 kHz audio signal is not attenuated significantly, as seen from the Bode plot. Also as we see from the plot the harmonic around the switching frequency(200 kHz) would be highly attenuated, thus making the filter suitable.
This simulation helped us choose appropriate values of inductors and capacitors for our filter.

## 5 Appendix

The code for PWM and amplifier stage is as follows

```
sim1
.include comparator.txt
.include IRF530.txt
*Comparator
x1 c11 c2 30 31 c51 COMPARATOR
x2 c2 c12 30 31 c52 COMPARATOR

*Power
vcc c3 0 15v
```

```
vdd c4 0 -15v
vdd2 30 0 15v
vss2 31 0 -15v

*r1 c51 0 10000k
*r2 c52 0 10000k

*triangular
Vtr1 c11 0 PWL(0 -9 25us 11 50us -9) r=0
Vtr2 c12 0 PWL(0 -10 25us 10 50us -10) r=0

*sine
Vin c2 0 sin(0 7 2khz 0 0)

*MOSFETS
m1 30 c51 o1 IRF530
m2 o1 c52 31 IRF530


*speaker/resistor
r3 o1 0 10000k

.tran 1us 1ms
.control
run
*plot v(c51) v(c11) v(c2) v(c52)
*plot v(c11) v(c12) v(c2)
plot v(o1) v(c52) v(c51)
*plot v(o1)
*plot v(c51) v(c52) v(o1)
*plot i(vdd2)
*plot v(c52)
*plot v(c4)
.endc
.end
```

The code for the LC filter is as follows-

```
*Low pass filter transfer characteristics simulation
l1 1 2 20uH
R1 2 3 3
c1 3 0 2uf
Vin 1 0 ac 1 dc 0
.AC DEC 20 2 100kHz
.control
run
plot 20*(log10(v(3))-log10(v(1)))
.endc
.end
```