EE 381: EE LABORATORIES (DIGITAL CIRCUITS AND MICROPROCESSORS)
2017-2018/II

EXPERIMENT 1: SYNCHRONOUS & RIPPLE COUNTERS

PART 1: SYNCHRONOUS COUNTERS

Design a divide-by-SIX synchronous counter using 74LS76 Dual J-K negative edge-triggered flip-flops. The sequence of states of the counter should be (CBA): 000, 010, 110, 001, 111, 101, 000 ….. . Ensure that if state 011 occurs the next state is 000 and if 100 occurs then the next state is 111. The ICs given to you are: 74LS76 – 2 nos., 7400 (Quad 2-i/p NAND) – 3 nos.

1.1 Lab Preparation

1. Design the above counter making use of appropriate transition tables and K-maps. Verify your design using a suitable table.
2. Draw the complete circuit diagram (functional diagram with all the required pin numbers).

1.2 Experiment

1. Show your design to your tutor before you start.
2. Test the flip-flops of 74LS76 using either manual clock or the Function Generator and CRO.
3. Wire the circuit. Use manual clock (circuit of Fig. 1) and the LEDs (circuit of Fig.2 with value of R chosen such that LED current = 20 mA) to verify that your counter follows the specified sequence. Set the unused states as well and ensure that the next states obtained are as specified.
4. Use TTL clock from the FG as the clock instead of the manual clock. Observe and sketch the Q_C, Q_B, and Q_A outputs with respect to the clock.
5. Increase the frequency of the TTL clock to several megahertz (say 5 MHz). Measure the propagation delay of the flip-flop.

PART 2: RIPPLE COUNTERS

Design a divide-by-EIGHT asynchronous DOWN counter using 74LS74 Dual D-flip flops. Use no other ICs.

2.1 Lab Preparation

1. Design the above counter.
2. Draw the complete circuit diagram (functional diagram with all the required pin numbers).

2.2 Experiment

1. Test the circuit using manual clock and verify that it is working as per design.
2. Use TTL clock from the FG instead of the manual clock. Observe and sketch the Q_C, Q_B, and Q_A outputs with respect to the clock.
3. Using the FG measure the delay between the Q_C, Q_B, and Q_A outputs.

PART 3: PROGRAMMABLE SYNCHRONOUS COUNTER

Design (i) a divide-by-NINE and (ii) a divide-by-THIRTEEN synchronous UP counters using 74LS163 (Synchronous binary counter with synchronous Clear) and ONE 3-input NAND gate (7410) in each case. Use no other ICs.

3.1 Lab Preparation and Experiment

1. Design the above counter and draw the complete circuit diagram.
2. Test the circuit using manual clock and verify that it is working as per design.
3. Use TTL clock from the FG instead of the manual clock. Observe and sketch the O_0, O_1, O_2 and O_3 outputs with respect to the clock.

PART4: DIVIDE-BY-256 SYNCHRONOUS COUNTER (Optional if time permits)

Design a divide-by-256 synchronous counter using two 74LS163 ICs. (Note: To do this experiment you need to understand the roles of the CET, CEP inputs and the TC output of 74LS163).

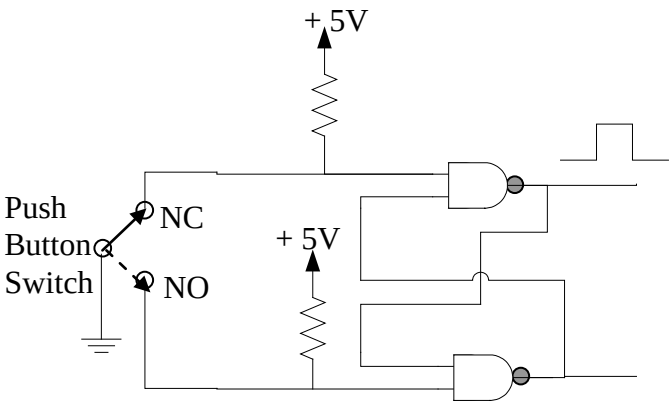


Fig. 1 Manual Clock Circuit

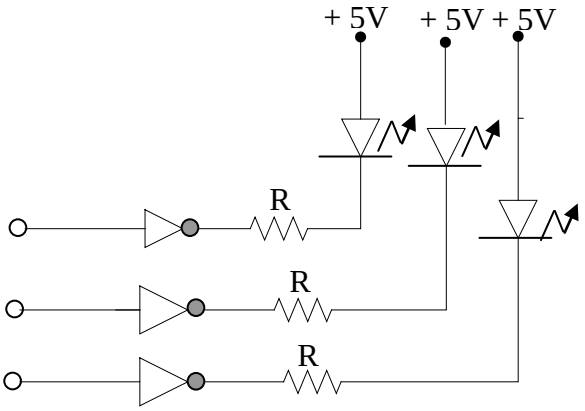
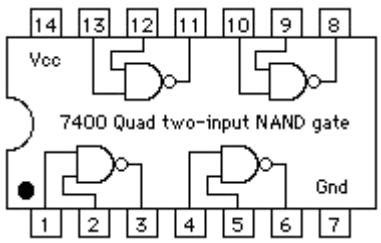
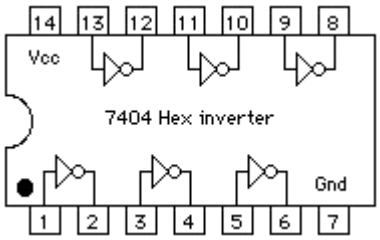
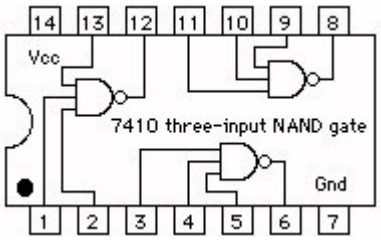


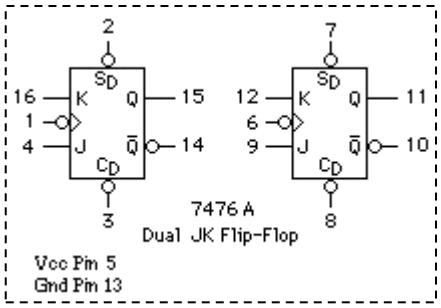
Fig. 2 LED Probes

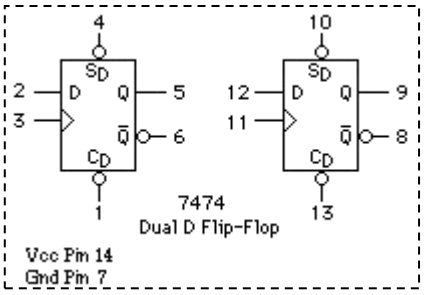
IC PIN Details

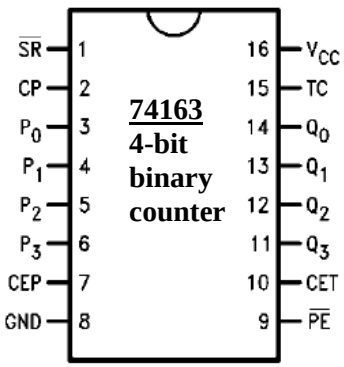












Pin Description and Mode Select Table for **74163**

Pin Descriptions

Pin Names	Description
CEP	Count Enable Parallel Input
CET	Count Enable Trickle Input
CP	Clock Pulse Input
$\overline{SR}$	Synchronous Reset Input
P_0–P_3	Parallel Data Inputs
$\overline{PE}$	Parallel Enable Input
Q_0–Q_3	Flip-Flop Outputs
TC	Terminal Count Output

Mode Select Table

$\overline{SR}$	$\overline{PE}$	CET	CEP	Action on the Rising Clock Edge (⌐)
L	X	X	X	Reset (Clear)
H	L	X	X	Load ($P_n \rightarrow Q_n$)
H	H	H	H	Count (Increment)
H	H	L	X	No Change (Hold)
H	H	X	L	No Change (Hold)

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial