Power Efficiency Model for MIMO Transmitters Including Memory Polynomial Digital Predistortion

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***Abstract*—Multiple-input multiple-output (MIMO) beamforming array gain can make multi-antenna transmitters (TXs) more power efficient. However, these MIMO TXs require more complex digital predistortion (DPD). In this brief, analytical expressions are derived for the power consumption of both MIMO power amplifier (PA) arrays and their respective DPD, taking into account the effects of precoding on PA output power and peak-to-average power ratio (PAPR). It is shown that for complex DPD algorithms such as cross-over DPD (CO-DPD) in combination with wide bandwidths, the overall DPD power consumption can exceed the overall PA power consumption already for scenarios with more than two antennas.**

***Index Terms*—Digital predistortion (DPD), MIMO, transmitter, power amplifier, digital signal processing (DSP), efficiency, power consumption, Volterra series, memory polynomial.**

I. Introduction

SPATIAL multiplexing using multiple-input multipleoutput (MIMO) transmitters (TXs) is widely regarded as one of the key enablers for the next generation of wireless systems, allowing for higher data rates and more simultaneous users [1]. Due to beamforming, array gain is achieved, decreasing the overall PA power consumption for the same effective isotropic radiated power (EIRP) [2].

For high power efficiency, these PAs are normally driven at low back-off. This decreases linearity, such that DPD is required to meet error vector magnitude and spectral mask specifications. For MIMO TXs, DPD algorithms become increasingly complex. The number of PAs increases, and the DPDs need to take into account the effects the PAs have on each other [3]–[6]. This complexity increases rapidly with the number of antennas. Corresponding to the bandwidths for 5G systems, the power consumption of the digital baseband circuitry increase significantly [7], [8]. The clock frequency for the DPDs has to be increased, and the same time constants in the PA, of e.g., bias and supply circuits, will now require more clock periods of compensation, increasing the memory depth [9]. As the number, complexity and clock frequencies of the DPDs increase, so will its power consumption.

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In conventional single-input single-output (SISO) TXs with DPD, the DPD power consumption is generally neglected on the total power consumption. For the next generation of MIMO TXs, the overall PA power decreases, but the overall DPD power consumption increases with the number of antennas.

This brief compares the DPD and PA power consumption for MIMO TXs, indicating the DPD can dominate the power consumption over the PAs for wideband MIMO TXs. In Section II, PA power consumption is analyzed for a given EIRP, taking into account the effect of precoding. Section III gives an overview of MIMO DPD architectures, Section IV analyzes the required number of calculations for a memory polynomial based DPD and Section V relates this to its power consumption in 22 nm FD-SOI CMOS technology. In Section VI, the PA and DPD power are compared. Conclusions are stated in Section VII.

II. Power Amplifier Power Consumption

In order to find the array power consumption, for each PA one needs to know:

1) The power efficiency versus output power
2) The output power probability density function

The latter is affected by the combining of signals in the precoder. Statistical analysis is used to find this parameter.

In Figure 1, a linear array with n_t transmit antennas is considered, transmitting signals to n_r single-antenna receiving users, where $n_r \leq n_t$. Line-of-sight propagation is assumed, resulting in beam patterns with a main lobe in the direction of the respective user. The user positions are random and at least one beam width apart to allow for spatial multiplexing. The precoding matrix $\mathbf{W}$ gives a generalized transfer of:

$$\begin{bmatrix} v_1 \\ \vdots \\ v_{n_t} \end{bmatrix} = \begin{bmatrix} w_{1,1} & \cdots & w_{1,n_r} \\ \vdots & \ddots & \vdots \\ w_{n_t,1} & \cdots & w_{n_t,n_r} \end{bmatrix} \begin{bmatrix} s_1 \\ \vdots \\ s_{n_r} \end{bmatrix} \tag{1}$$

where v_i are the spatially multiplexed signals, s_j are the input signals to the users, and w_{ij} are the precoder matrix elements. i and j are the indices for the transmitter and receiver antenna elements, respectively.

The zero-forcing precoding scheme can be considered to first generate base beams in the directions of the receiving antennas, using only phase shift. The precoder weights w_{ij} in this scenario with $n_t = 8$ and $n_r = 3$ are shown in Figure 2a and are all on the unit circle. Figure 2b shows the corresponding beam patterns versus angle in u-space with

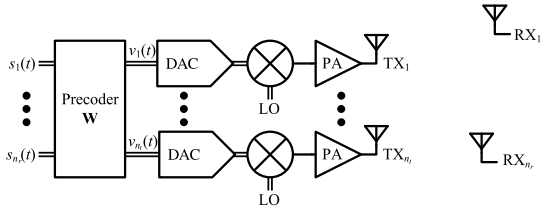

Fig. 1. Generalized MIMO TX with digital precoding. Spatially multiplexed signals are transmitted over n_t TX antennas to n_r receivers (RXs).

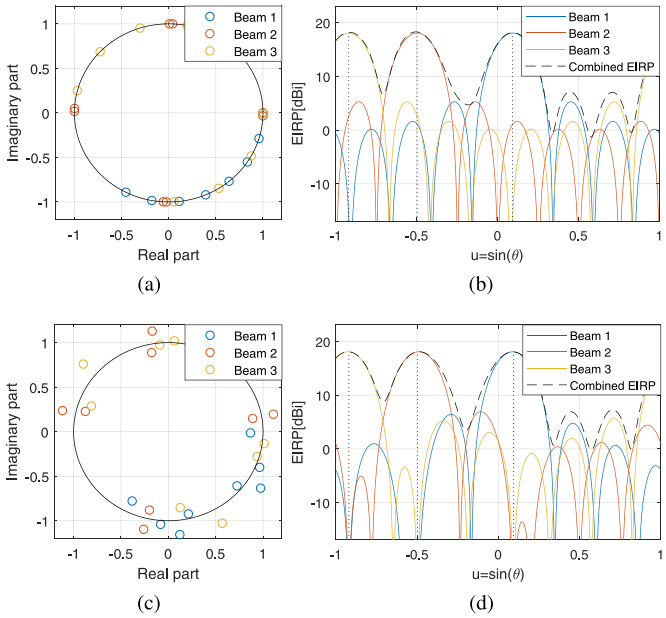

Fig. 2. Precoder weights and beam patterns. (a) Precoder weights w_{ij} for the generating a basis three beam pattern with an 8 element linear array. (b) Resulting beam pattern with interference. (c) Precoder weights for the null-steered orthogonal beams. (d) Resulting orthogonal beam pattern. Beam directions are indicated as dotted lines.

respect to broadside. Note that the side lobes of the beam patterns interfere in the direction of the other beams, albeit at a significantly lower amplitude than the main lobe.

By making linear combinations of these three basis beams, one can make three orthogonal beams, with nulls in the directions of the other beams . The adapted weights for w_{ij} are shown in Figure 2c. In this line-of-sight scenario, null-steering yields the same precoder weights as spatial multiplexing, so the same PA power analysis applies. The weights are still close to the original values, as the beam pattern amplitude inside the main lobe is much larger than the amplitude in the direction of the other receivers outside of it. As they have not shifted much from the unit circle, the modulus of the weigths $|w_{ij}| \approx 1$. The resulting beam pattern is shown in Figure 2d.

For uncorrelated input signals s_j with variance σ_s^2, the variance of the spatially multiplexed signals v_i is:

$$\sigma_{v_i}^2 = \sum_{j=1}^{n_r} |w_{ij}| \sigma_s^2 \approx n_r \sigma_s^2 \tag{2}$$

The distribution of v_i will converge towards a normal distribution for increasing n_r following the central limit theorem, regardless of the distributions of s_j. The the transmitted amplitude $\sigma_{|v_i|}$ is then Rayleigh distributed, as shown in

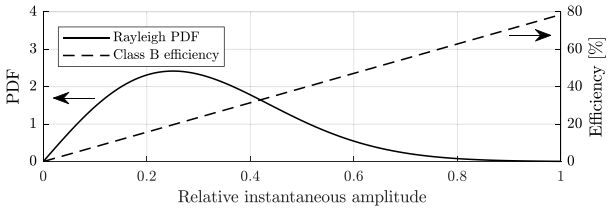

Fig. 3. Rayleigh amplitude probability density function and PA efficiency for an ideal class B amplifier transmitting a normal distributed signal with a peak-to-average power ratio of 9 dB.

Figure 3. This distribution has skirts up to infinite amplitude, albeit at ever decreasing probability density. Analogous to summing sub-carriers in OFDM systems, summing in the precoder yields similar signal properties for the PA input signals. Consequently, clipping can be applied to limit the PAPR to 9dB without significant effects on adjacent channel interference or bit errors [10]. Figure 3 plots this clipped amplitude distribution with 9 dB power back-off, as well as the power efficiency of an ideal class B amplifier. For low GHz frequencies and high f_T, losses due to parasitic capacitance can be neglected. The combination in Figure 3 results in an average PA efficiency η_{avg} of 31%.

As the power of a zero-mean signal is proportional to its variance, the ratio between total single-element EIRP due to all precoded input signals (EIRP_i), and its contribution in the direction of one specific receiver (EIRP_{ij}), is as in Equation (2):

$$\text{EIRP}_i \approx n_r \text{EIRP}_{ij} \tag{3}$$

In the direction of beam j, the field amplitudes of EIRP_{ij} with corresponding j index add constructively for the n_t TX antennas [2]. The EIRP_{ij} terms with indices other than the respective j will cancel due to the nulls in the beam patterns. The EIRP as observed by a receiver (EIRP) is:

$$\text{EIRP} \approx n_t^2 \text{EIRP}_{ij} = \frac{n_t^2}{n_r} \text{EIRP}_i \tag{4}$$

The power consumption for the PA array P_{PA} with ideal isotropic antennas can be found from the transmitted power per PA, the PA power efficiency, and the number of PAs. For a specific desired EIRP for proper communication, this can be further rewritten to:

$$P_{\text{PA}} = \frac{n_t \text{EIRP}_i}{\eta_{\text{avg}}} \approx \frac{n_r}{n_t} \frac{\text{EIRP}}{\eta_{\text{avg}}} \tag{5}$$

The first fraction is the proportion of the u-space which is inside a beam, and the latter fraction relates radiated electromagnetic power to electrical power.

III. MIMO DPD

The trend from single antenna TXs towards MIMO communications changes the TX architectures and with it the DPD in these systems. For simplicity, this section will only illustrate multi-antenna TXs with only two antennas. Three common memory polynomial DPDs are considered. Contrary to look-up table based DPD, they allow for memory DPD and their complexity can be expressed in a number of

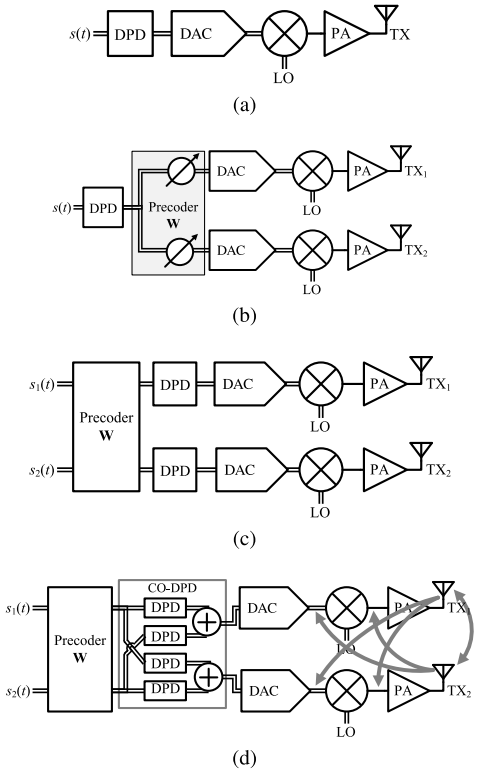

Fig. 4. DPD architectures. (a) Quadrature architectures for SISO TX. (b) SIMO TX with one DPD. (c) MIMO TX with n_t individual DPDs. (d) MIMO TX with CO-DPD and indicated coupling paths. Complex signals indicated with dual lines, feedback network for DPD parameter extraction not indicated.

multiplications. A conventional single-antenna direct upconverstion quadrature TX with DPD is shown in Figure 4a with complex input signal $x(t)$. In this case, only one DPD block is required. When extending this to a multi-antenna system with n_t antennas in Figure 4b, one DPD block still suffices when DPD is performed before phase shifting, as the phase shifted signals will have the same amplitude, and therefore the same distortion. When using a MIMO TX (Figure 4c), the PA input signals will have different amplitudes, and each of the n_t PAs will need a DPD. The system becomes even more complex when there is significant coupling between the TX paths [3]–[6]. CO-DPD, indicated in Figure 4d, was proposed in [4] to linearize these effects, but it increases the number of DPD blocks to n_t^2 [5]. When using a 2-dimensional generalized memory polynomial (2D-GMP), which takes into account all non-linear cross-terms of the inputs, including memory effects [6], the algorithm becomes even more complex.

For equal memory polynomial order K and memory depth M, the algorithms can result in different performance in terms of, e.g., adjacent channel power ratio or error vector magnitude. However, this is highly dependent on the situation, e.g., CO-DPD will excel in a scenario with strong crosstalk. Therefore, DPD power consumption for the different architectures is normalized to equal K and M, rather than performance.

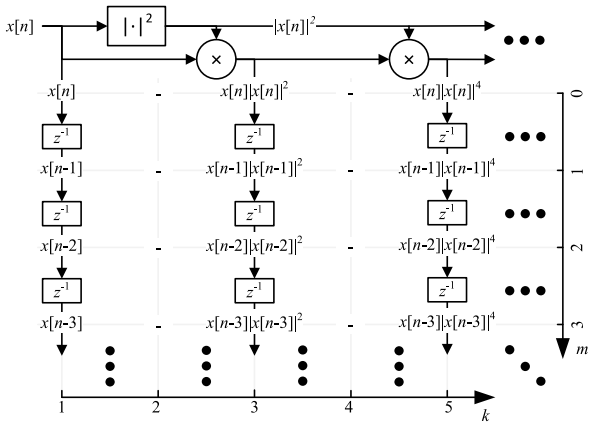

Fig. 5. Efficient method to calculate the basis functions $b_{km}[n]$ [11].

IV. Memory Polynomial Complexity

A common DPD algorithm is the baseband equivalent memory polynomial, based on the Volterra series [9]. It can be regarded as a polynomial extended with linear memory:

$$y[n] = \sum_{k=1}^{K} \sum_{m=0}^{M} h_{km} b_{km}[n] \tag{6a}$$

where

$$b_{km}[n] = x[n-m]|x[n-m]|^{k-1} \tag{6b}$$

$x[n]$ and $y[n]$ are the complex valued input and output of the memory polynomial, respectivelly, and h_{km} are complex coefficients. The polynomials $b_{km}[n]$ in Equation (6b) are often refered to as the 'basis functions', to which a finite impulse response (FIR) filter is applied is applied in Equation (6a). In [11], an analysis is made of the required computations. For minimal complexity, and thus DPD power consumption, the basis functions can be optimized by reusing the delayed result for $x[n]|x[n]|^{k-1}$, and limiting oneself to the dominant odd order linearity (odd k only) for differential PAs. The remaining operations are shown in Figure 5. The total complexity of the basis function calculations is:

$$C_{\text{basis}} = C_{|\mathbb{C}|^2} + \frac{K-1}{2} C_{\mathbb{R}\times\mathbb{C}} + K\left(\frac{P+1}{2}\right) C_{\mathbb{C}z^{-1}} \tag{7}$$

where C denotes the complexity weight of operations on real ($\mathbb{R}$) and complex ($\mathbb{C}$) numbers.

The filter in Equation (6a) multiplies the basis functions with odd p in Figure 5 with a respective complex coefficient and sums these products. The corresponding complexity is [11]:

$$C_{\text{filter}} = (M+1)\left(\frac{K+1}{2}\right) C_{\mathbb{C}\times\mathbb{C}} + \left((M+1)\left(\frac{K+1}{2}\right) - 1\right) C_{\mathbb{C}+\mathbb{C}} \tag{8}$$

Using the implementations in Table I, complex operations in Equation (7) and Equation (8) can be decomposed to real-real multiplications, real-real additions and real delays. The combined basis function and filter complexity is:

$$C_{\text{DPD}} = (MK - M) C_{\mathbb{R}z^{-1}}$$

TABLE I
DECOMPOSITION OF COMPLEX OPERATIONS INTO REAL OPERATIONS

Complex operation	Decomposed real operation $\mathbb{R}+\mathbb{R}$	$\mathbb{R}\times\mathbb{R}$	$\mathbb{R}z^{-1}$
$\mathbb{C}+\mathbb{C}$	2	0	0
$\mathbb{R}\times\mathbb{C}$	0	2	0
$\mathbb{C}\times\mathbb{C}$ [a]	5	3	0
$\lvert\mathbb{C}\rvert^2$ [b]	1	2	0
$\mathbb{C}z^{-1}$	0	0	2

[a] Using the Karatsuba multiplication algorithm
[b] $|\mathbb{C}|^2 = \mathrm{Re}\{\mathbb{C}\}^2 + \mathrm{Im}\{\mathbb{C}\}^2$

$$+\left(\frac{3}{2}MK+\frac{3}{2}M+\frac{5}{2}K+\frac{5}{2}\right)C_{\mathbb{R}\times\mathbb{R}} + \left(\frac{7}{2}MK+\frac{7}{2}M+\frac{7}{2}K+\frac{5}{2}\right)C_{\mathbb{R}+\mathbb{R}} \quad (9)$$

In hardware implementations, the number of gates, and thus the complexity of the multipliers is much greater than that of the delay registers or adders [5]. When also assuming $K \geq 5$, Equation (9) can be approximated by:

$$C_{\mathrm{DPD}} \approx \left(\frac{3}{2}M+\frac{5}{2}\right)KC_{\mathbb{R}\times\mathbb{R}} \quad (10)$$

Regardless of whether the actual hardware implementation might use pipelining or forms of parallelization, the number of multiplications to be performed and the energy per multiplication remain constant, so Equation (10) should apply.

V. DPD POWER CONSUMPTION

DPD power consumption has been investigated in [12] for trade-off for low power cells using a digital signal processing (DSP) processor. For the lowest DPD power consumption, a full-custom CMOS chip in a low-power digital process is desired over FPGA or DSP processor implementations. This best-case scenario is investigated in this section.

Power consumption of a DSP function scales with its complexity. To estimate the power consumption of the full DPD block, the power consumption of a single multiplier $P_{\mathbb{R}\times\mathbb{R}}$ is investigated. DPD power can be found from this and the number of multiplications found in Equation (10):

$$P_{\mathrm{DPD}} \approx \left(\frac{3}{2}M+\frac{5}{2}\right)KP_{\mathbb{R}\times\mathbb{R}} \quad (11)$$

To estimate the power consumption of a multiplier, a benchmark multiplier has been designed. A netlist for 10×10-bit array multiplier for a clock frequency of 1.5 GHz is synthesized from Verilog code in Global Foundries 22 nm FD-SOI CMOS technology. This number of bits still allows for simulations of extracted transistor level circuits. Power consumption for multipliers with a different number of bits can later be estimated from this benchmark. A layout for this multiplier is made, and parasitic extraction for capacitance and cross-capacitance is performed. The extracted multiplier is simulated for 1000 multiplications with random numbers at 1 GHz input data rate. The average power consumption for this multiplier was simulated to be 459 μW. The number of gates of an array multiplier, and therefore its power consumption, is approximately proportional to the number of input bits squared N_{bit}^2. Furthermore, the dynamic power of the multiplier scales with clock frequency f_{clk}. The power consumption for other multipliers in the same process can thus be estimated using a multiplier figure of merit (FoM):

$$P_{\mathbb{R}\times\mathbb{R}} = \mathrm{FoM}_{\mathbb{R}\times\mathbb{R}}N_{\mathrm{bit}}^2 f_{\mathrm{clk}} \quad (12)$$

Using this equation, the FoM for this 22 nm FD-SOI CMOS technology is estimated to be 4.6fJ/bit^2. Although different technology nodes will result in a different $\mathrm{FoM}_{\mathbb{R}\times\mathbb{R}}$, changes in the order of tens of percents result in only minor deviations on the logarithmic power scales.

For a clean spectrum, DPD needs to be performed at the clock frequency after the pulse shaping filter $f_{\mathrm{clk}} = N_{\mathrm{up}}f_{\mathrm{BW}}$, where f_{BW} is the symbol rate and radio frequency bandwidth and N_{up} is the upsampling ratio. The required memory depth M can be found by comparing the slowest memory effect in the TX with this clock frequency. An example could be a supply with a pole frequency of $f_p = 200$ MHz, limited by, e.g., bond wire inductance or closed loop bandwidth of supply regulators. This gives a time constant of $\tau_p = 1/(2\pi f_p) = 0.79$ ns. When the supply is disturbed by a current surge from the PA, its effects will have reduced to 5% in $-\ln(5\%)\tau_p = 2.38$ ns, and memory effects have decreased to insignificant contributions. For this degree of memory effect related compensation, M needs to be chosen as:

$$M = -\frac{\ln(5\%)f_{\mathrm{clk}}}{2\pi f_p} \approx 0.48\frac{N_{\mathrm{up}}f_{\mathrm{BW}}}{f_p} \quad (13)$$

When substituting Equation (11) into Equation (13), the power consumption of the DPD can be estimated to be:

$$P_{\mathrm{DPD}} \approx \left(0.72\frac{N_{\mathrm{up}}f_{\mathrm{BW}}}{f_p}+2.5\right)K\mathrm{FoM}_{\mathbb{R}\times\mathbb{R}}N_{\mathrm{bit}}^2N_{\mathrm{up}}f_{\mathrm{BW}} \quad (14)$$

Current MIMO trends are progressing towards the worst-case scenario for DPD power consumption. Bandwidths are increasing [8], increasing the required f_{BW} and M, while MIMO TXs increase the number of required DPDs blocks [3], [4], [6].

VI. DPD AND PA POWER COMPARISON

Closed-form expressions have been derived for PA array and DPD cell power consumption, in Equation (5) and 14 respectively. To compare the these, an example multi-antenna a short-range TXs are considered with bandwidths of 20MHz and 200MHz, examplary for, e.g., current IEEE 802.11n systems and novel 5G wideband MIMO communication, respectively. DPD is implemented using a memory polynomial DPD. Analysis in [13] demonstrates out-of-band distortion does not average out with increasing n_t, hence a constant $K = 5$ as in [9] is used in all scenarios. Due to the larger bandwidth of the 200 MHz system, it must also have a larger memory depth, as indicated by Equation (13). All other parameters are kept the same. An overview of the simulation parameters is given in Table II. The simulated PA and DPD power consumption versus the number of antennas are

TABLE II
SIMULATION PARAMETERS FOR PA AND DPD POWER COMPARISON

Parameter	20 MHz MIMO	200 MHz MIMO	Unit
f_{BW}	20	200	MHz
N_{up}	8		-
f_p	200		MHz
M	0	3	-
K	5		-
N_{bit}	14		-
$\text{FoM}_{\mathbb{R}\times\mathbb{R}}$	4.6 [c]		fJ/bit^2
EIRP	100		mW
η_{avg}	31		%

[c] For array multipliers in 22 nm FD-SOI technology

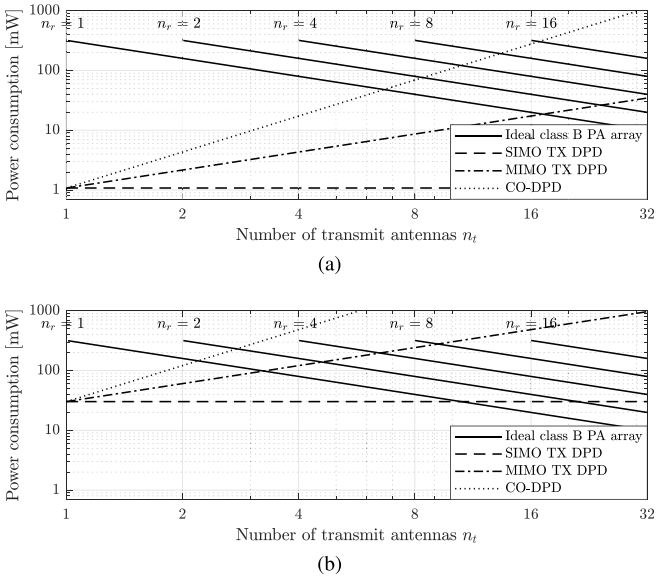

Fig. 6. Comparison of the power consumption for the PA array and its DPD versus the number of antennas n_t for the parameters in Table II. (a) 20 MHz bandwidth. (b) 200 MHz bandwidth.

shown in Figure 6a and Figure 6b for 20 MHz and 200MHz bandwidth, respectively.

In Figure 6a it can be seen that in current 20 MHz bandwidth systems, DPD adds only a minor contribution to the overall power consumption, unless the most complex CO-DPD algorithms and > 6 antennas are used.

For the 200 MHz bandwidth TX, the DPD power consumption is significantly higher due to the increased bandwidth and memory depth. As a consequence, even for the simplest SIMO DPD case the DPD power consumption exceeds the PA power consumption for > 10 antennas for when transmitting to one user. When using complex CO-DPD, the DPD power consumption exceeds the PA array power consumption for all n_t and n_r configurations when $n_t > 3$. DPD power consumption will be even more dominant in cases with bandwidths of up to 1GHz and higher [8], for lower output powers, or when a DSP processor is used instead of dedicated multipliers.

When $P_{\text{DPD}} > P_{\text{PA}}$, less power efficient but more linear PAs can be used, e.g., by increasing back-off, without significant changes to the overall power consumption. If this allows the DPD complexity and therefore power consumption to be reduced, this can have a net benefit to the overall power consumption.

VII. CONCLUSION

A set of analytical expressions was derived for the power consumption of an n_t antenna MIMO PA array and its DPD. The PA array power consumption takes into account beamforming gain and the effect of precoding on PA signal statistics. DPD power was analyzed by deconstructing the memory polynomial to a number of multiplications, and finding the energy per multiplication in digital CMOS circuits. For SIMO TX DPD, only one DPD block is employed in the system, but MIMO TX DPD or CO-DPD require n_t or n_t^2 DPD cells, respectively, increasing the DPD power proportionally. On the other hand, for a given EIRP, the PA power consumption decreases inversely proportional with n_t. Analysis indicates the power consumption of the DPD of a MIMO TX can exceed that of its PAs when the number of antennas increases. For the 200MHz bandwidth scenario in Table II using CO-DPD and one receiving user, this can already happen for $n_t > 2$. For MIMO systems with a large number of antennas and wide bandwidths, system efficiency can become largely dictated by the digital power consumption, rather than the PA power consumption. Hence, for short-range wideband MIMO, it can be beneficial for system efficiency to value PA linearity over PA power efficiency, e.g., by increasing back-off, when this decreases the dominant DPD power consumption.

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