Implementation of Predistortion Circuits via HLS: An Orthogonal Memory polynomial Application

1. PES University, B. tech, ECE, email: pes1ug23ec274@pes.pesu.edu

2. PES University, B. tech, ECE, email: pes1ug23ec277@pes.pesu.edu

3. PES University, B. tech, ECE, email: pes1ug23ec280@pes.pesu.edu

4. PES University, B. tech, ECE, email: pes1ug23ec266@pes.pesu.edu

ABSTRACT:

A simple predistortion linearization model has been implemented on HLS (High-level Synthesis), with performance measured via usual standard methods of NMSE, Spectral Regrowth. Our main aim was to implement the already popular Digital predistortion technique for linearization of the power amplifier output by the newer software method called HLS, where our software code is written in high-level languages (such as C, C++, System C) and the software itself converts this input to the Verilog code that is required for actual hardware implementation, the predistortion model chosen for this implementation was the memory polynomial model which is a very well-known method for linearization and we used the indirect learning approach for this implementation.

Keywords: digital predistortion, High Level Synthesis (HLS), indirect learning

1. INTRODUCTION:

HLS is a newer software that still hasn't matured, its goal is to bridge the gap between high level language coding and hardware specific coding, so that any person with basic C or C++ coding knowledge can leverage this skill to implement real Hardware modules of their liking whilst not having any knowledge of how the written high level code actually gets implemented on the FPGA's or ASICS for which it is designed, hence we have tried to introduce the novelty of using this software to implement and solve a real world problem called distortion in Power Amplifiers. With the widespread use of wireless communication systems and satellite systems, modern communication standards utilize highly complex modulation schemes to increase spectral efficiency. These complex modulation schemes often have nonconstant envelopes that are required to be amplified linearly. Moreover, these modulation schemes often possess very high peak-to average power ratios (PAPR) and necessitate the power amplifier (PA) to be backed off accordingly, which leads to low PA power efficiency [1]. Backoff here means that we need to operate the PA in its linear region of operation. Usually, the power amplifier works in its saturation region to amplify signals (since best amplification is achieved here) but this kind of working leads to heavy distortion in the input signal and hence needs to be avoided. This is why backoff is one of the options since if we back off the PA to work in the linear region we would not significantly distort our incoming signal but the downside as discussed above is that we lose a lot of power for this kind of operation.

Hence, here comes the concept of Digital Predistortion which tries to correct this 'distortion' by applying the inverse of the power amplifier output onto the incoming input signal so that the inverse and the distortion cancel each other, hence rendering a linear signal output from the PA, therefore effectively linearizing the output efficiently without much loss of power.

This paper is divided into 4 sections:

Section I -> Setup and Block Diagram used,

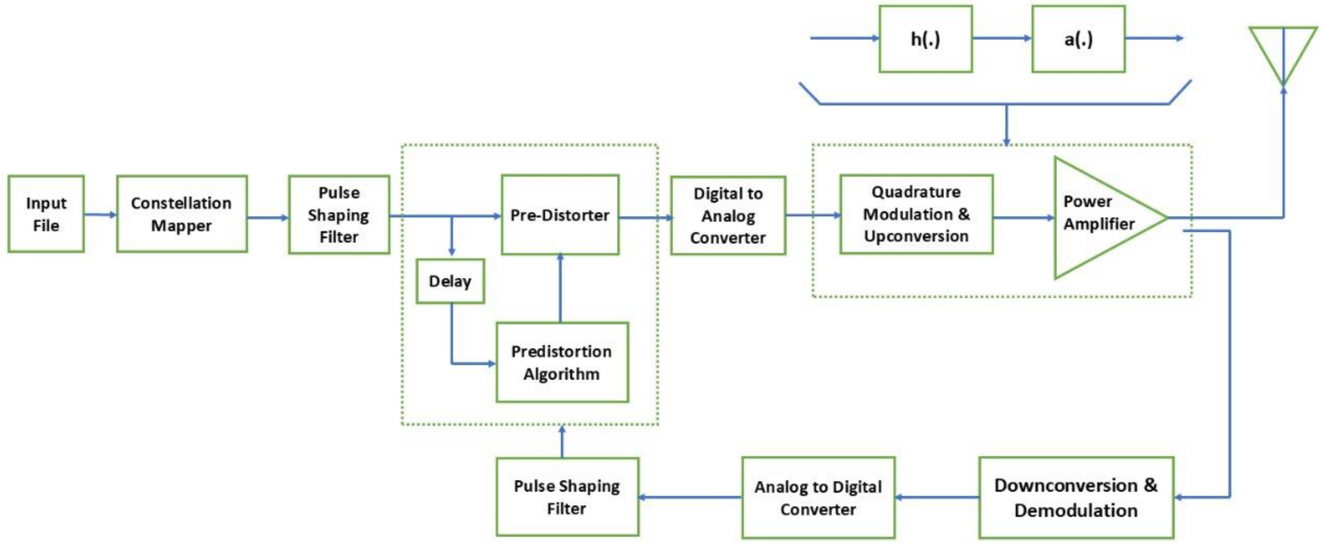
Section 2 -> Digital Predistortion Model,

Section 3 -> Results from Implementing on HLS,

Section 4 -> Conclusions and future prospects.

SECTION 1: The Setup/ Block Diagram used to implement the Digital Predistorter

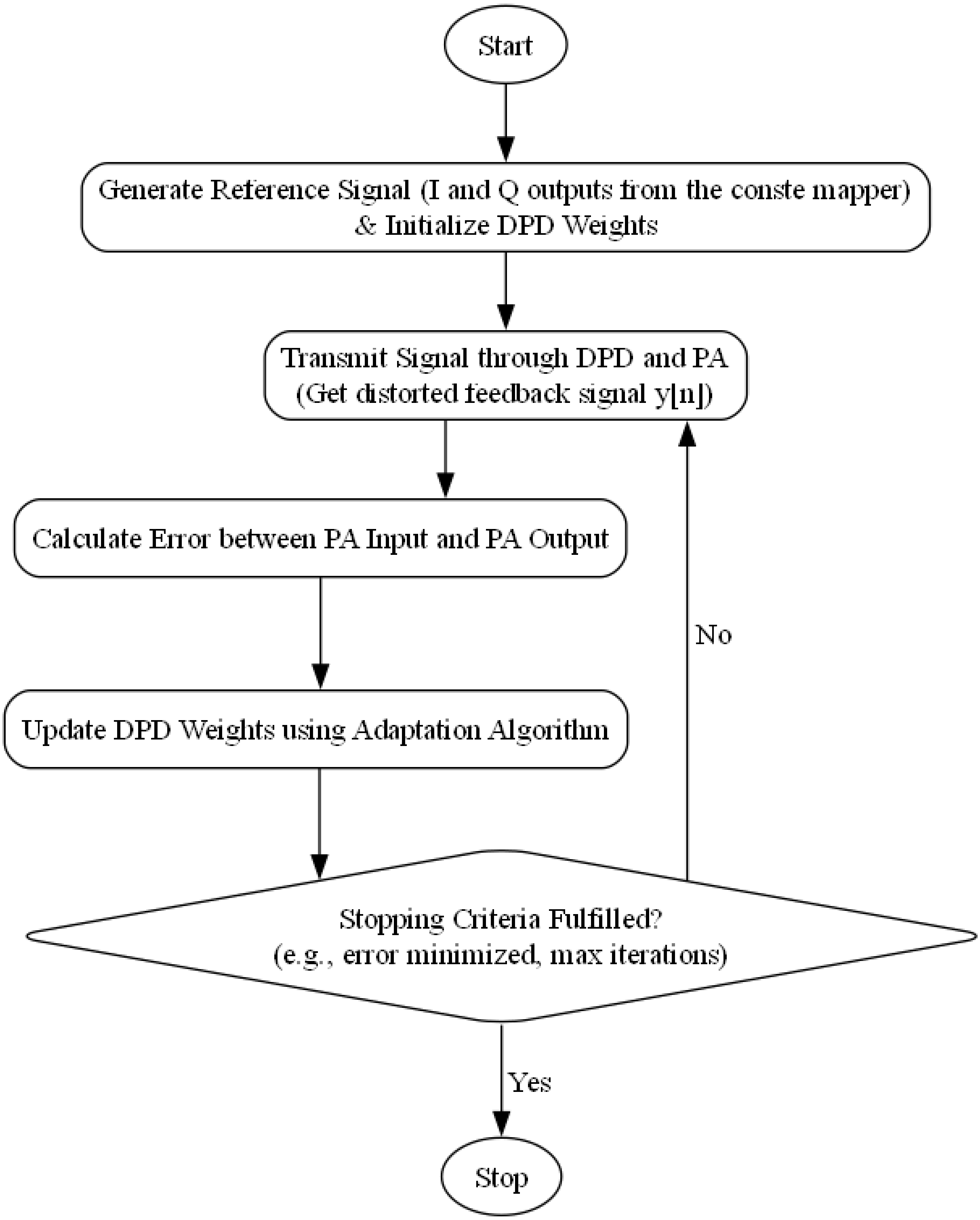
Ref: K. J. Muhonen, M. Kavehrad and R. Krishnamoorthy, "Look-up table techniques for adaptive digital predistortion: a development and comparison," in *IEEE Transactions on Vehicular Technology*, vol. 49, no. 5, pp. 1995-2002, Sept. 2000, doi: 10.1109/25.89260 (page 2, fig 1)



Now, let's briefly look into each of the modules used here:

1) ***Constellation Mapper:*** We use it to convert the incoming binary 1's and 0's to a more quantified/modulated number, basically we follow the Quadrature Phase Shift Keying(QPSK) with gray coding where each pair of the 1's and 0's (like 00, 10, 01, 11) are assigned certain numbers like (00 = 0.7071, 0.7071, 10 = -0.7071, 0.7071, 01 = 0.7071, -0.7071, 11= -0.7071, -0.7071), effectively making two distinct set of numbers which are assigned as I and Q .
2) ***Pulse Shaping Filter (PSF):*** This module is used to basically smoothen out the incoming I's and Q's as abrupt rises and falls do not facilitate in further processing.
3) ***Digital Predistorter Block (DPD):*** The next (first dotted) block is the main DPD module, this is where we use the orthogonal polynomial (Legendre's Technique) in an Indirect learning fashion such that the incoming I's and Q's from the initial PSF are delayed so that the Power amplifiers output can come in and then the algorithm is applied to get the inverse of the PA output which is then multiplied(complex) to the same initial PSF I's and Q's to render a predistorted output from the Pre-distorter module.
4) ***Digital to Analog Converter (DAC):*** This is where the incoming predistorted I's and Q's are prepared to undergo amplification, the first step of which is done here by converting the digital I's and Q's back to its analog form.
5) ***Quadrature Modulator (QM):*** Here the analog I's and Q's are combined by output = I*(cos(alpha))+Q*(sin(alpha)). Therefore producing a real RF signal
6) ***Digital Upconverter (DUC):*** Here the RF signal is upsampled to the same range as power amplifiers input.
7) ***Power Amplifier (PA):*** This is of course the power amplifier with a range of input being [-1,1] and the output range being somewhere like [-8,8], we have implemented the Saleh Amplifier model here as it is a standard in most uses, since the incoming RF signal itself has both the magnitude(I) and the phase(Q) parts within it we give the full RF signal as the input I of the Saleh Amplifier and the Q part input of the PA as 0.
8) ***Digital Downconverter and Modulator (DDC):*** This is the first module in the feedback path where we receive the high frequency output from the PA and demodulate (recover the amplified I's and Q's) and downconvert to facilitate in further processing.
9) ***Analog to Digital Converter (ADC):*** The demodulated I's and Q's are still in their analog form and to actually use them we need them in their digital form hence we use this module to convert then from analog to digital.

FLOW CHART:


Start
Generate Reference Signal (I and Q outputs from the conste mapper)
& Initialize DPD Weights
Transmit Signal through DPD and PA
(Get distorted feedback signal y[n])
Calculate Error between PA Input and PA Output
Update DPD Weights using Adaptation Algorithm
Stopping Criteria Fulfilled?
(e.g., error minimized, max iterations)
No
Yes
Stop

Section 2: The Digital Predistortion Model: we decided to implement the robust yet non-complex model of orthogonal polynomial [2]. DPD based on Volterra polynomials can compensate the nonlinear distortion of HPA. In [3] it is show that a pre-distortion method based on orthogonal polynomials also can resolve the nonlinear distortion problem and the numerical stability is better than those Volterra polynomials based. The model of orthogonal polynomials based DPD is expression in equation [4].

[1] K. -F. Liang, J. -H. Chen and Y. -J. E. Chen, "A Quadratic-Interpolated LUT-Based Digital Predistortion Technique for Cellular Power Amplifiers," in IEEE Transactions on Circuits and Systems II: Express Briefs, vol. 61, no. 3, pp. 133-137, March 2014, doi: https://doi.org/10.1109/TCSII.2013.2296194

[2] H. Huaming, T. Liang, Z. Chunsheng, Y. Bin, Y. Kai and B. Zhiyong, "An adaptive pre-distortion method based on orthogonal polynomials," *Proceedings of the 31st Chinese Control Conference*, Hefei, China, 2012, pp. 5573-5576.

[3] R. Raich, Hua Qian and G. T. Zhou, "Digital baseband predistortion of nonlinear power amplifiers using orthogonal polynomials," *2003 IEEE International Conference on Acoustics, Speech, and Signal Processing, 2003. Proceedings. (ICASSP '03).*, Hong Kong, China, 2003, pp. VI-689, doi: https://doi.org/10.1109/ICASSP.2003.1201775

[4] Shen Jia, Suo Shiqiang, Hu Haijing, Quan Haiyang, Zhao Xunwei, Jiang Yihua. 3GPP long term evolution: principle and system design.Beijing: POSTS & TELECOM PRESS,2008.