KATHMANDU UNIVERSITY

SCHOOL OF ENGINEERING

DEPARTMENT OF ELECTRICAL & ELECTRONICS ENGINEERING

LAB REPORT 01

EEEG-321

Department of Electrical and Electronics Engineering

By:

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To:

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Date:

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Title: Implement Half Adder / Full Adder / Subtraction using VHDL

Requirements: Vivado Software, Laptop

1) Half Adder

VHDL Code

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
entity lab01_56 is
   Port ( A : in STD_LOGIC;
          B : in STD_LOGIC;
          S : out STD_LOGIC;
          C : out STD_LOGIC);
end lab01_56;

architecture Behavioral of lab01_56 is
begin
S <= A XOR B;
C <= A AND B;
end Behavioral;
```

Test Bench code:

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

entity Lab1_56_tb is
--  Port ( );
end Lab1_56_tb;

architecture Behavioral of Lab1_56_tb is
component lab01_56
Port(a: IN std_logic;
b: IN std_logic;
c: OUT std_logic;
s: OUT std_logic);
end component;

signal A: std_logic : = '0';
signal B: std_logic : = '0';
signal C: std_logic : = '0';
signal S: std_logic : = '0';

begin

UUT lab01_56 Port Map (
A => a;
B => b;
S => s;
```

```
C => c);

stimuli : process begin
     wait for 10ns;
     A <= '0';
     B <= '0';
   wait for 10ns;
   A <= '0';
   B <= '1';
   wait for 10ns;
   A <= '1';
   B <= '0';
   wait for 10ns;
   A <= '1';
   B <= '1';
   wait;
end process;
end Behavioral;
```

RTL Schematic Diagram:

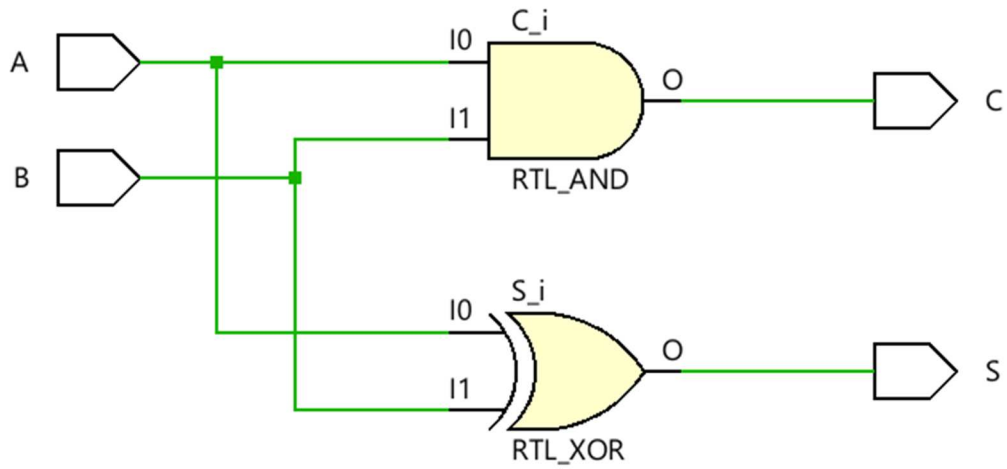

Figure 1: RTL Schematic Diagram

Simulation Model:

Here, A and B are two input signals. S = Sum and C = Carry. The generated waveform for different combinations for input is shown in the figures below.

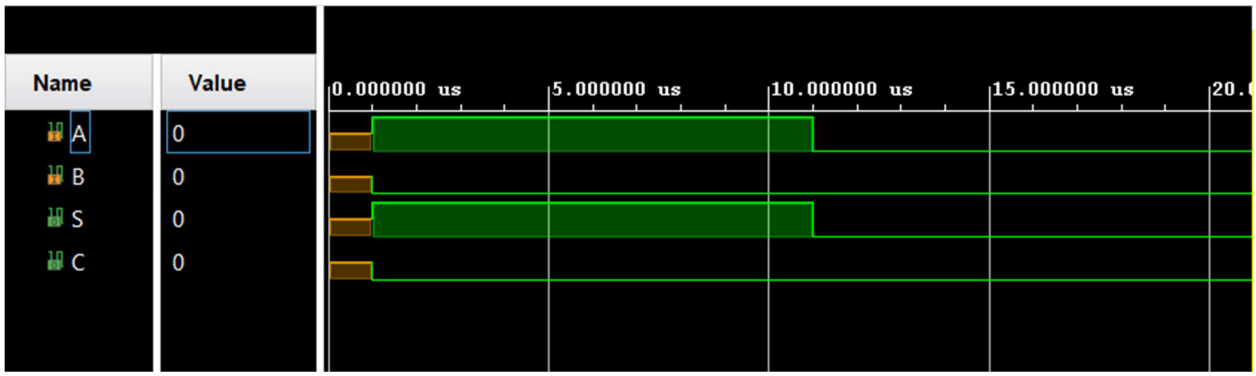

Figure 2: A=0, B=0 S=0, C=0

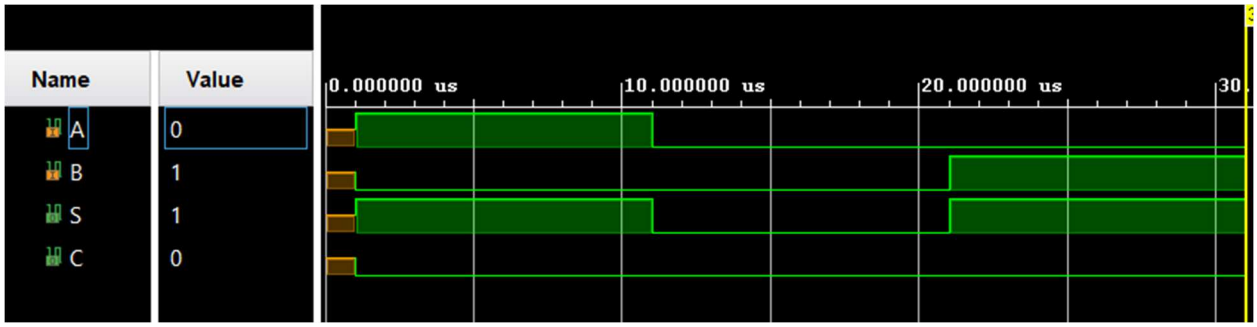

Figure 3: A=0, B=1, S=1, C= 0

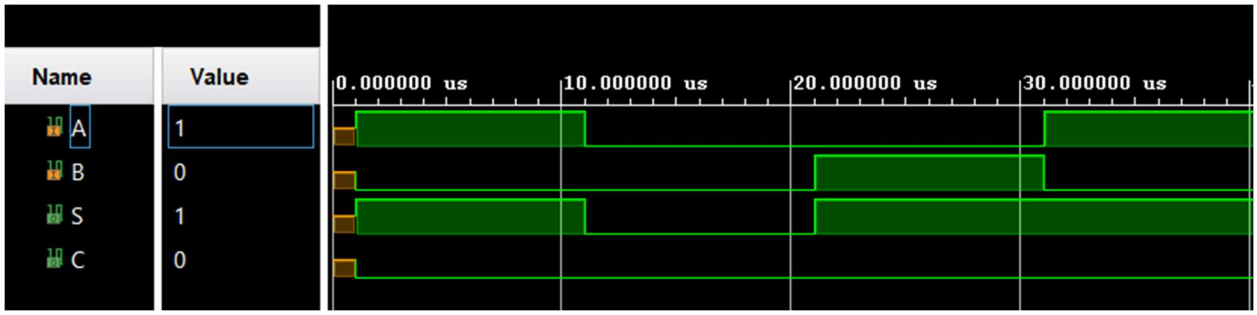

Figure 4: A=1, B= 0, S=1, C=0

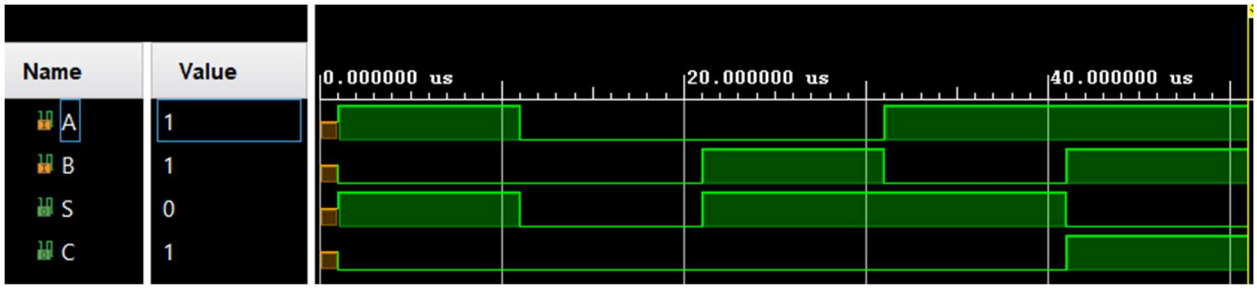

Figure 5: A=1, B=1, S=0, C=1

Device Utilization Report:

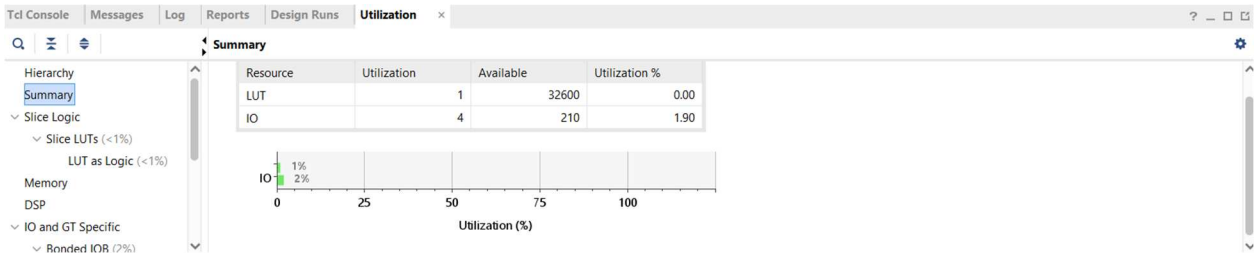

Figure 6: Device Utilization Report

Timing Analysis Report:

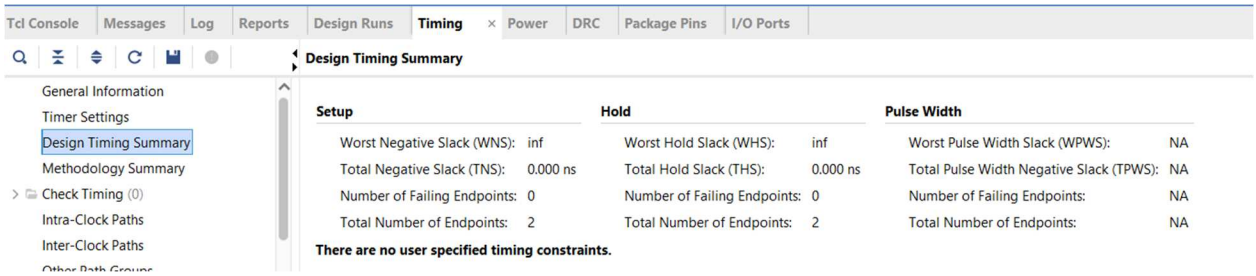

Figure 7: Timing Summary for Half Adder

2) Full Adder

VHDL Code

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

entity fulladder_56 is
    Port ( A : in STD_LOGIC;
           B : in STD_LOGIC;
           C : in STD_LOGIC;
           Carry : out STD_LOGIC;
           Sum : out STD_LOGIC);
end fulladder_56;
```

```
architecture Behavioral of fulladder_56 is

begin
Sum <= A XOR (B XOR C);
Carry <= (A and B) OR (B and C) OR (A and C);
end Behavioral;
```

Test Bench Code

```
library IEEE;
use IEEE.Std_logic_1164.all;
use IEEE.Numeric_Std.all;
entity fulladder_56_tb is
end;

architecture bench of fulladder_56_tb is

  component fulladder_56
     Port ( A : in STD_LOGIC;
          B : in STD_LOGIC;
          C : in STD_LOGIC;
          Carry : out STD_LOGIC;
          Sum : out STD_LOGIC);
  end component;

  signal A: STD_LOGIC;
  signal B: STD_LOGIC;
  signal C: STD_LOGIC;
  signal Carry: STD_LOGIC;
  signal Sum: STD_LOGIC;

begin

  uut: fulladder_56 port map ( A     => A,
                       B     => B,
                       C     => C,
                       Carry => Carry,
                       Sum   => Sum );

  stimulus: process
  begin
  a<= '0';
  b <= '0';
  c<= '0';
  wait for 10ns;
  a<= '0';
  b <= '0';
  c<= '1';
```

```
wait for 10ns;
a<= '0';
b <= '1';
c<= '0';
wait for 10ns;
a<= '0';
b <= '0';
c<= '1';
wait for 10ns;
a<= '1';
b <= '0';
c<= '0';
wait for 10ns;
a<= '1';
b <= '0';
c<= '1';
wait for 10ns;
a<= '1';
b <= '1';
c<= '0';
wait for 10ns;
a<= '1';
b <= '1';
c<= '1';
wait for 10ns;
  wait;
 end process;
end;
```

RTL Schematic

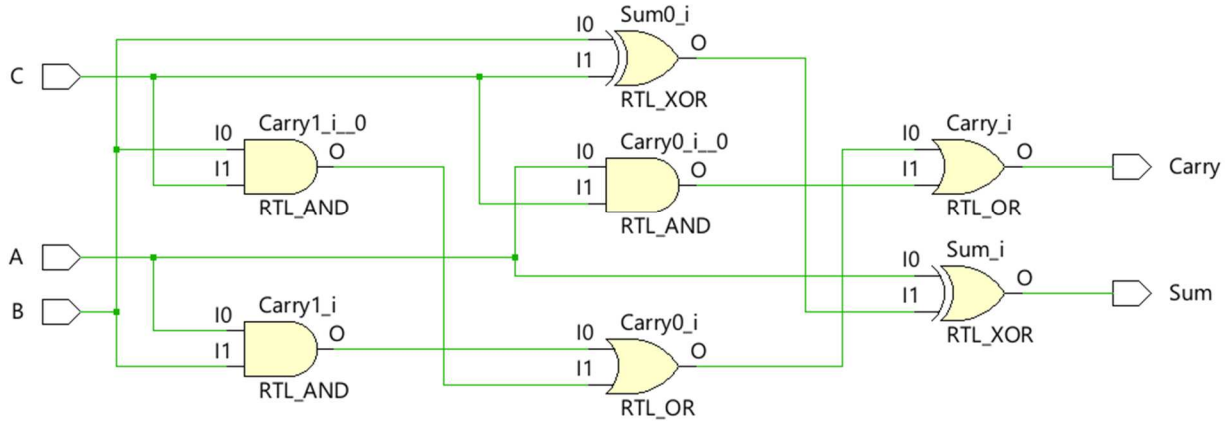

Figure 8: RTL Schematic of Full Adder

Simulation

The timing waveform graph for different possible combinations of input is given in the figure below. In a test-bench code, the different input combination was given and also the wait instruction for 10ns. So, while simulating, all the output can be seen in a single figure.

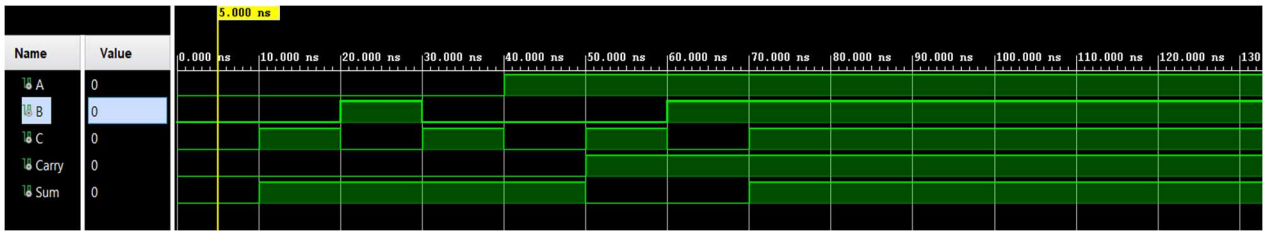

Figure 9: Timing Diagram for all the possible input combinations for full adder

Device Utilization Report

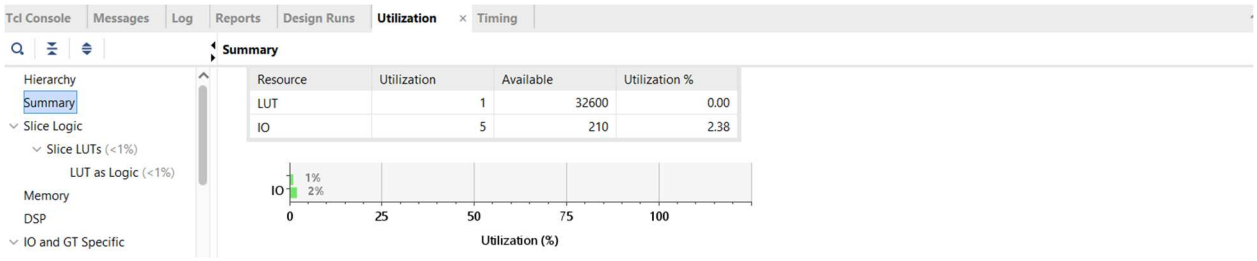

Figure 10: Device Utilization Report

Time Analysis Report

Design Timing Summary

Setup		Hold		Pulse Width	
Worst Negative Slack (WNS):	inf	Worst Hold Slack (WHS):	inf	Worst Pulse Width Slack (WPWS):	NA
Total Negative Slack (TNS):	0.000 ns	Total Hold Slack (THS):	0.000 ns	Total Pulse Width Negative Slack (TPWS):	NA
Number of Failing Endpoints:	0	Number of Failing Endpoints:	0	Number of Failing Endpoints:	NA
Total Number of Endpoints:	2	Total Number of Endpoints:	2	Total Number of Endpoints:	NA

There are no user specified timing constraints.

Figure 11: Timing Summary for Full Adder

3) Half Subtractor

VHDL Code:

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

entity halfsubtractor_56 is
```

```
   Port ( A : in STD_LOGIC;
          B : in STD_LOGIC;
          Diff : out STD_LOGIC;
          Borrow : out STD_LOGIC);
end halfsubtractor_56;

architecture Behavioral of halfsubtractor_56 is

begin
Diff <= A XOR B;
Borrow <= (NOT A) AND B;
end Behavioral;
```

Test-bench Code:

```
library IEEE;
use IEEE.Std_logic_1164.all;
use IEEE.Numeric_Std.all;

entity halfsubtractor_56_tb is
end;

architecture bench of halfsubtractor_56_tb is

  component halfsubtractor_56
     Port ( A : in STD_LOGIC;
            B : in STD_LOGIC;
            Diff : out STD_LOGIC;
            Borrow : out STD_LOGIC);
  end component;

  signal A: STD_LOGIC;
  signal B: STD_LOGIC;
  signal Diff: STD_LOGIC;
  signal Borrow: STD_LOGIC;

begin
  uut: halfsubtractor_56 port map ( A      => A,
                                    B      => B,
                                    Diff   => Diff,
                                    Borrow => Borrow );

  stimulus: process
  begin
  a<= '0';
  b<= '0';
  wait for 10ns;
  a<= '0';
  b<= '0';
  wait for 10ns;
   a<= '0';
```

```
    b<= '0';
    wait for 10ns;
    a<= '0';
    b<= '0';
    wait for 10ns;
      wait;
    end process;
end;
```

Simulation Model

Here in the waveform, for the input signal A and B = 0, the difference and borrow is also 0.

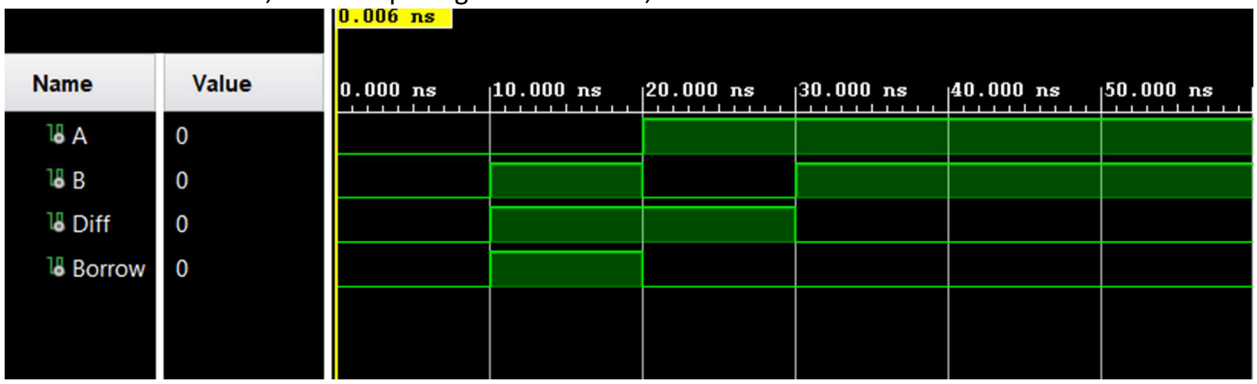

Figure 12: Simulation Diagram for Half Subtractor

RTL Schematic

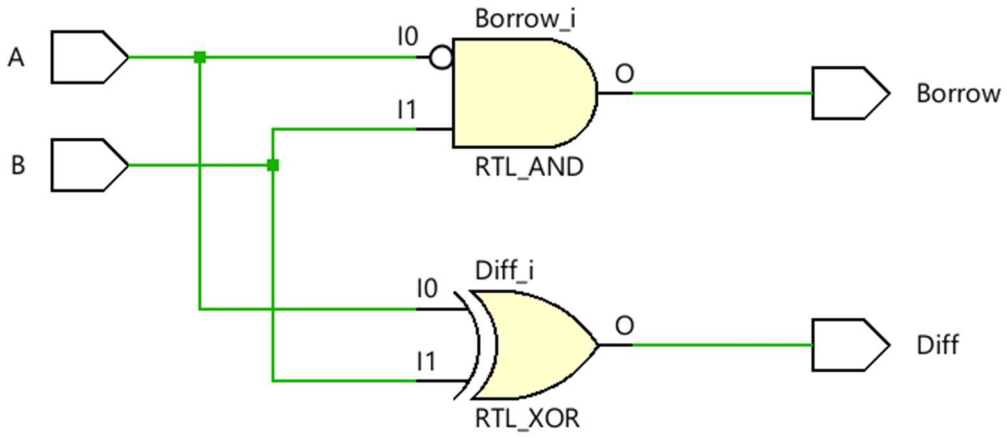

Figure 13: RTL Schematic for Half Subtractor

Device Utilization Report

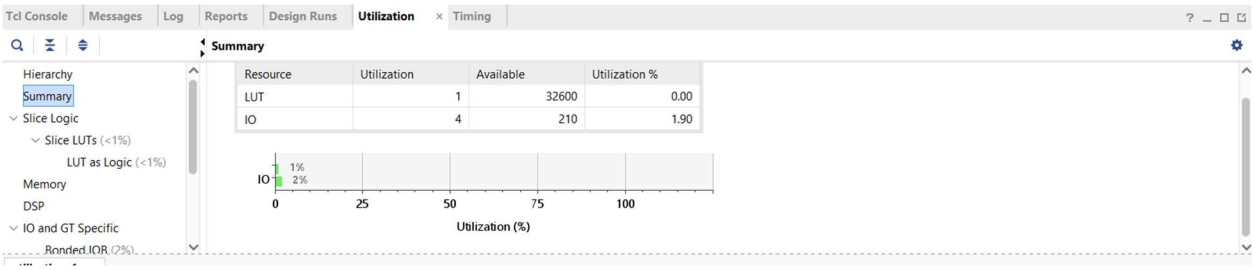

Figure 14: Utilization Report for Half Subtractor

Time Analysis Report

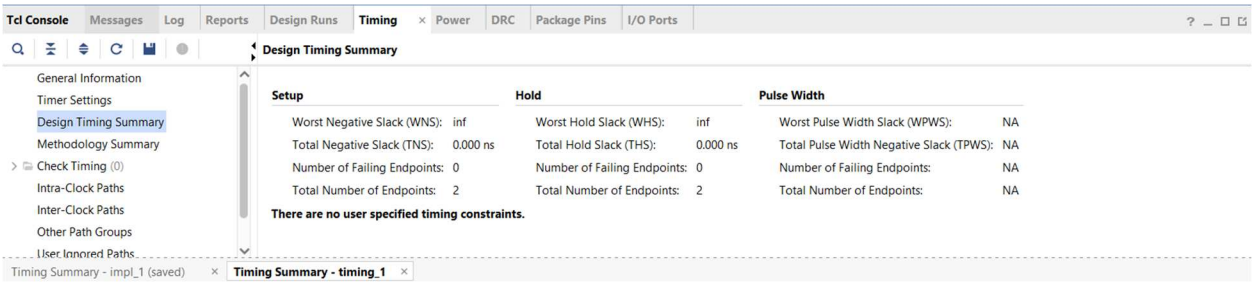

Figure 15: Timing Summary for Half Subtractor