KATHMANDU UNIVERSITY

School of Engineering

Department of Electrical & Electronics Engineering

EEEG-321: Digital Circuit and Systems Laboratory Work

Lab-III

Submitted by:

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Year III, Semester II

Submitted to:

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Department of Electrical & Electronics Engineering

Date: 7th May, 2024

Title: Implementation of 4-bit Adder Using 1-bit Adder

Requirements: Vivado Software

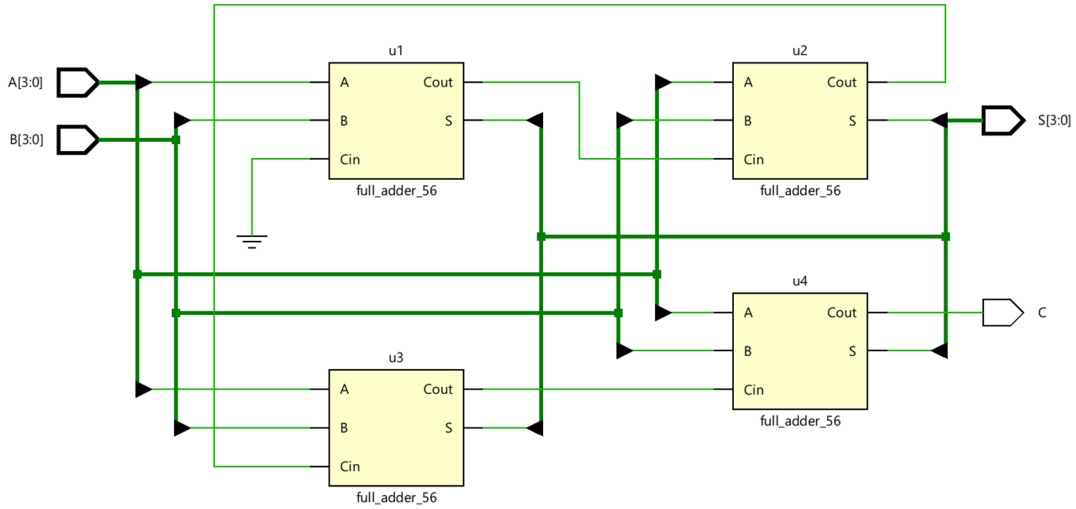
VHDL Code:

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
entity four_bit_full_adder_56 is
Port(A: in std_logic_vector(3 downto 0); B:
    in std_logic_vector(3 downto 0); S: out
    std_logic_vector(3 downto 0); C: out
    std_logic);
end four_bit_full_adder_56;
architecture Behavioral of four_bit_full_adder_56 is component
full_adder_56 Port(
A: in std_logic;
B: in std_logic;
Cin: in std_logic;
S: out std_logic;
Cout: out std_logic);
End component;
signal carry: std_logic_vector(2 downto 0);
begin
u1: full_adder_56 port map(A=>A(0), B=>B(0), Cin=>'0', S=>S(0), Cout=>Carry(0));
u2: full_adder_56 port map(A=>A(1), B=>B(1), Cin=> Carry(0), S=>S(1), Cout=>Carry(1)); u3:
full_adder_56 port map(A=>A(2), B=>B(2), cin=> Carry(1), S=>S(2), Cout=>Carry(2)); u4:
full_adder_56 port map(A=>A(3), B=>B(3), Cin=>Carry(2), S=>S(3), Cout=>C);
end Behavioral;
```

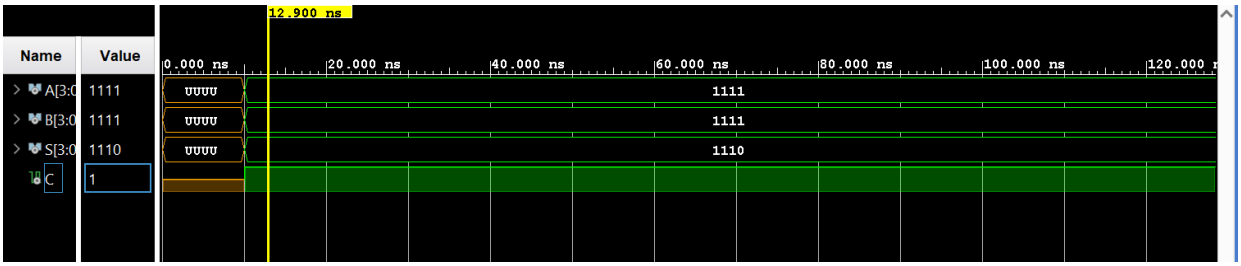
TestBench code:

```
library IEEE;
use IEEE.std_logic_1164.all; use

IEEE.numeric_std.all;

entity four_bit_full_adder_56_tb is end;

architecture behavioral of four_bit_full_adder_56_tb is component

four_bit_full_adder_56

Port(A: in std_logic_vector(3 downto 0);

B: in std_logic_vector(3 downto 0);

S: out std_logic_vector(3 downto 0);

C: out std_logic);

end component;
signal A: std_logic_vector(3 downto 0);

signal B: std_logic_vector(3 downto 0);

signal S: std_logic_vector(3 downto 0);

signal C: std_logic;

begin
uut: four_bit_full_adder_56 port map(A=>A, B=>B, S=>S, C=>C); stimulus:

process begin

wait for 10 ns;
A<="1111";
B<="1111";
wait;
end process;

end;
```

RTL Schematic Diagram:

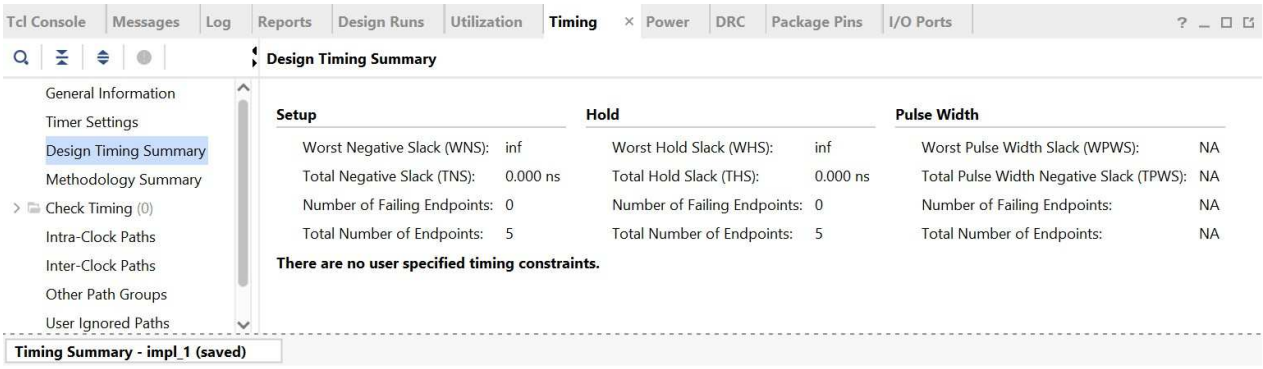


Simulation Model:



Device Utilization Report:

Time Analysis Report:



XDC File:

set_property PACKAGE_PIN J15 [get_ports {A[3]}] set_property PACKAGE_PIN L16 [get_ports {A[2]}] set_property PACKAGE_PIN M13 [get_ports {A[1]}] set_property PACKAGE_PIN R15 [get_ports {A[0]}] set_property IOSTANDARD LVCMOS33 [get_ports {A[3]}] set_property IOSTANDARD LVCMOS33 [get_ports {A[2]}] set_property IOSTANDARD LVCMOS33 [get_ports {A[1]}] set_property IOSTANDARD LVCMOS33 [get_ports {A[0]}] set_property PACKAGE_PIN R17 [get_ports {B[3]}] set_property PACKAGE_PIN T18 [get_ports {B[2]}] set_property PACKAGE_PIN U18 [get_ports {B[1]}]

set_property PACKAGE_PIN R13 [get_ports {B[0]}] set_property

IOSTANDARD LVCMOS33 [get_ports {B[3]}] set_property IOSTANDARD

LVCMOS33 [get_ports {B[2]}] set_property IOSTANDARD LVCMOS33

[get_ports {B[1]}] set_property IOSTANDARD LVCMOS33 [get_ports {B[0]}]

set_property IOSTANDARD LVCMOS33 [get_ports {S[3]}] set_property

IOSTANDARD LVCMOS33 [get_ports {S[2]}] set_property IOSTANDARD

LVCMOS33 [get_ports {S[1]}] set_property IOSTANDARD LVCMOS33

[get_ports {S[0]}]

Title: Implementation of four bit adder and subtractor in VHDL

VHDL Code:

```
library IEEE;
use IEEE.std_logic_1164.ALL;
entity four_bit_adder_and_subtractor_56 is

port (A: in std_logic_vector(3 downto 0); B: in

std_logic_vector(3 downto 0);

M: in std_logic;
S: out std_logic_vector(3 downto 0); Cout:

out std_logic);

end entity;
architecture Behavioral of four_bit_adder_and_subtractor_56 is component

full_adder_56 is

port (A:in std_logic;
B: in std_logic;
Cin: in std_logic;
S: out std_logic;
Cout: out std_logic);
```

end component;

signal B3: std_logic;

signal B2: std_logic;

signal B1: std_logic;

signal B0: std_logic;

signal Carry: std_logic_vector (2 downto 0); begin

B3 <= B(3) xor M;

B2 <= B(2) xor M;

B1 <= B(1) xor M;

B0 <= B(0) xor M;

u1: full_adder_56 port map (A=>A(0), B=>B0, Cin=>M, S=>S(0),Cout=>Carry(0)); u2:full_adder_56

port map (A=>A(1), B=>B1, Cin=>Carry(0), S=>S(1),Cout=>Carry(1)); u3:full_adder_56 port map

(A=>A(2), B=>B2, Cin=>Carry(1), S=>S(2),Cout=>Carry(2)); u4:full_adder_56 port map (A=>A(3),

B=>B3, Cin=>Carry(2), S=>S(3),Cout=>Cout); end Behavioral;

TestBench Code:

library IEEE;
use IEEE.std_logic_1164.all; use

IEEE.numeric_std.all;

entity four_bit_adder_and_subtractor_56_tb is end;

architecture bench of four_bit_adder_and_subtractor_56_tb is

component four_bit_adder_and_subtractor_56

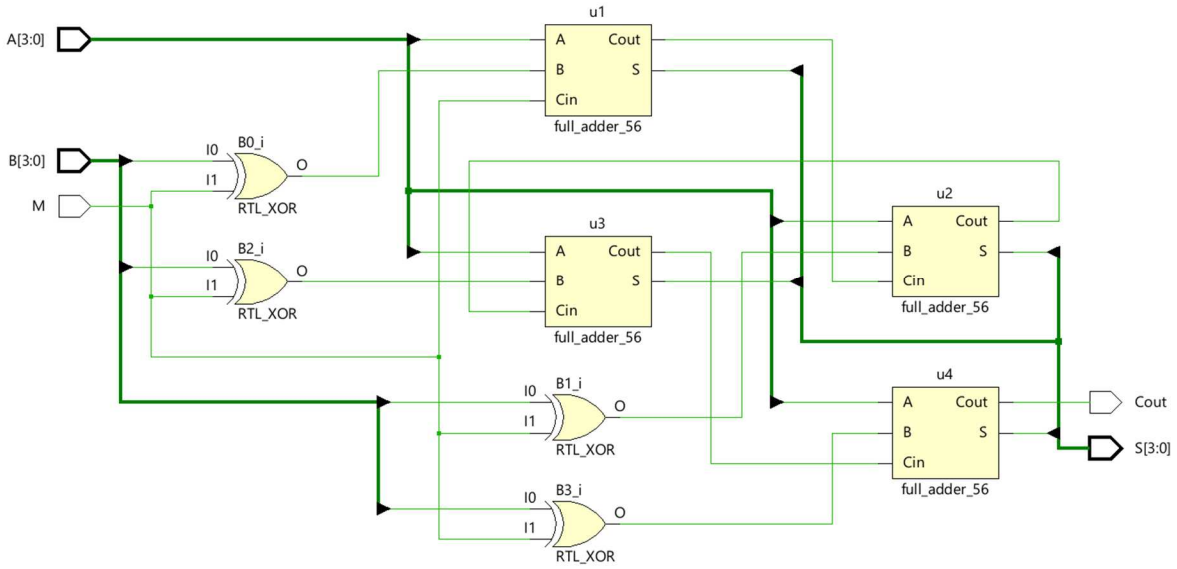
port (A: in std_logic_vector(3 downto 0); B: in

std_logic_vector(3 downto 0);

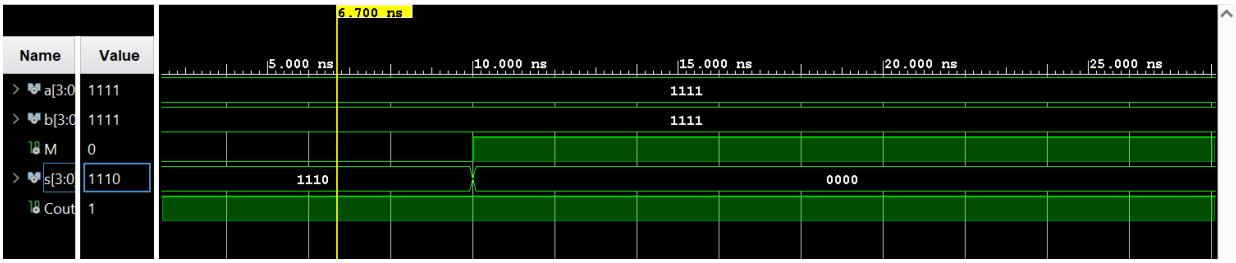
M: in std_logic;

```
S:  out  std_logic_vector(3  downto  0);

Cout: out std_logic);

end component;
signal  A:  std_logic_vector(3  downto  0);

signal  B:  std_logic_vector(3  downto  0);

signal M: std_logic;

signal  S:  std_logic_vector(3  downto  0);

signal Cout: std_logic;

begin
uut: four_bit_adder_and_subtractor_56 port map (a =>a, b => b, M => M, s => s, Cout => Cout
);
stimulus: process

begin A<="1111";

B<="1111";

M<='0';

wait for 10 ns;
A<="1111";
B<="1111";
M<='1';
wait for 10 ns;

wait;

end process;

end;
```

RTL Schematic Diagram:

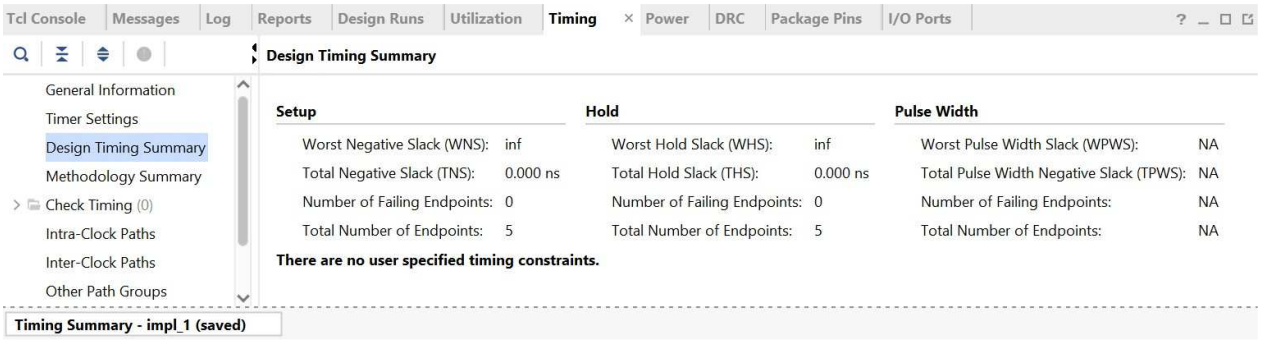


Simulation Model:



Device Utilization Report:

Time Analysis Report:



XDC File:

set_property PACKAGE_PIN J15 [get_ports {A[3]}] set_property PACKAGE_PIN L16 [get_ports {A[2]}] set_property PACKAGE_PIN M13 [get_ports {A[1]}] set_property PACKAGE_PIN R15 [get_ports {A[0]}] set_property IOSTANDARD LVCMOS33 [get_ports {A[3]}] set_property IOSTANDARD LVCMOS33 [get_ports {A[2]}] set_property IOSTANDARD LVCMOS33 [get_ports {A[1]}] set_property IOSTANDARD LVCMOS33 [get_ports {A[0]}] set_property PACKAGE_PIN R17 [get_ports {B[3]}] set_property PACKAGE_PIN T18 [get_ports {B[2]}]

set_property PACKAGE_PIN U18 [get_ports {B[1]}] set_property

PACKAGE_PIN R13 [get_ports {B[0]}] set_property IOSTANDARD

LVCMOS33 [get_ports {B[3]}] set_property IOSTANDARD LVCMOS33

[get_ports {B[2]}] set_property IOSTANDARD LVCMOS33 [get_ports

{B[1]}] set_property IOSTANDARD LVCMOS33 [get_ports {B[0]}]

set_property IOSTANDARD LVCMOS33 [get_ports {S[3]}] set_property

IOSTANDARD LVCMOS33 [get_ports {S[2]}] set_property IOSTANDARD

LVCMOS33 [get_ports {S[1]}] set_property IOSTANDARD LVCMOS33

[get_ports {S[0]}] set_property PACKAGE_PIN U13 [get_ports {S[3]}]

set_property PACKAGE_PIN T9 [get_ports {S[2]}] set_property

PACKAGE_PIN T10 [get_ports {S[1]}] set_property PACKAGE_PIN R10

[get_ports {S[0]}] set_property PACKAGE_PIN H17 [get_ports Cout]

set_property PACKAGE_PIN V10 [get_ports M] set_property

IOSTANDARD LVCMOS33 [get_ports Cout] set_property IOSTANDARD

LVCMOS33 [get_ports M]

Title: Implementation of 4-bit Subtractor using 1-bit Subtractor

VHDL Code:

```
library IEEE;
use IEEE.std_logic_1164.all;
entity four_bit_full_subtractor_56 is
port( A: in std_logic_vector( 3 downto 0); B: in
    std_logic_vector(3 downto 0); D: out
    std_logic_vector(3 downto 0); Bout: out
    std_logic);
```

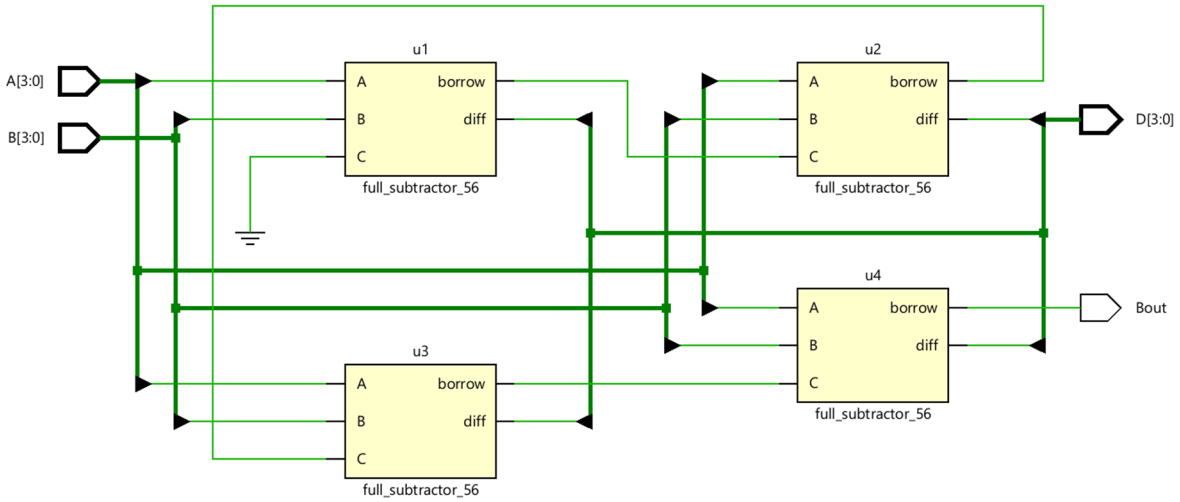
```
end entity;
architecture behavioral of four_bit_full_subtractor_56 is component

full_subtractor_56

port( A : in STD_LOGIC;
      B : in STD_LOGIC;
      C : in STD_LOGIC;
      diff : out STD_LOGIC; borrow : out

      STD_LOGIC);

end component;
signal borr: std_logic_vector(2 downto 0); begin

u1: full_subtractor_56 port map(A=>A(0), B=>B(0), C=>'0', diff=>D(0), borrow=>borr(0));
u2: full_subtractor_56 port map(A=>A(1), B=>B(1), C=>borr(0), diff=>D(1), borrow=>borr(1));

u3: full_subtractor_56 port map(A=>A(2), B=>B(2), C=>borr(1), diff=>D(2), borrow=>borr(2));

 u4: full_subtractor_56 port map(A=>A(3), B=>B(3), C=>borr(2), diff=>D(3), borrow=>Bout);

 end behavioral;
```

TestBench Code:

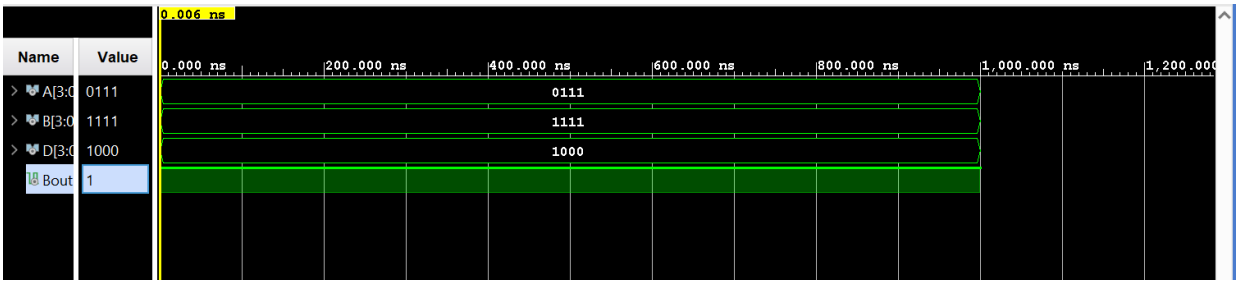
```
library IEEE;
use IEEE.std_logic_1164.all; use

IEEE.numeric_std.all;

entity four_bit_full_subtractor_56_tb is end;

architecture behavioral of four_bit_full_subtractor_56_tb is component

four_bit_full_subtractor_56

port( A: in std_logic_vector( 3 downto 0);

B: in std_logic_vector(3 downto 0);

D: out std_logic_vector(3 downto 0);
```

```
        Bout: out std_logic);
        end component;
signal A: std_logic_vector( 3 downto 0); signal B:
std_logic_vector(3 downto 0); signal D:
std_logic_vector(3 downto 0); signal Bout:
std_logic;
begin
uut: four_bit_full_subtractor_56 port map ( A => A,B => B, D => D,Bout => Bout); stimulus: process
begin A<="0111";
B<="1111";
wait for 10 ns;
wait;
end process;
end behavioral;
```

RTL Schematic Diagram:



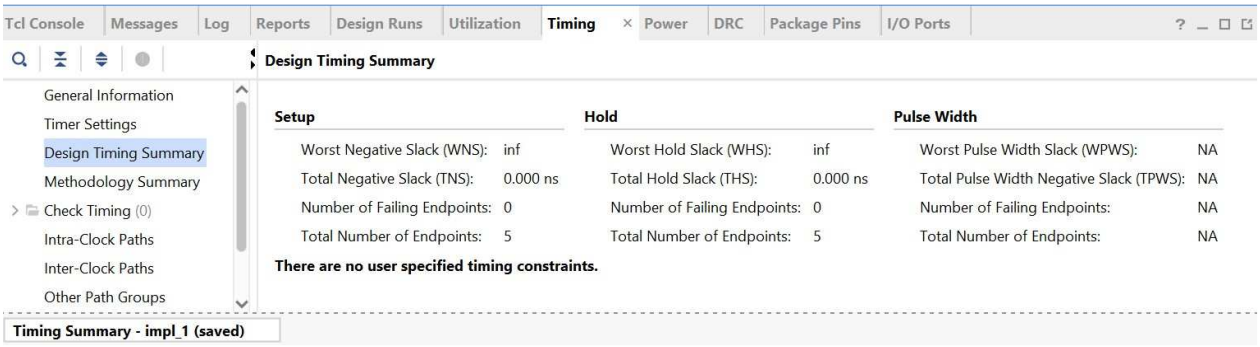
Simulation Model:



Device Utilization Report:

Slice LUTs (32600)	Slice (8150)	LUT as Logic (32600)	Bonded IOB (210)
4	1	4	13

Time Analysis Report:



XDC File:

set_property PACKAGE_PIN U11 [get_ports {D[3]}] set_property PACKAGE_PIN U12 [get_ports {D[2]}] set_property PACKAGE_PIN V12 [get_ports {D[1]}] set_property PACKAGE_PIN V10 [get_ports {D[0]}] set_property IOSTANDARD LVCMOS33 [get_ports {A[3]}] set_property IOSTANDARD LVCMOS33 [get_ports {A[2]}] set_property IOSTANDARD LVCMOS33 [get_ports {A[1]}] set_property IOSTANDARD LVCMOS33 [get_ports {A[0]}] set_property PACKAGE_PIN J15 [get_ports {A[3]}] set_property PACKAGE_PIN L16 [get_ports {A[2]}] set_property PACKAGE_PIN M13 [get_ports {A[1]}]

set_property PACKAGE_PIN R15 [get_ports {A[0]}] set_property IOSTANDARD LVCMOS33 [get_ports {B[3]}] set_property IOSTANDARD LVCMOS33 [get_ports {B[2]}] set_property IOSTANDARD LVCMOS33 [get_ports {B[1]}] set_property IOSTANDARD LVCMOS33 [get_ports {B[0]}] set_property PACKAGE_PIN R17 [get_ports {B[3]}] set_property PACKAGE_PIN T18 [get_ports {B[2]}] set_property PACKAGE_PIN U18 [get_ports {B[1]}] set_property PACKAGE_PIN R13 [get_ports {B[0]}] set_property IOSTANDARD LVCMOS33 [get_ports {D[3]}] set_property IOSTANDARD LVCMOS33 [get_ports {D[2]}] set_property IOSTANDARD LVCMOS33 [get_ports {D[1]}] set_property IOSTANDARD LVCMOS33 [get_ports {D[0]}]

Conclusion:

Through the lab work, a comprehension of structured programming was gained. Employing the full-adder constructed in lab1 as a foundational example, a four-bit adder was developed in the initial code. This involved acquiring the RTL schematic diagram and crafting a dedicated simulation file to script the test-bench code. Building upon these principles, the subsequent task enabled user interaction, granting the option to utilize the circuit as either a four-bit adder or subtractor based on the value of 'M'. When 'M' equaled 1, subtraction was executed; conversely, addition occurred when 'M' equaled 0. The subtraction operation was implemented by adding one to the 2s complement of the second number, leveraging binary arithmetic principles. Pin assignments for inputs and outputs were established to generate XDC files for both functionalities, facilitating code deployment on the board. Additionally, by extending the logic akin to the four-bit adder, four 1-bit subtractors were integrated to form a 4-bit subtractor. Rigorous simulation testing was conducted across various input values to validate the functionality of the designed models.