FSMDesignTest Documentation

2017

Introduction

All the processes involved in the design and manufacture of any electronic system are subject to error. Checking that the product has been correctly built (manufacturing test) is an essential part of the production process. The generation of test patterns for manufacturing test can be difficult even for quite simple circuits, but the difficulties can be minimised by applying the principles of design for testability (DFT).

The project aims to show how DFT structures can be built into an integrated circuit (IC) to assist testing via a scan path. Fault detection and analysis can be done. Stuck-at-0/1 implemented.

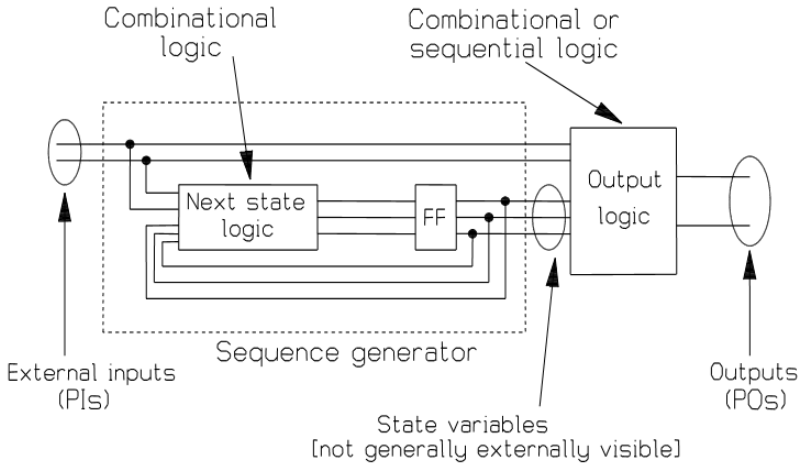

FIGURE 1: General Finite State Machine

The main problem in testing is the access (or lack of it) to the internal nodes of the circuit; the main point of DFT is to provide means for improving this access.

The pin allocation is designed to work with CycloneV FPGA. If using another FPGA/CPLD please note the changes needed by the pin sheet documentation.

The code can be synthesised, and the board programmed with a tool as Quartus.

FSM Design

The FSM of Figure 2 is extended by adding the combinational logic block shown in Figure 3 at the outputs. We now have an additional Primary Input (PI) (B). The Primary Outputs (POs) are now K and L. S and T are no longer POs and cannot be directly observed. the FSM developed (Figure 2+3) is further extended by adding the output circuitry indicated in Figure 5, we

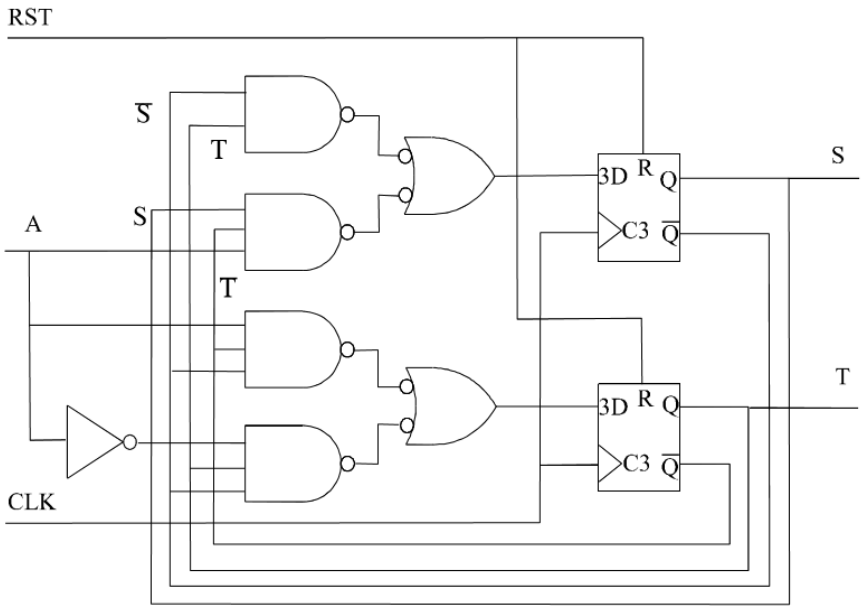

FIGURE 2: Basic FSM

have introduced an additional PI, C, and PO, N instead of the original POs, T and S1.

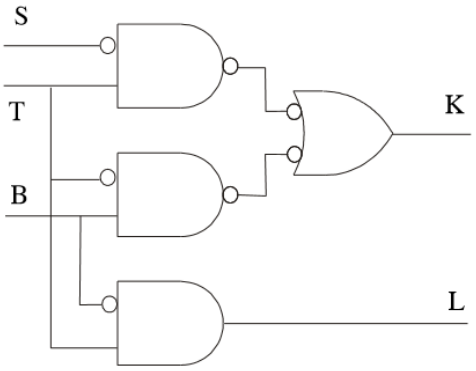

FIGURE 3: Additional combinational output logic

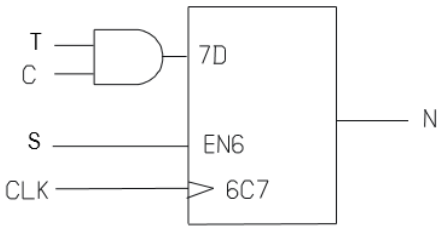

FIGURE 5: Additional sequential output logic

Scan Path Design

Multiplexers (MUX) are inserted in front of each flip-flop. This allows each flip-flop to take one of two signals.

The mode input (M) is a required additional PI to the circuit. When M = 0, the circuit is in its normal operating condition; when M = 1, the circuit is in scan mode. Scan mode means that the flip-flops are all connected together to form a shift register or scan path. (iii) The scan path allows the state of each flip-flop to be set, regardless of the behaviour of the FSM. We simply set M = 1 and clock in the values we want. We would then set M = 0, to allow the FSM to move to the next state. Similarly, we can read out the state that we're in by setting M = 1 again and clocking the flip-flop values out through SDI.

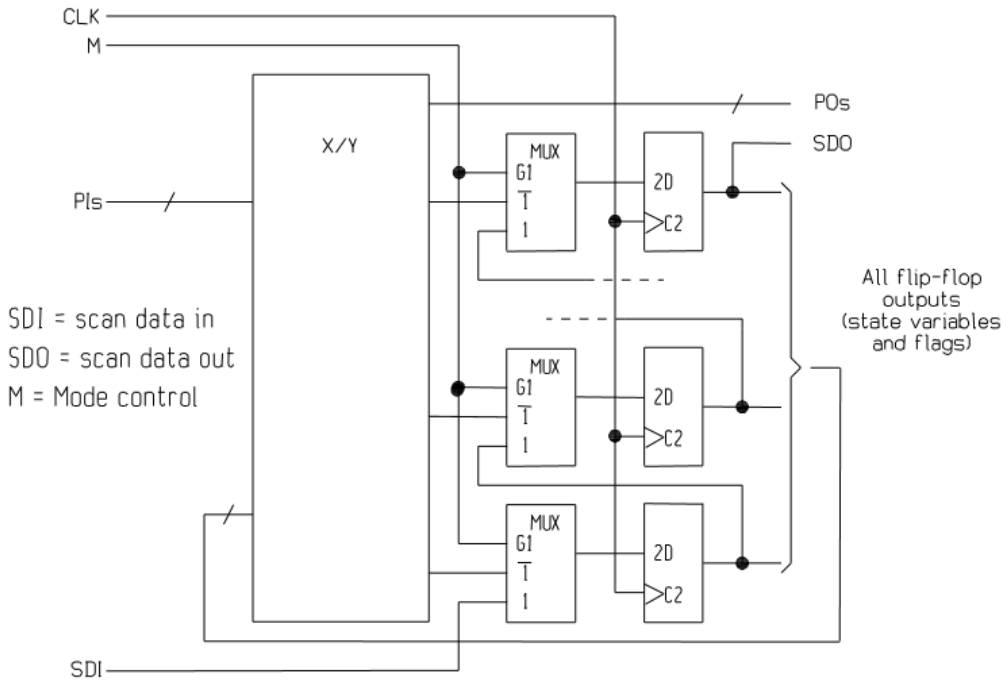

FIGURE 6: General scan path model

Reference: Material taken from Digital System & Signal Processing, c4 Lab by Mark Zwolinski, Electronics & Computer Science, University of Southampton