VLSI 8-Bit Divider Datapath System Design

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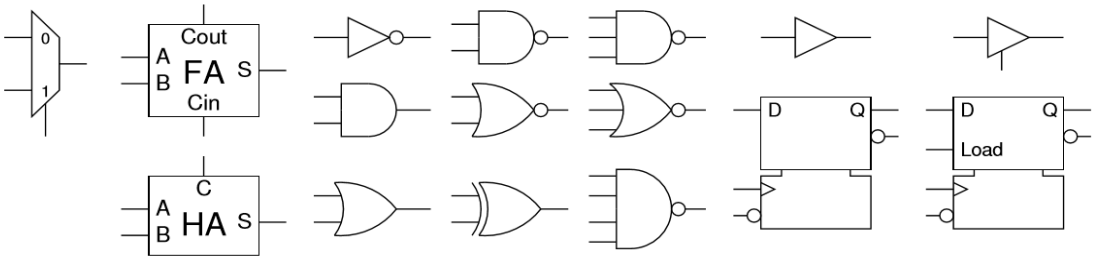
Custom implementation of an 8-bit divider datapath architecture using bitslice technique and a synthesizable SystemVerilog control unit.

Custom-designed Cell Library is used for synthesis.

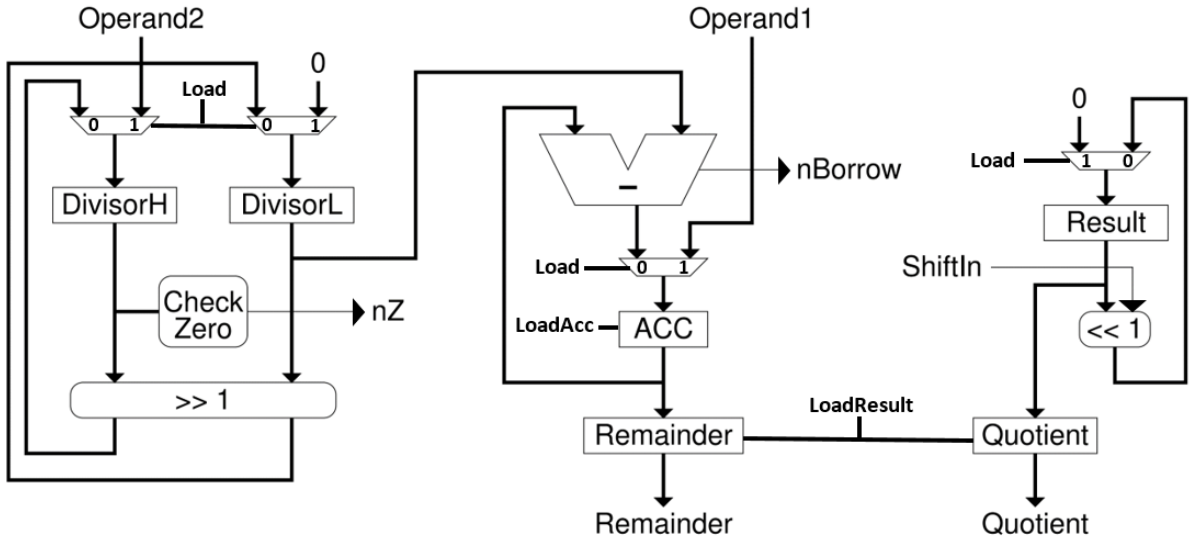
Cell library[1]



- Combinational Cells — `mux2 fulladder halfadder inv and2 or2 nand2 nor2 xor2 nand3 nor3 nand4 buffer trisbuf`
- Sequential Cells — `scandtype scanreg`

Divider Architecture

Divider Datapath Architecture Diagram

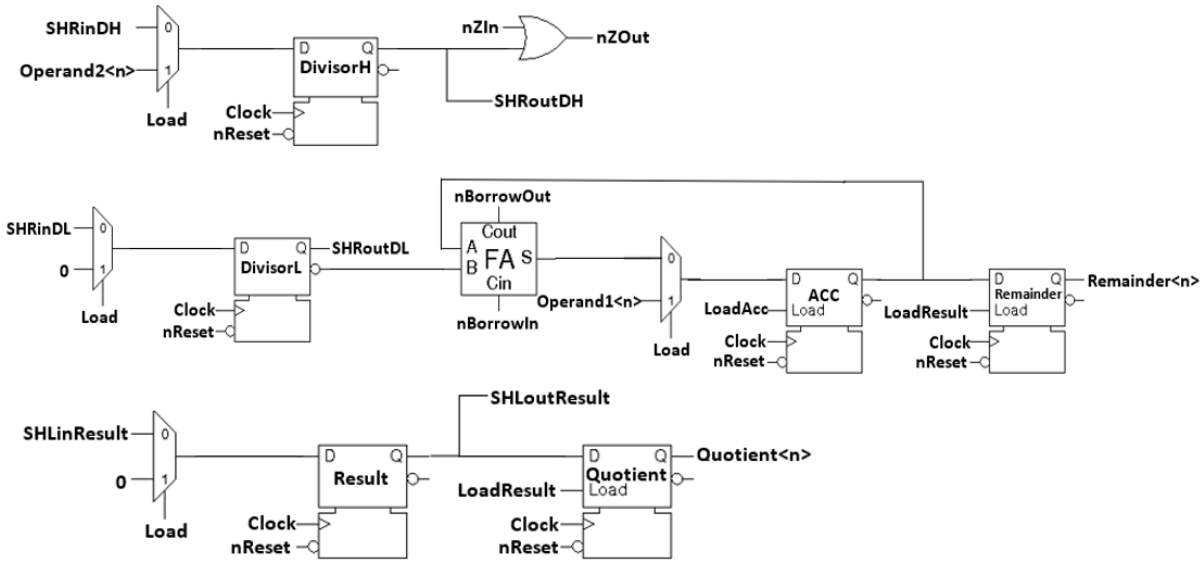


Division Algorithm

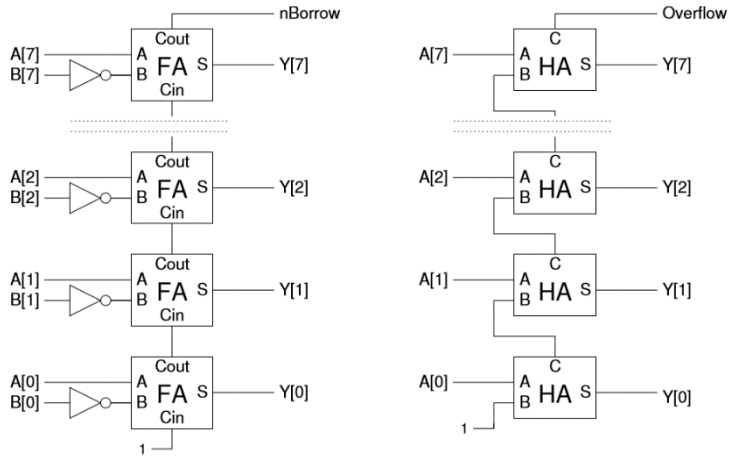
```
ACC = Operand1; Result = 0;
DivisorH = Operand2; DivisorL = 0;

for ( i = 0; i < 8; i = i+1 )
  begin
    {DivisorH,DivisorL} = {DivisorH,DivisorL} >> 1;
    Result = Result << 1;
    if ( (DivisorH == 0) && ( ACC >= DivisorL) )
      begin
        ACC = ACC - DivisorL;
        Result[0] = 1;
      end
  end

Remainder = ACC;
Quotient = Result;
```

Bitslice Datapath Design

Divider Bitslice Gate-Level Schematic

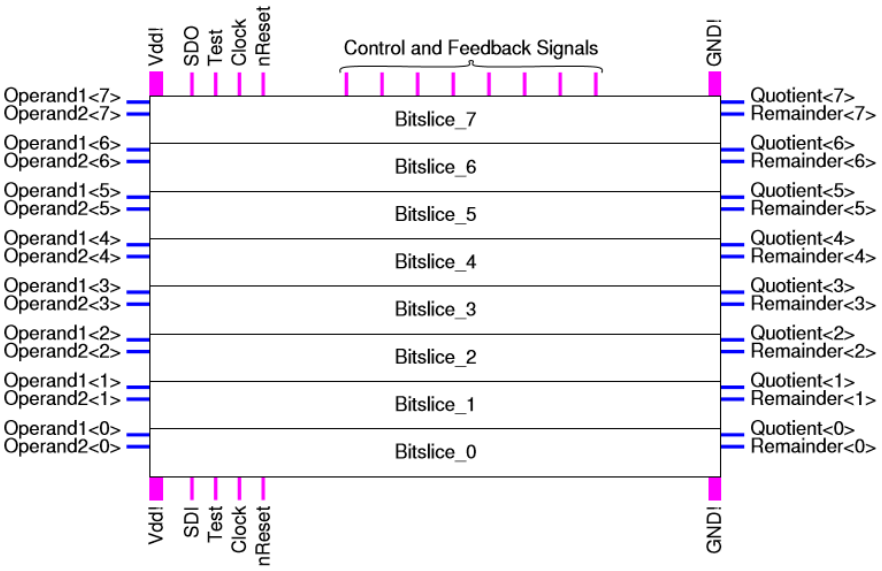


- The subtractor and incrementer[2] circuits:



8 Identical Bitslice Cells

- all inter-bitslice wiring is by butting.



Control Design