Gated D-Latch

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Abstract—

A Latch is sequential logic circuit which can store and hold binary information once provided at the input without the need of maintaining constant input voltage level. Since Latches can hold 2 stable states, latches are referred as bi-stable multi-vibrator. Gated latches changes its output state with respect to inputs when the latch is enabled and when they are disabled they hold its previous value irrespective of the changes in inputs. Since the enable input on a gated S-R latch provides a way to latch the Q and not-Q outputs without regard to the status of S or R, we can eliminate one of those inputs to create a multivibrator latch circuit with no "illegal" input states. Such a circuit is called a D latch.

Keywords— Latches, Gated Latch

I. CIRCUIT DETAILS

The Gated D-Latch circuit diagram is represented below in the figure 1. The Latch is in transparent mode when the enable signal is high and the output follows the input logic state whereas when the enable signal is low, the latch is in hold state and the output remain in its previous state even when the logic levels of the input changes. This circuit is implemented using a buffer, a PMOS, two NMOS and three inverters. The detailed design is illustrated below where the PMOS is used for high only and the NMOS is used to low only. Further a pair of inverters are connected in a feedback manner from the output to latch the output value in its desired state. The buffer and inverter will be implemented using Verilog code.

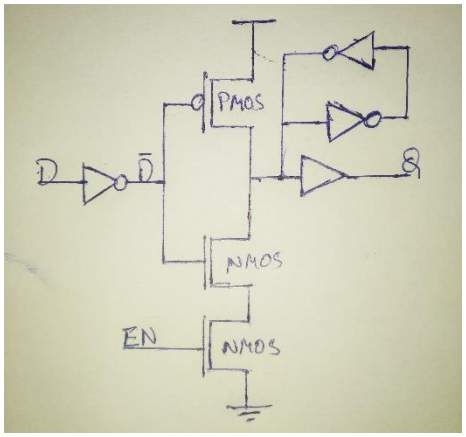

Figure 1: Gated D-Latch Circuit Diagram

The PMOS and the NMOS are analog devices which will be implemented using SKY130 PDK.

The truth table of the D-latch is presented below.

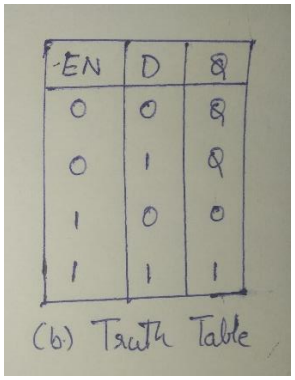

Figure 2: Gated D-Latch Truth Table

II. EXPECTED WAVEFORM

The expected waveform of the Gated D-Latch is presented below.

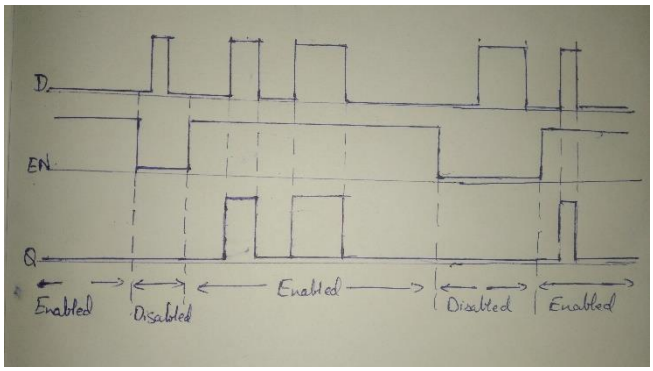

Figure 3: Expected Waveform

III. REFERENCES

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