**EXPERIMENT NO. 6A** **DATE:03/09/2020**

**RA1911028010110 CSE-CC (J1)**

**SANKALP MISHRA**

# FULL ADDER CIRCUIT

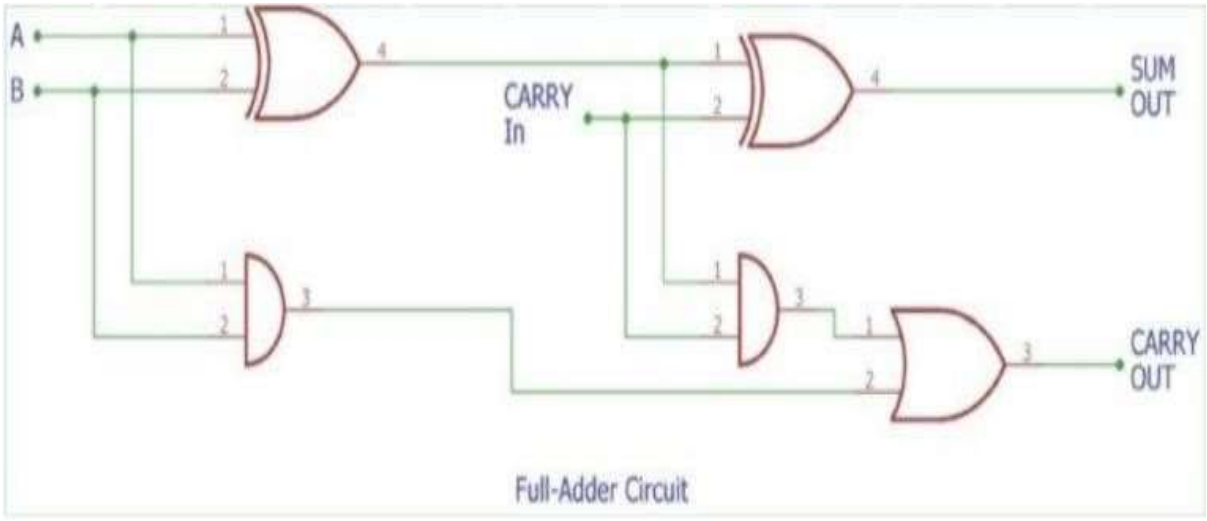
AIM : To design and implement a full adder circuit.

SOFTWARE USED : Logic gate simulator

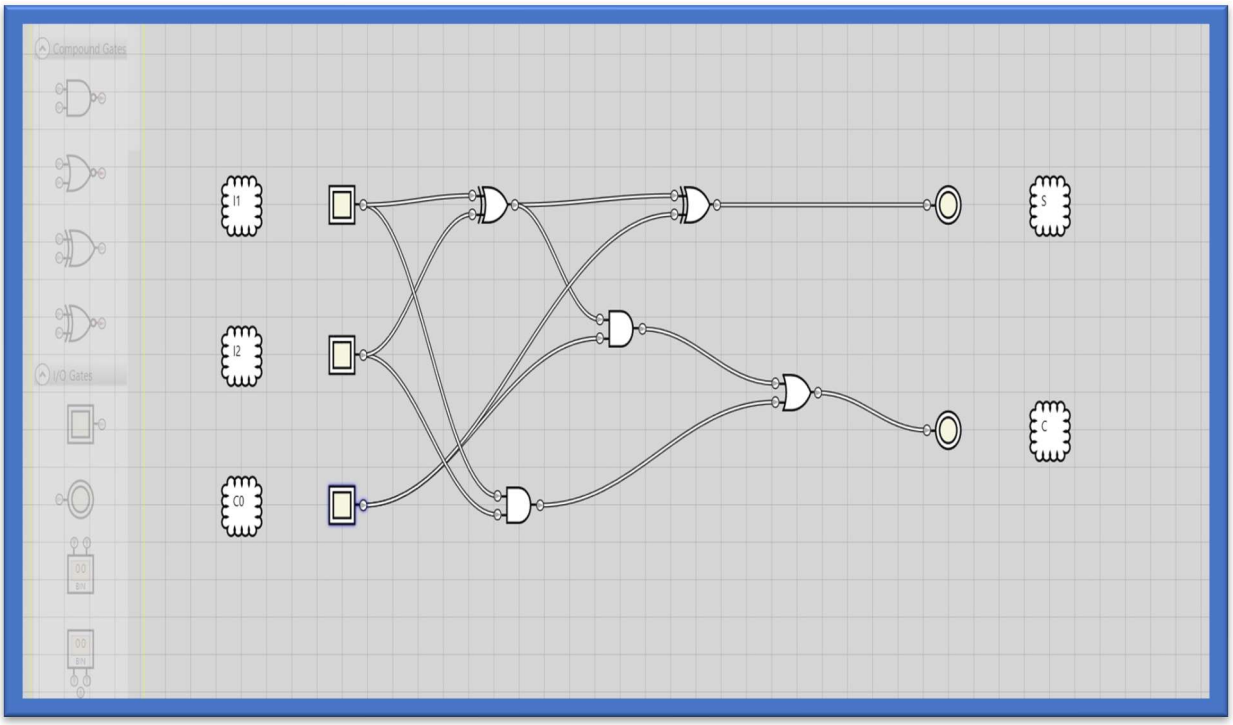
TRUTH TABLE :

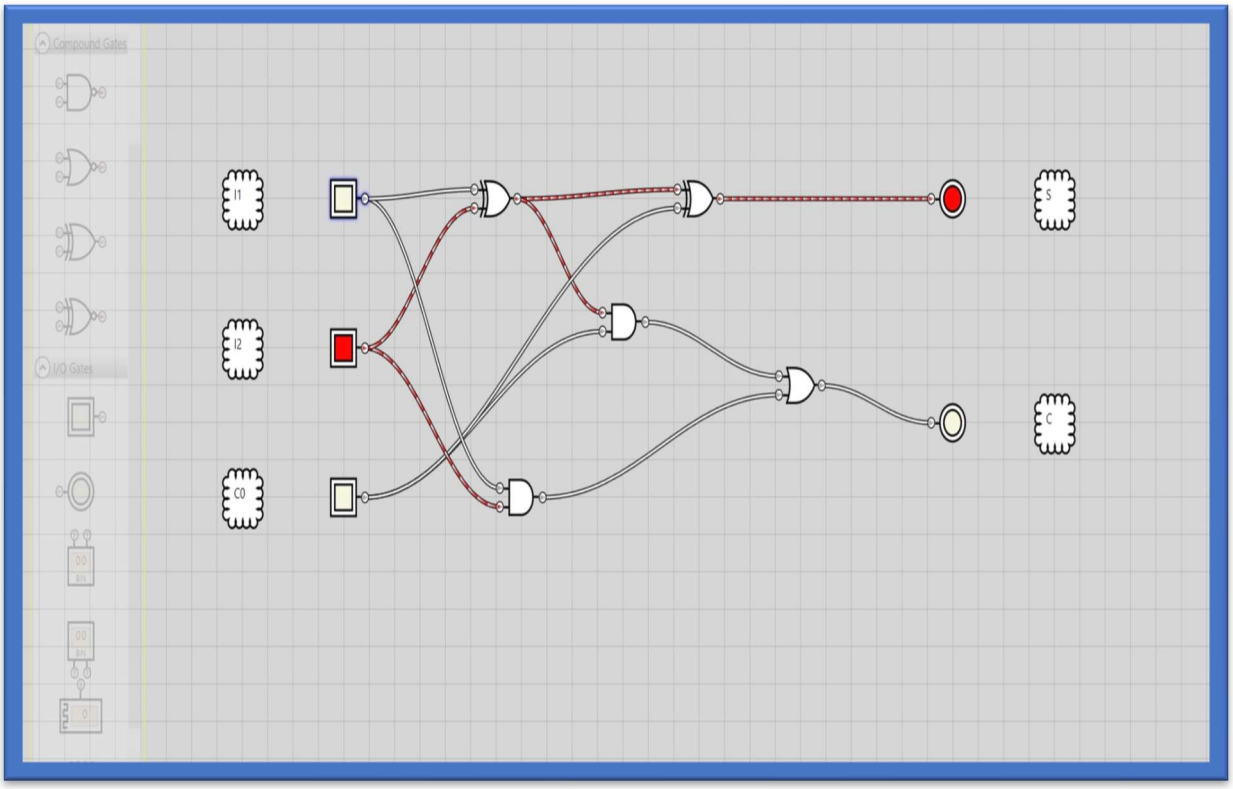
| A | B | $C_{IN}$ | SUM | $CARRY_{OUT}$ |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 | 0 |
| 0 | 1 | 0 | 1 | 0 |
| 0 | 1 | 1 | 0 | 1 |
| 1 | 0 | 0 | 1 | 0 |
| 1 | 0 | 1 | 0 | 1 |
| 1 | 1 | 0 | 0 | 1 |
| 1 | 1 | 1 | 1 | 1 |

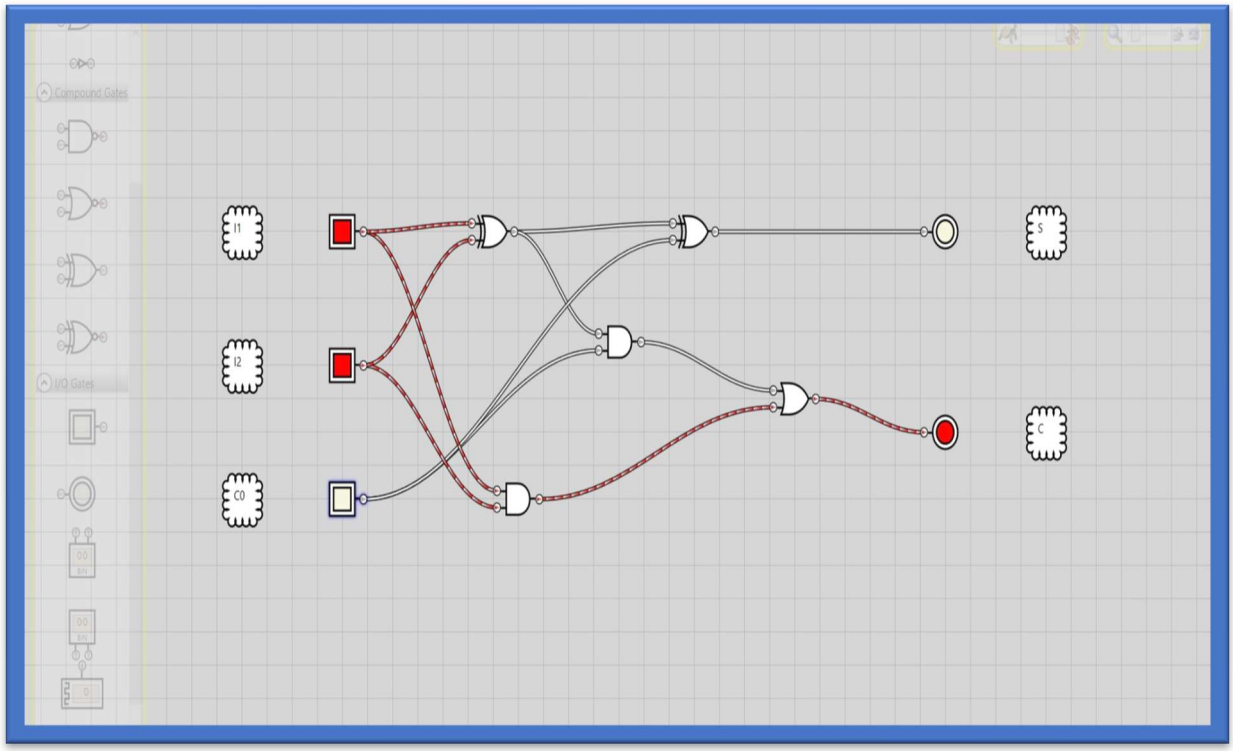
CIRCUIT DIAGRAM :

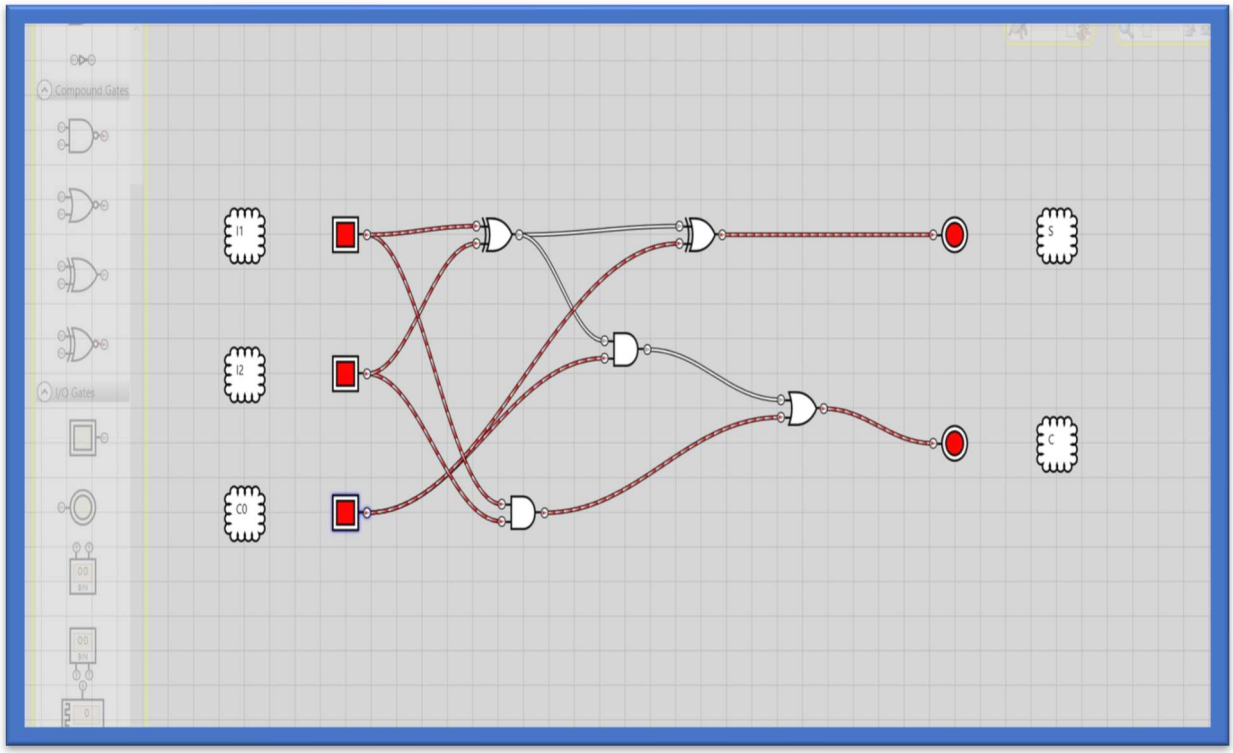


OUTPUT :


Compound Gates
I/O Gates
I1
I2
C0
S
C


Compound Gates
I/O Gates
I1
I2
C0
S
C




RESULT : Here, we add three one bit binary numbers, two operands & a carry bit.

**EXPERIMENT NO. 6B** **DATE:03/09/2020**

# HALF ADDER CIRCUIT

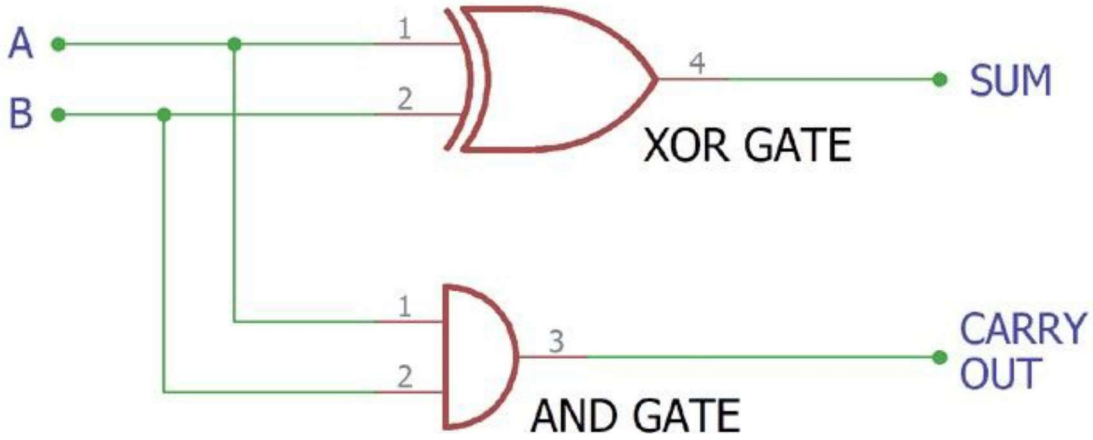
AIM : To design and implement a half adder circuit.

SOFTWARE USED : Logic gate simulator

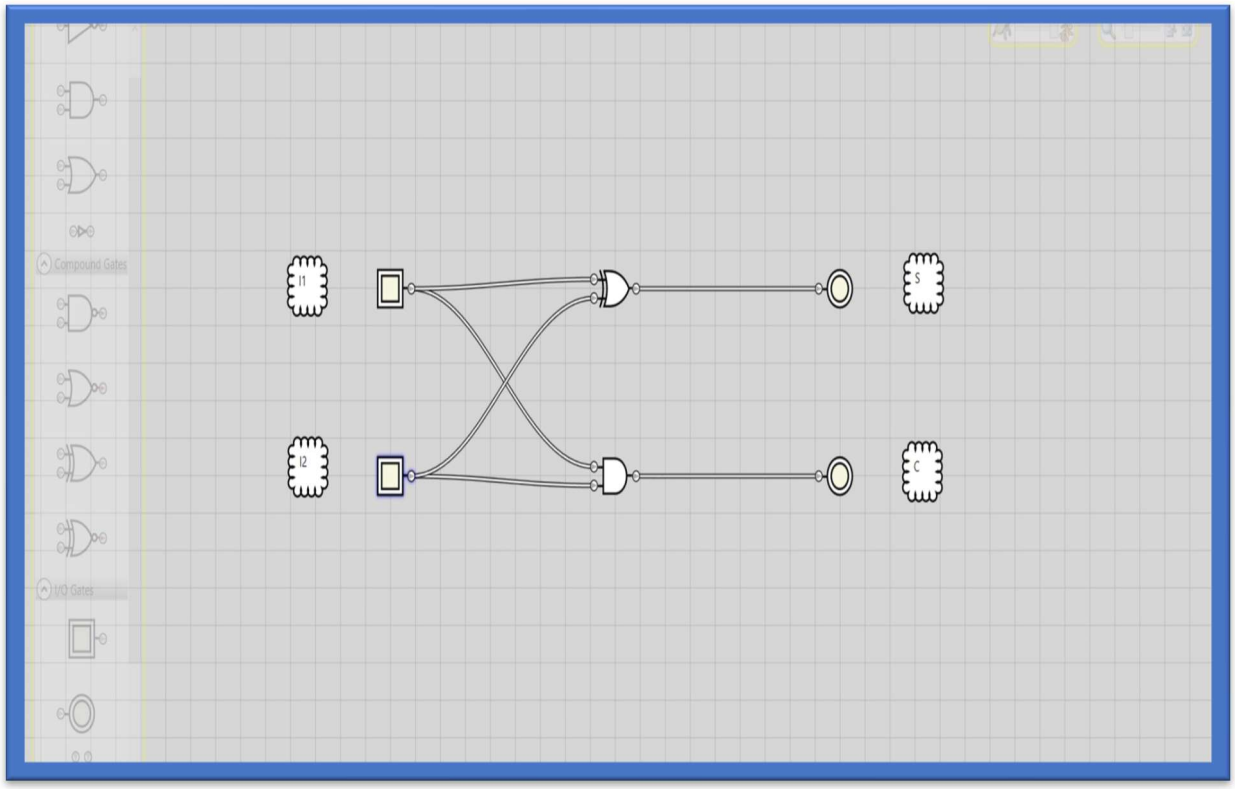
TRUTH TABLE :

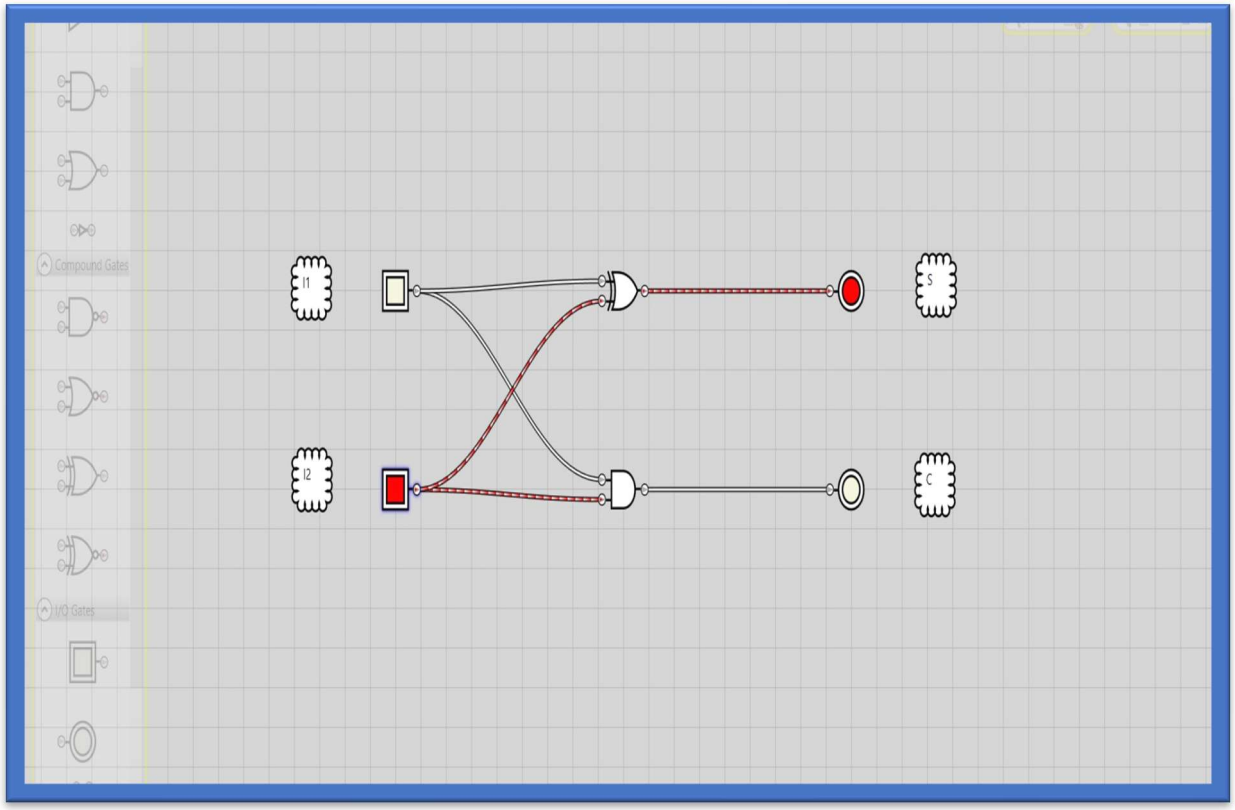
| A | B | SUM | CARRY |
|---|---|---|---|
| **0** | 0 | 0 | 0 |
| **0** | 1 | 1 | 0 |
| **1** | 0 | 1 | 0 |
| **1** | 1 | 0 | 1 |

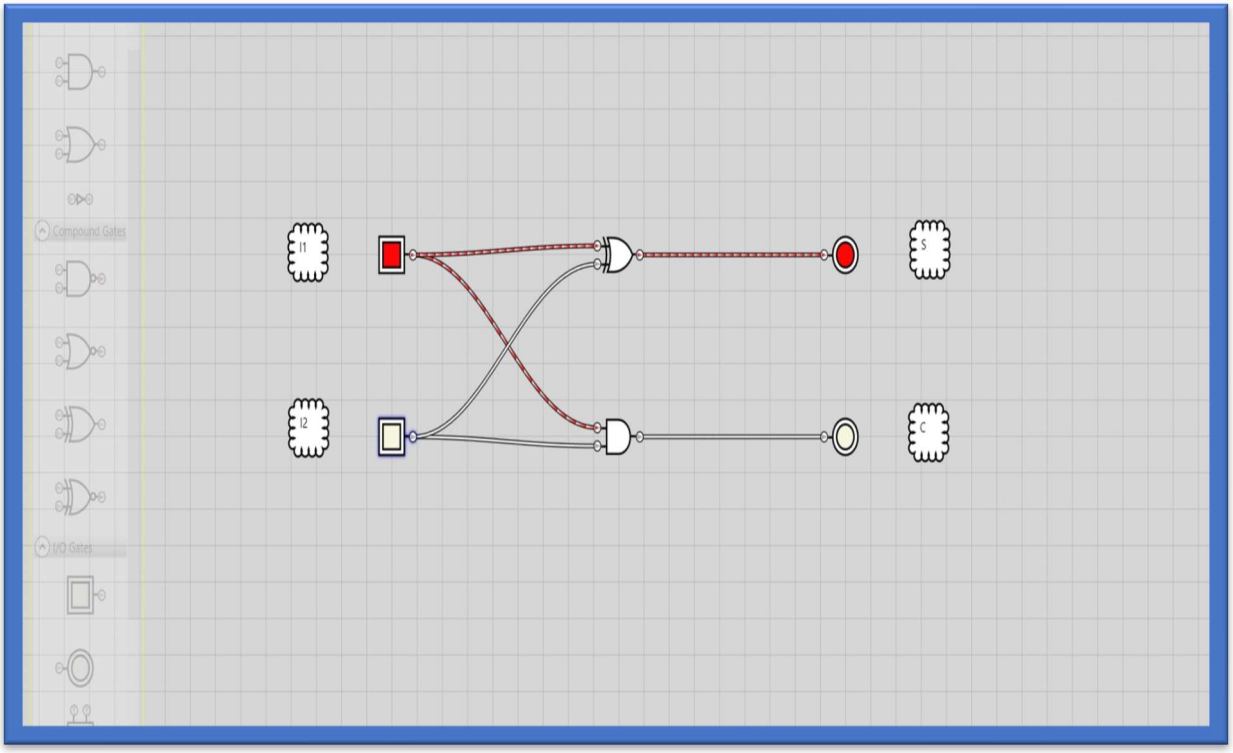
CIRCUIT DIAGRAM :

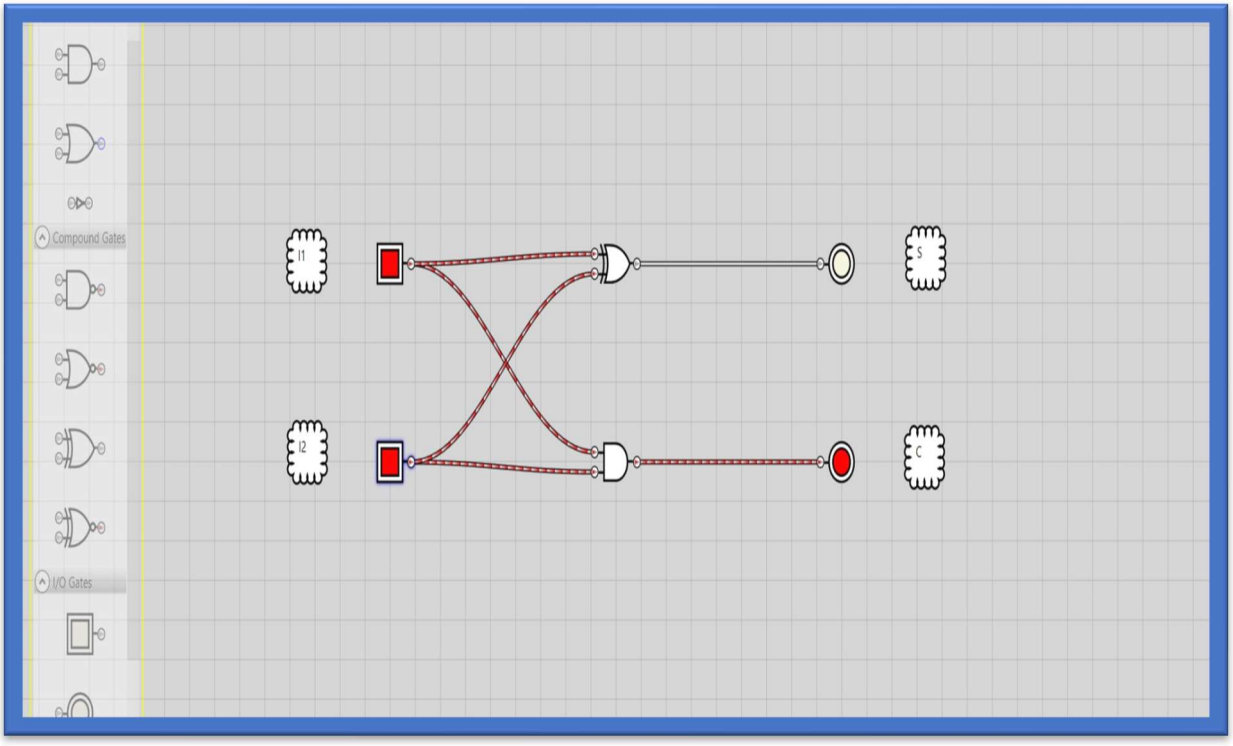



OUTPUT :


Compound Gates
I/O Gates
I1
I2
S
C


Compound Gates
I/O Gates
I1
I2
S
C




RESULT : Here, we add two single digit binary numbers & results in two digit out.