This schematic is *NOT SUPPORTED* and DOES NOT constitute a reference design. Only "community" support is allowed.

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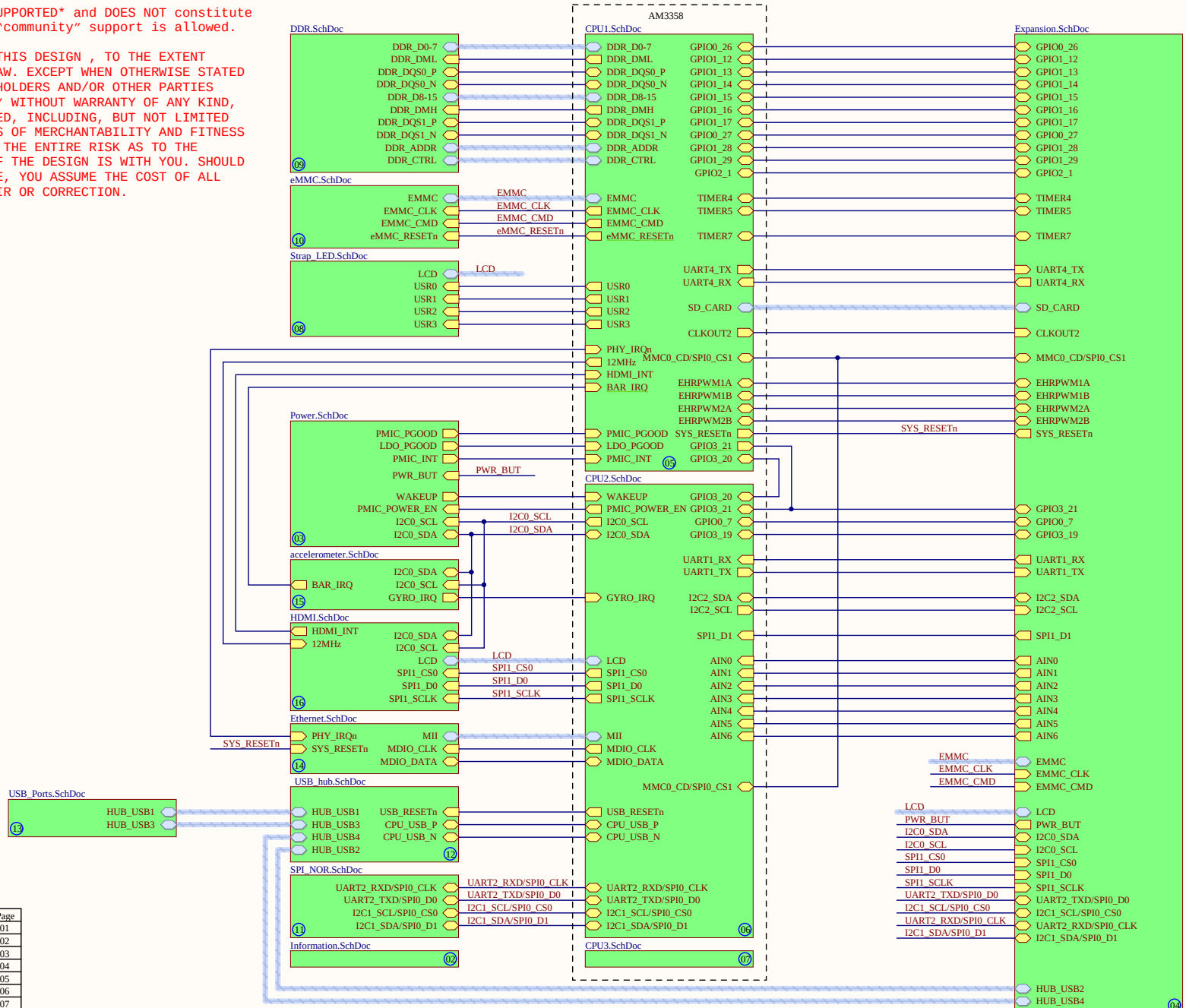

Block	Range	Page
Top Level	-	01
Information	4300 - 4399	02
DC-DC and Power	200 - 299	03
Port Expansion	7000 - 7099	04
CPU DDR, Clocks GPIO1	2000 - 2099	05
CPU GPIO2	2100 - 2199	06
CPU Power and Ground	2200 - 2299	07
CPU Pin Strapping and LEDs	7100 - 7199	08
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SPI NOR Flash	3100 - 3199	11
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Ethernet and RJ45	4000 - 4099	14
Accelermometer and Barometer	7400 - 7499	15
HDMI Port	5800 - 5899	16

Title: Top Level

Size:	A3	Date:	26/01/2017
Drawn by	David Fields		
Revision	1D		
Sheet	01 of 16		

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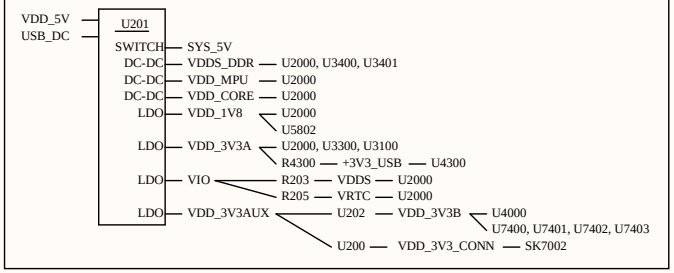
United Kingdom

SYSBOOT[15:14]	SYSBOOT[13:12]	SYSBOOT[11:10]	SYSBOOT[9]	SYSBOOT[8]	SYSBOOT[7:6]	SYSBOOT[5]	SYSBOOT[4:0]	Boot Sequence			
00b = 19.2MHz 01b = 24MHz 10b = 25MHz 11b = 26MHz	00b (all other values reserved)	Don't care for ROM code	Don't care for ROM code	Don't care for ROM code	Don't care for ROM code	0 = CLKOUT1 disabled 1 = CLKOUT1 enabled	11100b <-	MMC1 SW7100 open	MMC0 SW7100 closed	UART0	USB0
00b = 19.2MHz 01b = 24MHz 10b = 25MHz 11b = 26MHz	00b (all other values reserved)	Don't care for ROM code	Don't care for ROM code	Don't care for ROM code	Don't care for ROM code	0 = CLKOUT1 disabled 1 = CLKOUT1 enabled	11000b	SPI0 SW7100 open	MMC0 SW7100 closed	USB0	UART0

Power Tree



I2C Buses			
BUS	DEVICE	FUNCTION	I2C READ ADDR
I2C0	U201	REGULATOR	REGULATOR
	U7000	EEPROM	EEPROM
	U7400	MPU-9150 Gyro, Accelerometer, Compass	0xC0 or 0xC1
	U7401	MPU-6000 Gyro, Accelerometer	0xC0 or 0xC1
	U7402	MPU-9250 Gyro, Accelerometer, Compass	0xC0 or 0xC1
	U7403	LPS331AP Barometer	0xB8 or 0xBA
	U5802	TDA19988 HDMI Transmitter	
I2C1	-	Expansion Port	

Power Budget (Max)					All current in mA				
	VDD_CORE	VDD_MPU	VDDS_DDR	VDD_1V8~	VDD_IO§	VDD_3V3A	VDD_3V3B	VDD_3V3CONN	SYS_5V
Functional Block	1.1V	1.1V	1.5V	1.8V	3.3V	3.3V	3.3V	3.3V	5V
Core	400								
MPU		380							
DDR			450						
RTC + VDDS					55				
CPU PLL + ADC				120					
CPU IO						415			
eMMC									
SPI NOR*								230	
USB Hub								25	
USB Ports								80	1000
Ethernet							54		
Accelerometer*									
Barometer*								4	
HDMI				127				1	65
Expansion EEPROM								3	
Micro SD Card								100	
Sled									
Total Current (mA)	400	380	450	247	55	760	54	100	1065
Voltage Rail (V)	1.1	1.1	1.5	1.8	3.3	3.3	3.3	3.3	5
Rail Power (mW)	440	418	675	444					
DC-DC efficiency									
Input Power									
Input Current									

* If Part Is Fitted Only
§ VIO is a combination of VDDS and VRTC
~ VDD 1V8 is a combination of VDD_PLL, VDD_ADC and VDD_1V8

Version	Description
1D	Backer Released Design

Notes:

USB OTG Port - Normally USB port 0 on U2000 is configured for a device port only. Siince this port is an On The Go port it can be configured for host mode instead.
To use USB 0 has host mode R2000 and R2104 must be fitted. R2000 means U2000 is in host mode. R2104 is to make the OTG port provide power to the external device
The Linux Kernel must also be recompiled to enable USB 0 in host mode.

SPI NOR - Standard boot device is eMMC flash. It is possible to make U2000 boot from SPI NOR instead.
This has several security benefits since the bootloader is now seperate from the application image
To enable this mode SYSMODE[2] must change from 1 to 0. This is done by removing R7135 and fitting R7114. U3100 must also be fitted.
Be aware that SPI NOR signals are also used on the expansion port.

Title: Information			
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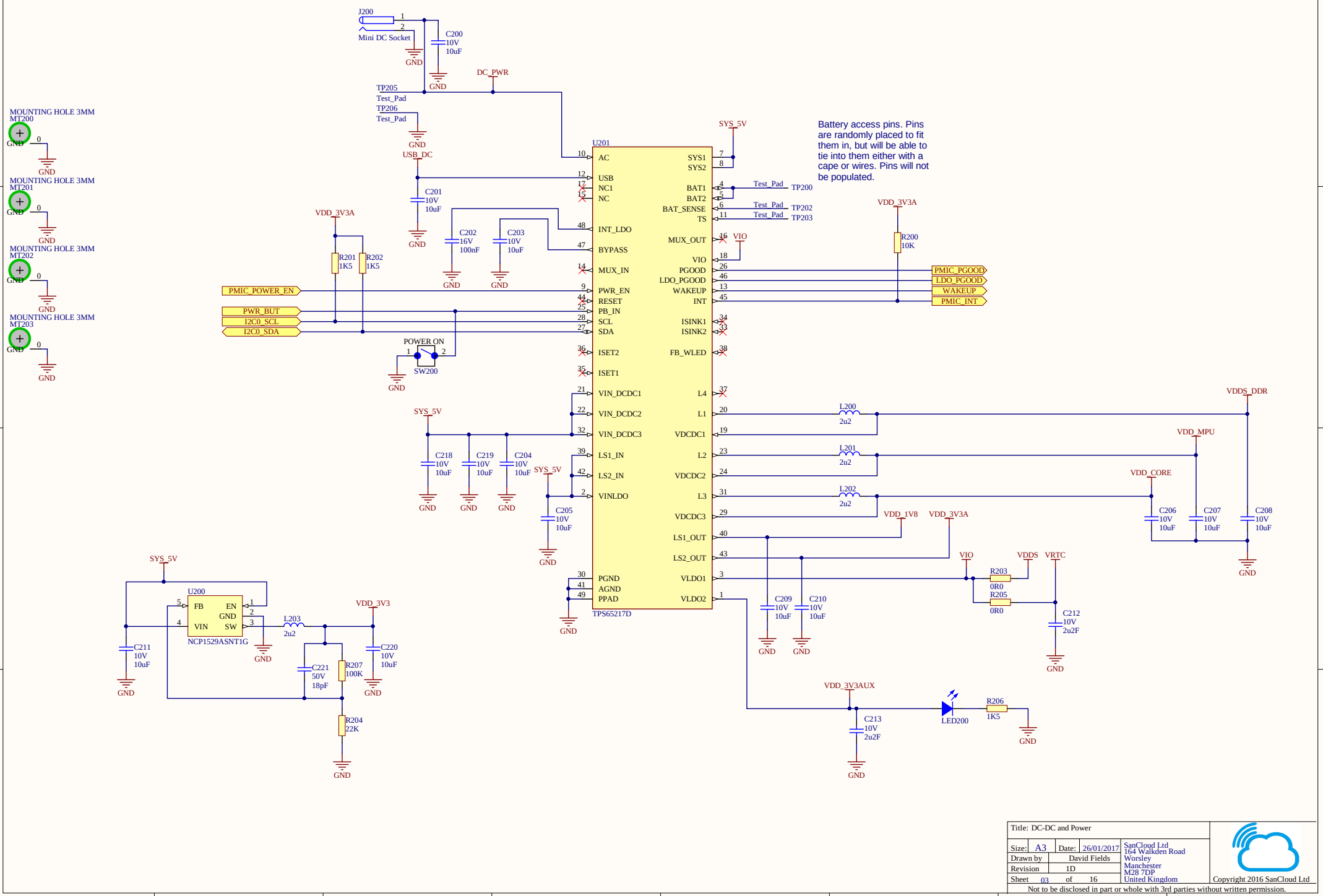

Title: DC-DC and Power			
Size: A3	Date: 26/01/2017	SanCloud Ltd 164 Walkden Road Worsley Manchester M28 7DP United Kingdom	
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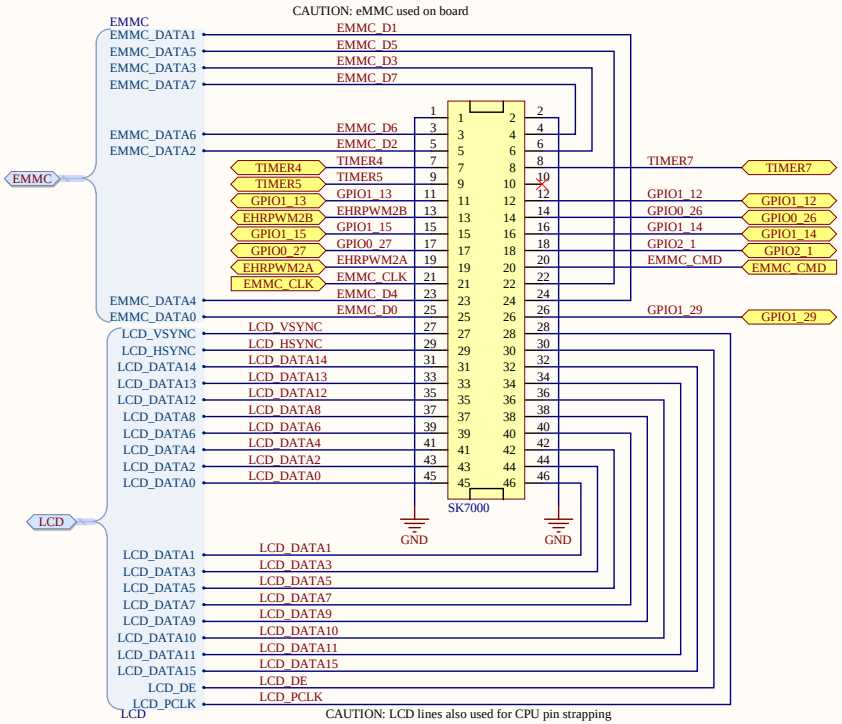
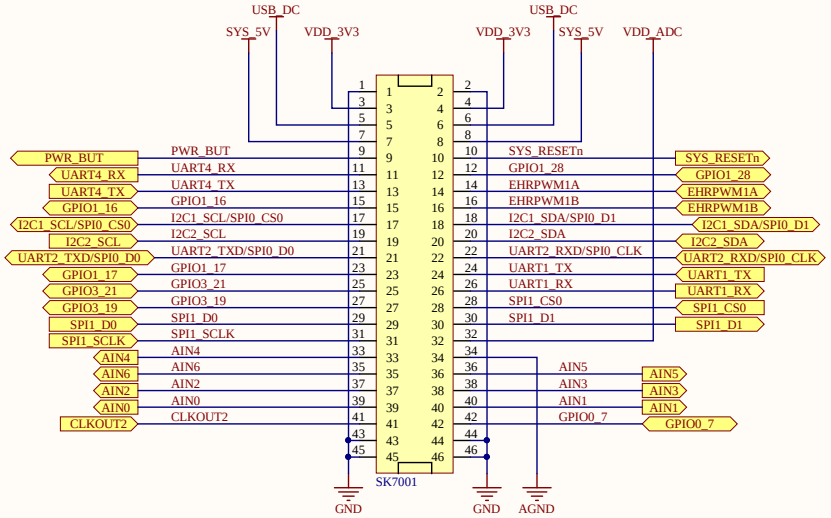
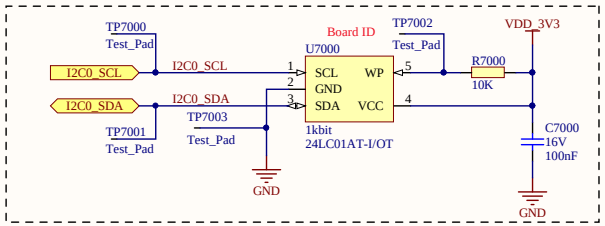
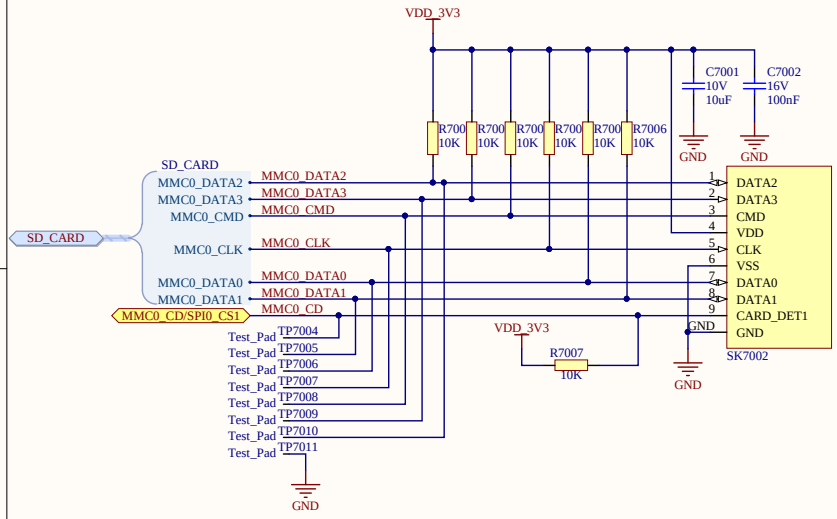
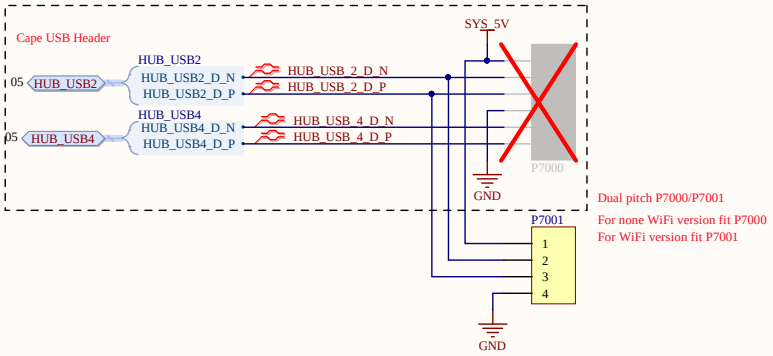
Revision	1D		
Sheet 03 of 16			











Title: Power Expansion and uSD Card			
Size: A3	Date: 26/01/2017	SanCloud Ltd 164 Walkden Road Worsley Manchester M28 7DP United Kingdom	
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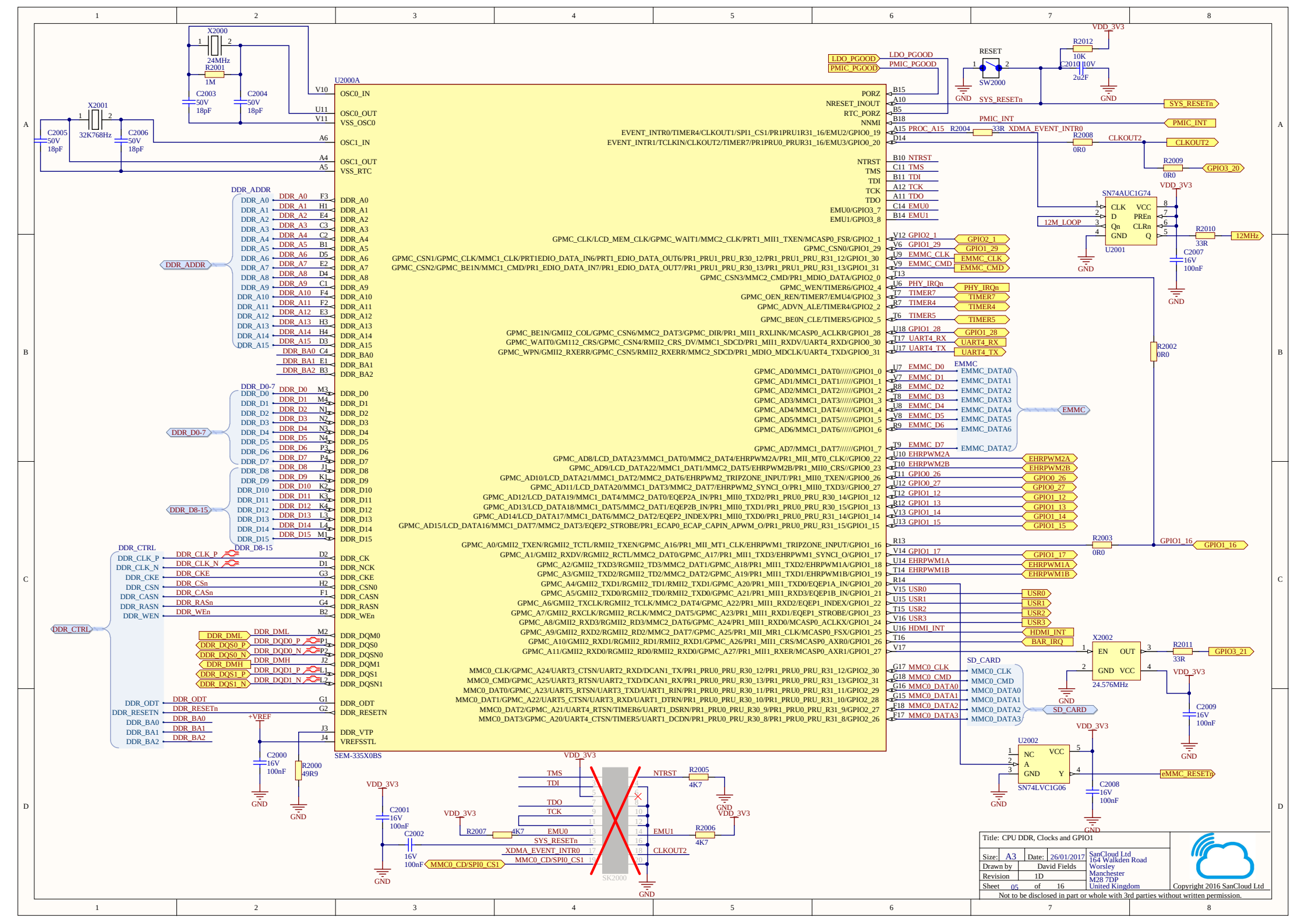
U2000A
SEM-335X0BS
OSC0_IN
OSC0_OUT
VSS_OSC0
OSC1_IN
OSC1_OUT
VSS_RTC
PORZ
NRESET_INOUT
RTC_PORZ
NNMI
EVENT_INTR0/TIMER4/CLKOUT1/SPI1_CS1/PR1PRU1R31_16/EMU2/GPIO0_19
EVENT_INTR1/TCLKIN/CLKOUT2/TIMER7/PR1PRU0_PRUR31_16/EMU3/GPIO0_20
NTRST
TMS
TDI
TCK
TDO
EMU0/GPIO3_7
EMU1/GPIO3_8
DDR_ADDR
DDR_D0-7
DDR_D8-15
DDR_CTRL
DDR_CLK_P
DDR_CLK_N
DDR_CKE
DDR_CSn
DDR_CASn
DDR_RASn
DDR_WEn
DDR_DML
DDR_DQS0_P
DDR_DQS0_N
DDR_DMH
DDR_DQS1_P
DDR_DQS1_N
DDR_ODT
DDR_RESETn
DDR_BA0
DDR_BA1
DDR_BA2
+VREF
DDR_VTP
VREFSSTL
GPMC_CLK/LCD_MEM_CLK/GPMC_WAIT1/MMC2_CLK/PRT1_MII1_TXEN/MCASP0_FSR/GPIO2_1
GPMC_CSN0/GPIO1_29
GPMC_CSN1/GPMC_CLK/MMC1_CLK/PRT1EDIO_DATA_IN6/PRT1_EDIO_DATA_OUT6/PR1_PRU1_PRU_R30_12/PR1_PRU1_PRU_R31_12/GPIO1_30
GPMC_CSN2/GPMC_BE1N/MMC1_CMD/PR1_EDIO_DATA_IN7/PR1_EDIO_DATA_OUT7/PR1_PRU1_PRU_R30_13/PR1_PRU1_PRU_R31_13/GPIO1_31
GPMC_CSN3/MMC2_CMD/PR1_MDIO_DATA/GPIO2_0
GPMC_WEN/TIMER6/GPIO2_4
GPMC_OEN_REN/TIMER7/EMU4/GPIO2_3
GPMC_ADVN_ALE/TIMER4/GPIO2_2
GPMC_BE0N_CLE/TIMER5/GPIO2_5
GPMC_BE1N/GMII2_COL/GPMC_CSN6/MMC2_DAT3/GPMC_DIR/PR1_MII1_RXLINK/MCASP0_ACLKR/GPIO1_28
GPMC_WAIT0/GM112_CRS/GPMC_CSN4/RMII2_CRS_DV/MMC1_SDCD/PR1_MII1_RXDV/UART4_RXD/GPIO0_30
GPMC_WPN/GMII2_RXERR/GPMC_CSN5/RMII2_RXERR/MMC2_SDCD/PR1_MDIO_MDCLK/UART4_TXD/GPIO0_31
GPMC_AD0/MMC1_DAT0//////GPIO1_0
GPMC_AD1/MMC1_DAT1//////GPIO1_1
GPMC_AD2/MMC1_DAT2//////GPIO1_2
GPMC_AD3/MMC1_DAT3//////GPIO1_3
GPMC_AD4/MMC1_DAT4//////GPIO1_4
GPMC_AD5/MMC1_DAT5//////GPIO1_5
GPMC_AD6/MMC1_DAT6//////GPIO1_6
GPMC_AD7/MMC1_DAT7//////GPIO1_7
GPMC_AD8/LCD_DATA23/MMC1_DAT0/MMC2_DAT4/EHRPWM2A/PR1_MII_MT0_CLK//GPIO0_22
GPMC_AD9/LCD_DATA22/MMC1_DAT1/MMC2_DAT5/EHRPWM2B/PR1_MII0_CRS//GPIO0_23
GPMC_AD10/LCD_DATA21/MMC1_DAT2/MMC2_DAT6/EHRPWM2_TRIPZONE_INPUT/PR1_MII0_TXEN//GPIO0_26
GPMC_AD11/LCD_DATA20/MMC1_DAT3/MMC2_DAT7/EHRPWM2_SYNCI_O/PR1_MII0_TXD3//GPIO0_27
GPMC_AD12/LCD_DATA19/MMC1_DAT4/MMC2_DAT0/EQEP2A_IN/PR1_MII0_TXD2/PR1_PRU0_PRU_R30_14/GPIO1_12
GPMC_AD13/LCD_DATA18/MMC1_DAT5/MMC2_DAT1/EQEP2B_IN/PR1_MII0_TXD1/PR1_PRU0_PRU_R30_15/GPIO1_13
GPMC_AD14/LCD_DATA17/MMC1_DAT6/MMC2_DAT2/EQEP2_INDEX/PR1_MII0_TXD0/PR1_PRU0_PRU_R31_14/GPIO1_14
GPMC_AD15/LCD_DATA16/MMC1_DAT7/MMC2_DAT3/EQEP2_STROBE/PR1_ECAP0_ECAP_CAPIN_APWM_O/PR1_PRU0_PRU_R31_15/GPIO1_15
GPMC_A0/GMII2_TXEN/RGMII2_TCTL/RMII2_TXEN/GPMC_A16/PR1_MII_MT1_CLK/EHRPWM1_TRIPZONE_INPUT/GPIO1_16
GPMC_A1/GMII2_RXDV/RGMII2_RCTL/MMC2_DAT0/GPMC_A17/PR1_MII1_TXD3/EHRPWM1_SYNCI_O/GPIO1_17
GPMC_A2/GMII2_TXD3/RGMII2_TD3/MMC2_DAT1/GPMC_A18/PR1_MII1_TXD2/EHRPWM1A/GPIO1_18
GPMC_A3/GMII2_TXD2/RGMII2_TD2/MMC2_DAT2/GPMC_A19/PR1_MII1_TXD1/EHRPWM1B/GPIO1_19
GPMC_A4/GMII2_TXD1/RGMII2_TD1/RMII2_TXD1/GPMC_A20/PR1_MII1_TXD0/EQEP1A_IN/GPIO1_20
GPMC_A5/GMII2_TXD0/RGMII2_TD0/RMII2_TXD0/GPMC_A21/PR1_MII1_RXD3/EQEP1B_IN/GPIO1_21
GPMC_A6/GMII2_TXCLK/RGMII2_TCLK/MMC2_DAT4/GPMC_A22/PR1_MII1_RXD2/EQEP1_INDEX/GPIO1_22
GPMC_A7/GMII2_RXCLK/RGMII2_RCLK/MMC2_DAT5/GPMC_A23/PR1_MII1_RXD1/EQEP1_STROBE/GPIO1_23
GPMC_A8/GMII2_RXD3/RGMII2_RD3/MMC2_DAT6/GPMC_A24/PR1_MII1_RXD0/MCASP0_ACLKX/GPIO1_24
GPMC_A9/GMII2_RXD2/RGMII2_RD2/MMC2_DAT7/GPMC_A25/PR1_MII_MR1_CLK/MCASP0_FSX/GPIO1_25
GPMC_A10/GMII2_RXD1/RGMII2_RD1/RMII2_RXD1/GPMC_A26/PR1_MII1_CRS/MCASP0_AXR0/GPIO1_26
GPMC_A11/GMII2_RXD0/RGMII2_RD0/RMII2_RXD0/GPMC_A27/PR1_MII1_RXER/MCASP0_AXR1/GPIO1_27
MMC0_CLK/GPMC_A24/UART3_CTSN/UART2_RXD/DCAN1_TX/PR1_PRU0_PRU_R30_12/PR1_PRU0_PRU_R31_12/GPIO2_30
MMC0_CMD/GPMC_A25/UART3_RTSN/UART2_TXD/DCAN1_RX/PR1_PRU0_PRU_R30_13/PR1_PRU0_PRU_R31_13/GPIO2_31
MMC0_DAT0/GPMC_A23/UART5_RTSN/UART3_TXD/UART1_RIN/PR1_PRU0_PRU_R30_11/PR1_PRU0_PRU_R31_11/GPIO2_29
MMC0_DAT1/GPMC_A22/UART5_CTSN/UART3_RXD/UART1_DTRN/PR1_PRU0_PRU_R30_10/PR1_PRU0_PRU_R31_10/GPIO2_28
MMC0_DAT2/GPMC_A21/UART4_RTSN/TIMER6/UART1_DSRN/PR1_PRU0_PRU_R30_9/PR1_PRU0_PRU_R31_9/GPIO2_27
MMC0_DAT3/GPMC_A20/UART4_CTSN/TIMER5/UART1_DCDN/PR1_PRU0_PRU_R30_8/PR1_PRU0_PRU_R31_8/GPIO2_26
LDO_PGOOD
PMIC_PGOOD
RESET
SW2000
SYS_RESETn
PMIC_INT
R2004
33R
XDMA_EVENT_INTR0
CLKOUT2
GPIO3_20
SN74AUC1G74
12M_LOOP
U2001
12MHz
EMMC
EMMC_DATA0
EMMC_DATA1
EMMC_DATA2
EMMC_DATA3
EMMC_DATA4
EMMC_DATA5
EMMC_DATA6
EMMC_DATA7
EMMC_D0
EMMC_D1
EMMC_D2
EMMC_D3
EMMC_D4
EMMC_D5
EMMC_D6
EMMC_D7
EHRPWM2A
EHRPWM2B
GPIO0_26
GPIO0_27
GPIO1_12
GPIO1_13
GPIO1_14
GPIO1_15
GPIO1_16
GPIO1_17
EHRPWM1A
EHRPWM1B
USR0
USR1
USR2
USR3
HDMI_INT
BAR_IRQ
X2002
24.576MHz
GPIO3_21
SD_CARD
MMC0_CLK
MMC0_CMD
MMC0_DATA0
MMC0_DATA1
MMC0_DATA2
MMC0_DATA3
U2002
SN74LVC1G06
eMMC_RESETn
PHY_IRQn
TIMER7
TIMER4
TIMER5
UART4_RX
UART4_TX
SK2000
MMC0_CD/SPI0_CS1
R2000 49R9
R2001 1M
R2002 0R0
R2003 0R0
R2005 4K7
R2006 4K7
R2007 4K7
R2008 0R0
R2009 0R0
R2010 33R
R2011 33R
R2012 10K
C2000 16V 100nF
C2001 16V 100nF
C2002 16V 100nF
C2003 50V 18pF
C2004 50V 18pF
C2005 50V 18pF
C2006 50V 18pF
C2007 16V 100nF
C2008 16V 100nF
C2009 16V 100nF
C2010 10V 2u2F
X2000 24MHz
X2001 32K768Hz
VDD_3V3
GND
Title: CPU DDR, Clocks and GPIO1
Size: A3
Date: 26/01/2017
Drawn by David Fields
Revision 1D
Sheet 05 of 16
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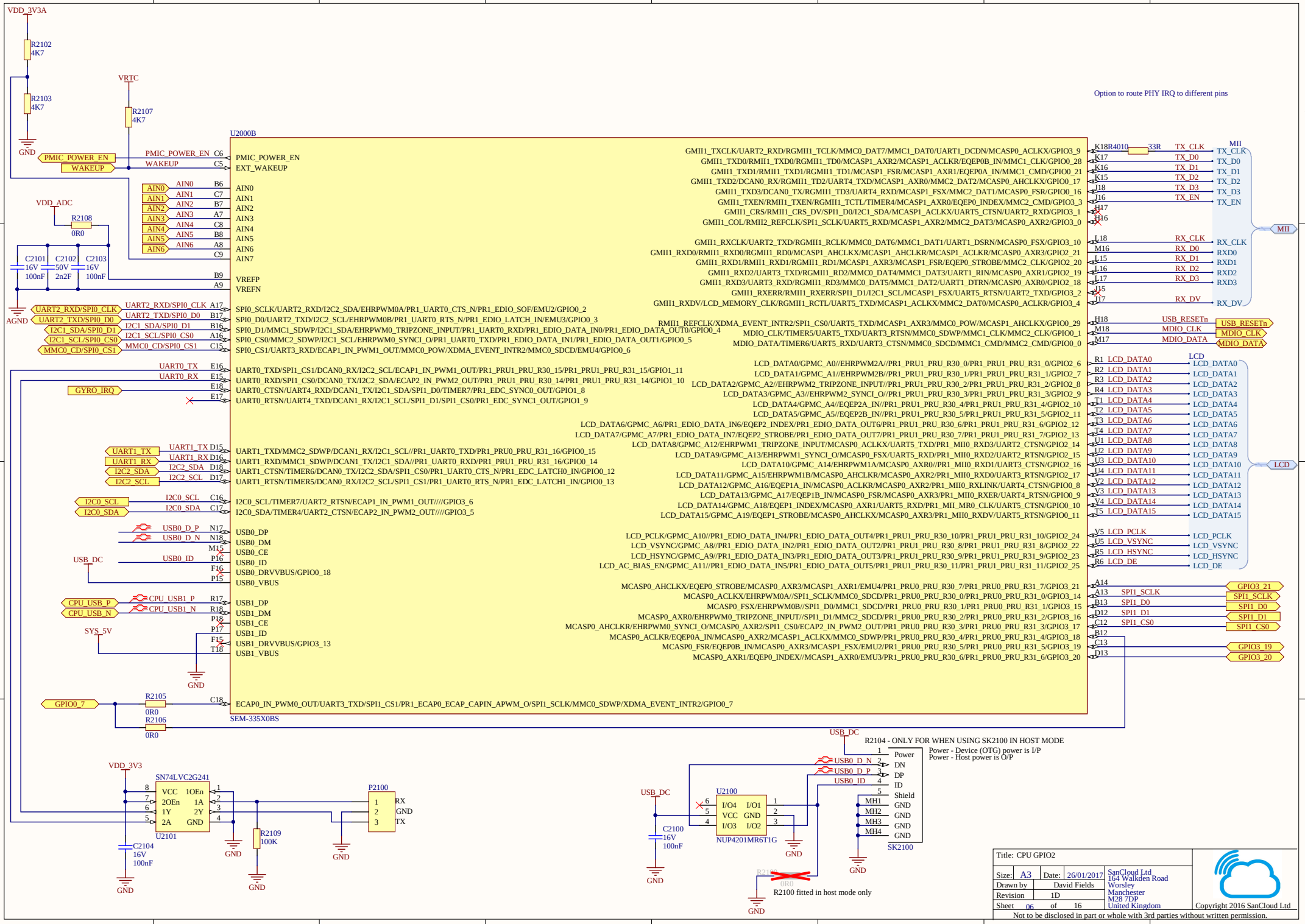
VDD_3V3A
R2102 4K7
R2103 4K7
GND
VRTC
R2107 4K7
PMIC_POWER_EN
WAKEUP
VDD_ADC
R2108 0R0
C2101 16V 100nF
C2102 50V 2n2F
C2103 16V 100nF
AGND
U2000B
SEM-335X0BS
Option to route PHY IRQ to different pins
MII
LCD
R2104 - ONLY FOR WHEN USING SK2100 IN HOST MODE
Power - Device (OTG) power is I/P
Power - Host power is O/P
R2100 fitted in host mode only
SN74LVC2G241
U2101
P2100
U2100
NUP4201MR6T1G
SK2100
Title: CPU GPIO2
Size: A3
Date: 26/01/2017
Drawn by David Fields
Revision 1D
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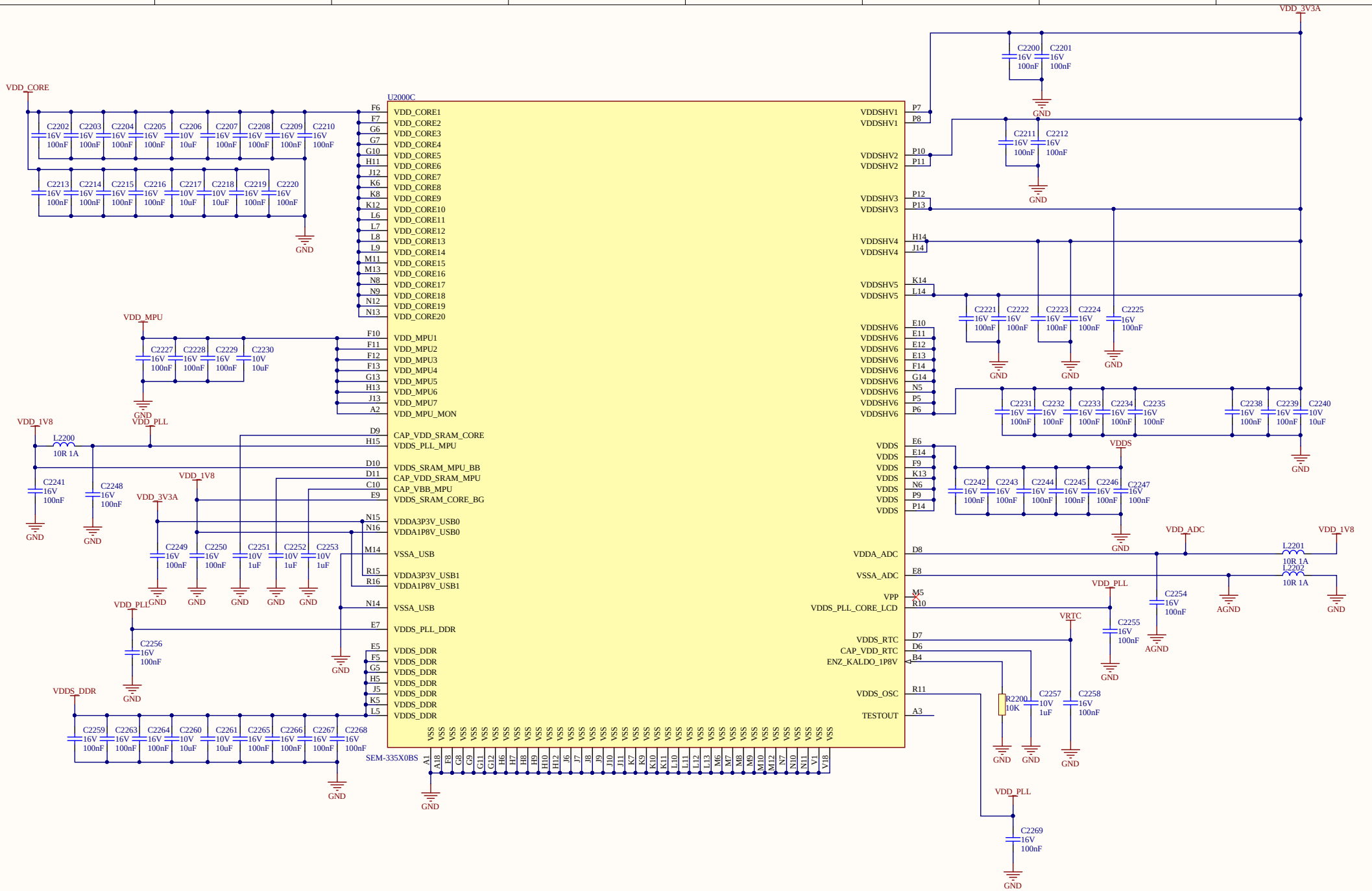
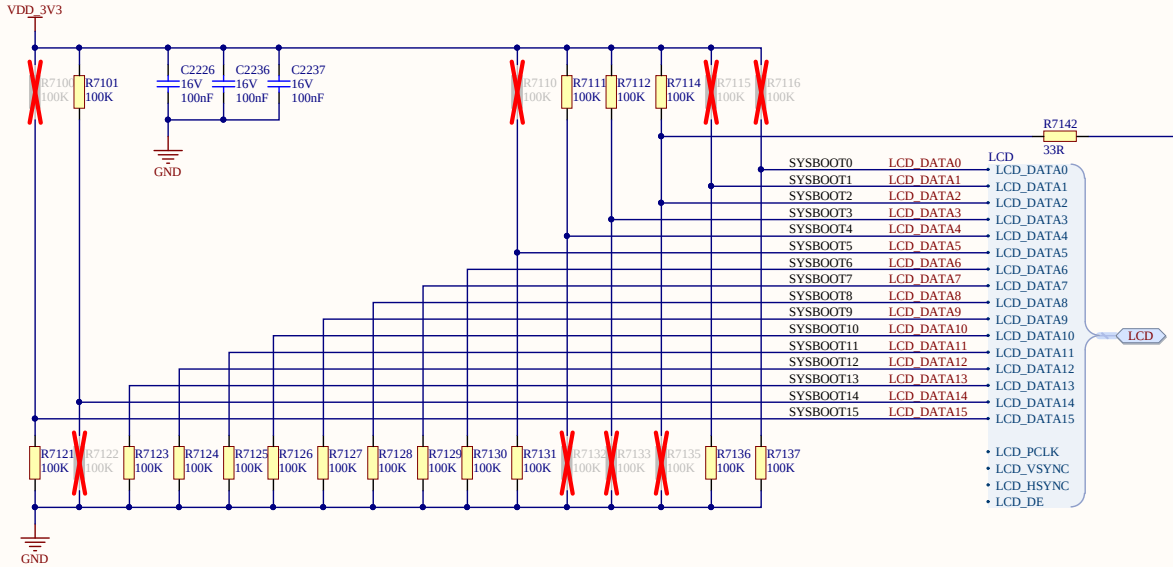
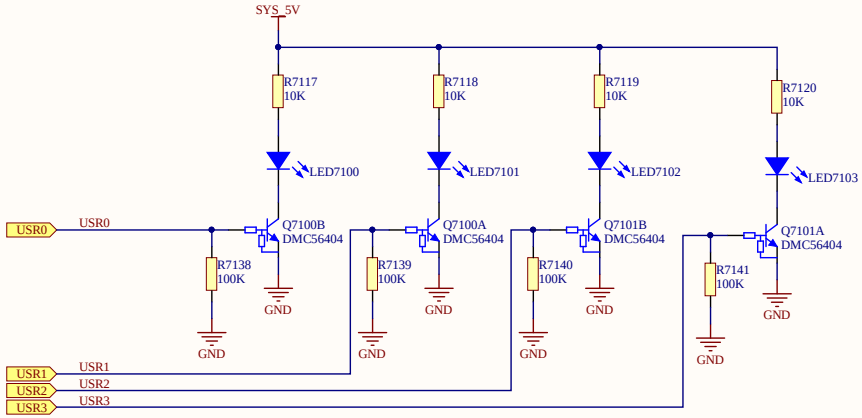


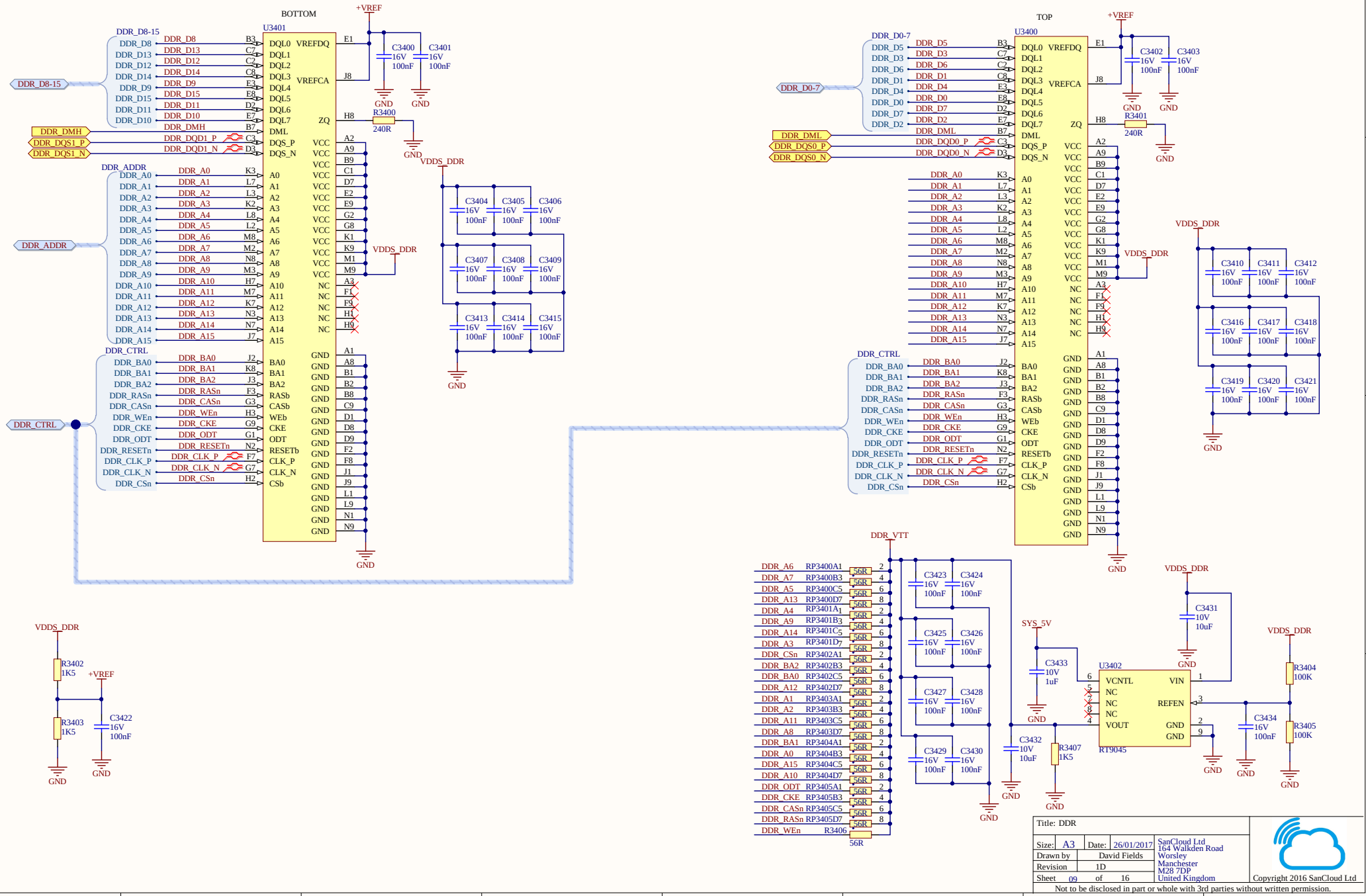
Title: CPU Power and Ground			
Size: A3	Date: 26/01/2017	SanCloud Ltd 164 Walkden Road Worsley Manchester M28 7DP United Kingdom	
Drawn by	David Fields		
Revision	1D		
Sheet 07 of 16			





SYSBOOT[15:14]	SYSBOOT[13:12]	SYSBOOT[11:10]	SYSBOOT[9]	SYSBOOT[8]	SYSBOOT[7:6]	SYSBOOT[5]	SYSBOOT[4:0]	Boot Sequence			
00b = 19.2MHz 01b = 24MHz 10b = 25MHz 11b = 26MHz	00b (all other values reserved)	Don't care for ROM code	Don't care for ROM code	Don't care for ROM code	Don't care for ROM code	0 = CLKOUT1 disabled 1 = CLKOUT1 enabled	11100b <-	MMC1 SW7100 open	MMC0 SW7100 closed	UART0	USB0
00b = 19.2MHz 01b = 24MHz 10b = 25MHz 11b = 26MHz	00b (all other values reserved)	Don't care for ROM code	Don't care for ROM code	Don't care for ROM code	Don't care for ROM code	0 = CLKOUT1 disabled 1 = CLKOUT1 enabled	11000b	SPI0 SW7100 open	MMC0 SW7100 closed	USB0	UART0

Title: CPU Pin Strapping and LEDs			
Size: A3	Date: 26/01/2017	SanCloud Ltd 164 Walkden Road Worsley Manchester M28 7DP United Kingdom	
Drawn by	David Fields		
Revision	1D		
Sheet 08 of 16			



Title:	DDR
Size:	A3
Date:	26/01/2017
Drawn by	David Fields
Revision	1D
Sheet	09 of 16

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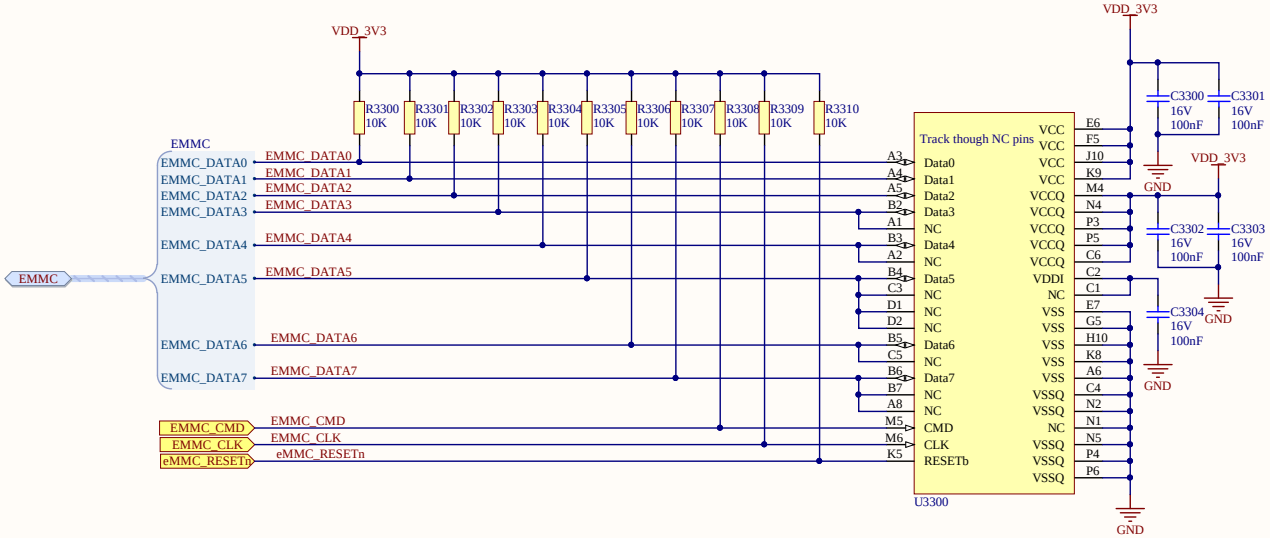

Title: eMMC Flash			
Size: A3	Date: 26/01/2017	SanCloud Ltd 164 Walkden Road Worsley Manchester M28 7DP United Kingdom	
Drawn by	David Fields		
Revision	1D		
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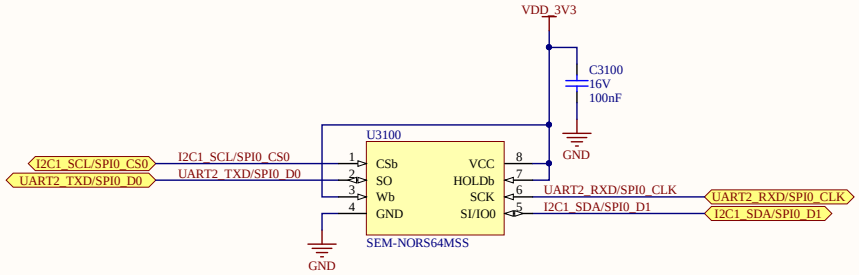

Title: SPI NOR Flash			
Size: A3	Date: 26/01/2017	SanCloud Ltd 164 Walkden Road Worsley Manchester M28 7DP United Kingdom	
Drawn by	David Fields		
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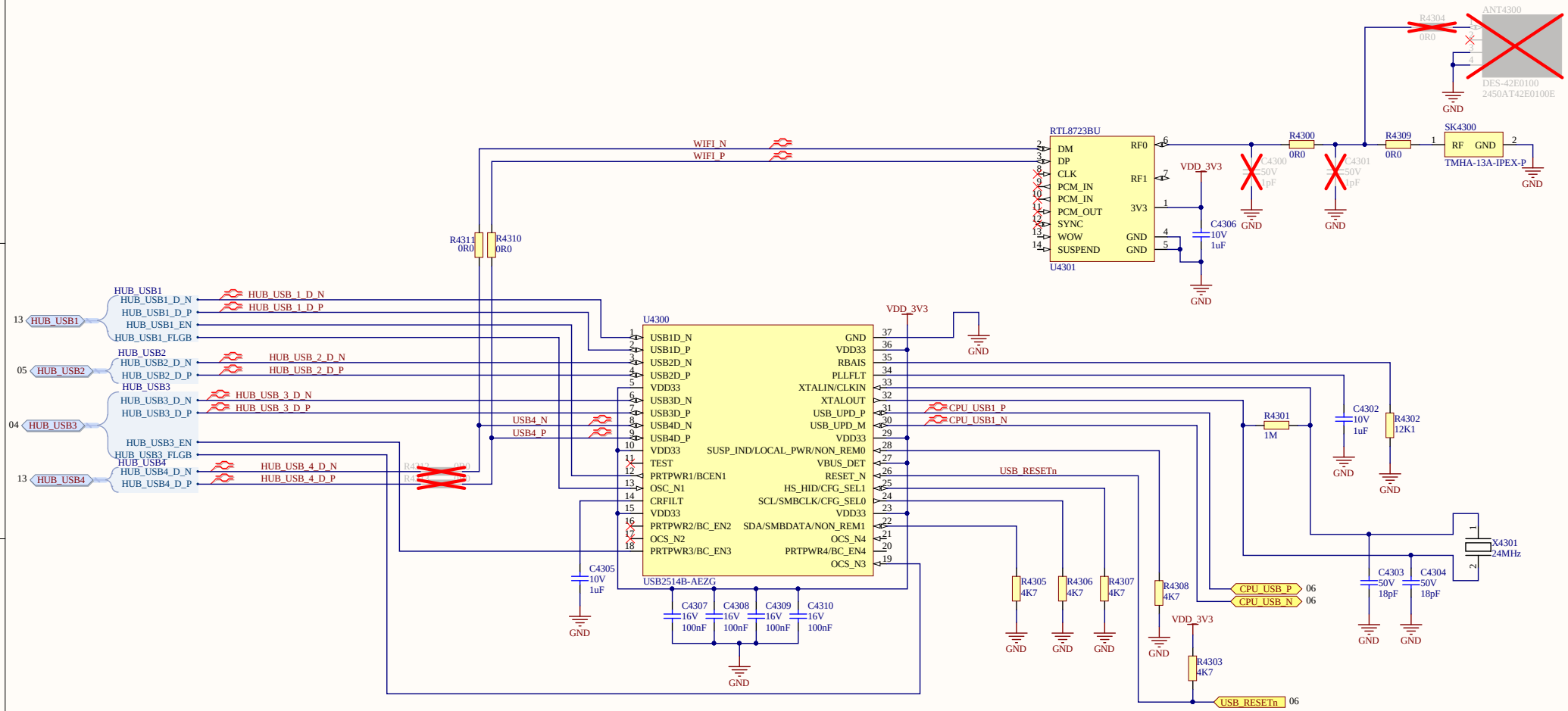

4300 - 4399

Title: USB Hub			
Size: A3	Date: 26/01/2017	SanCloud Ltd 164 Walkden Road Worsley Manchester M28 7DP United Kingdom	
Drawn by	David Fields		
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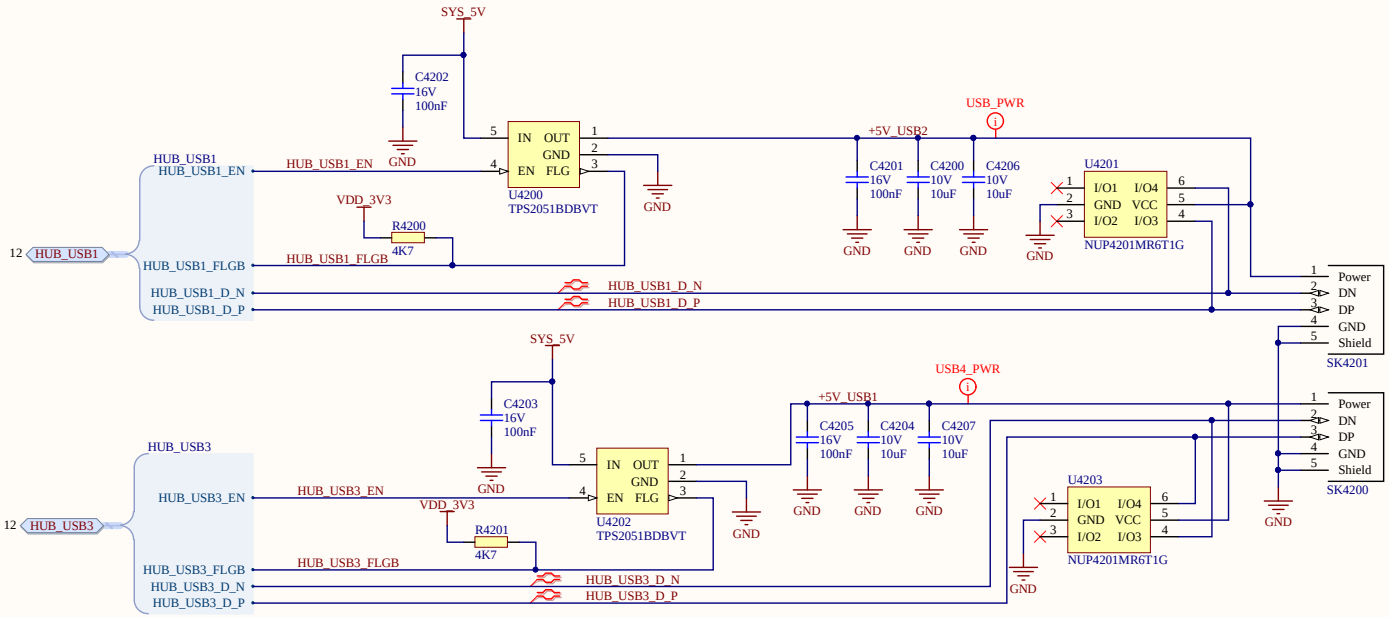

4200 - 4299

Title: USB Ports			
Size: A3	Date: 26/01/2017	SanCloud Ltd 164 Walkden Road Worsley Manchester M28 7DP United Kingdom	
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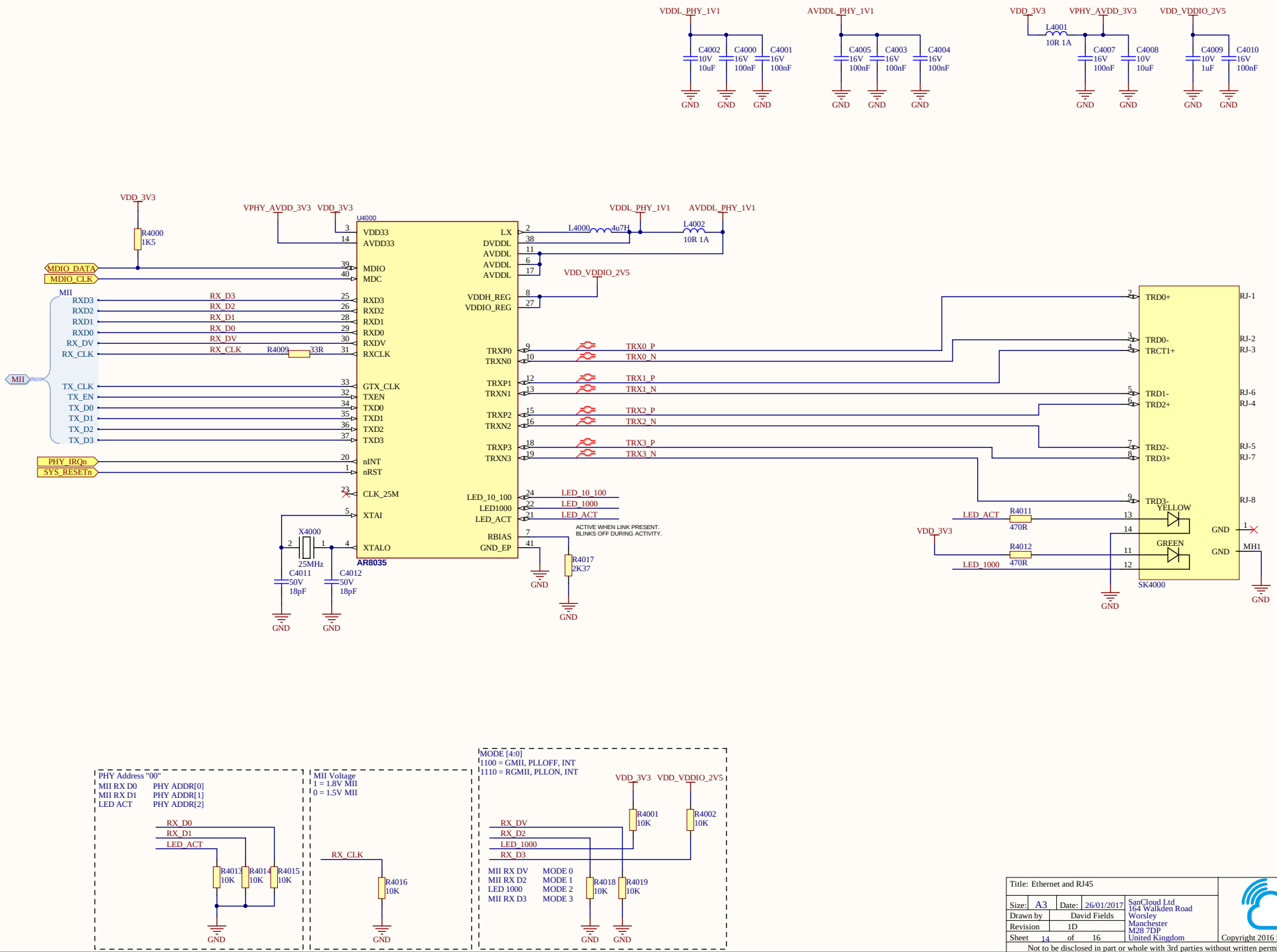

Title: Ethernet and RJ45			
Size: A3	Date: 26/01/2017	SanCloud Ltd 164 Walkden Road Worsley Manchester M28 7DP United Kingdom	
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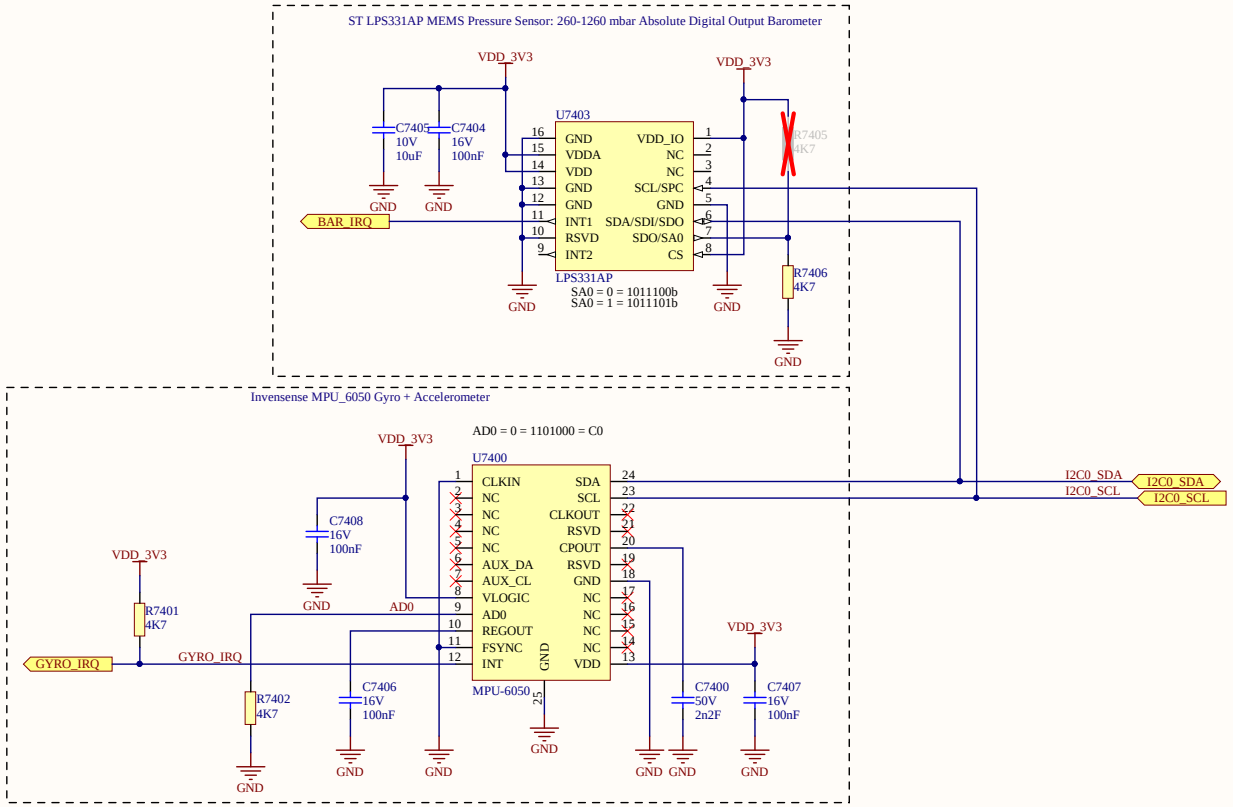

Title: Accelerometer and Barometer			
Size: A3	Date: 26/01/2017	SanCloud Ltd 164 Walkden Road Worsley Manchester M28 7DP United Kingdom	
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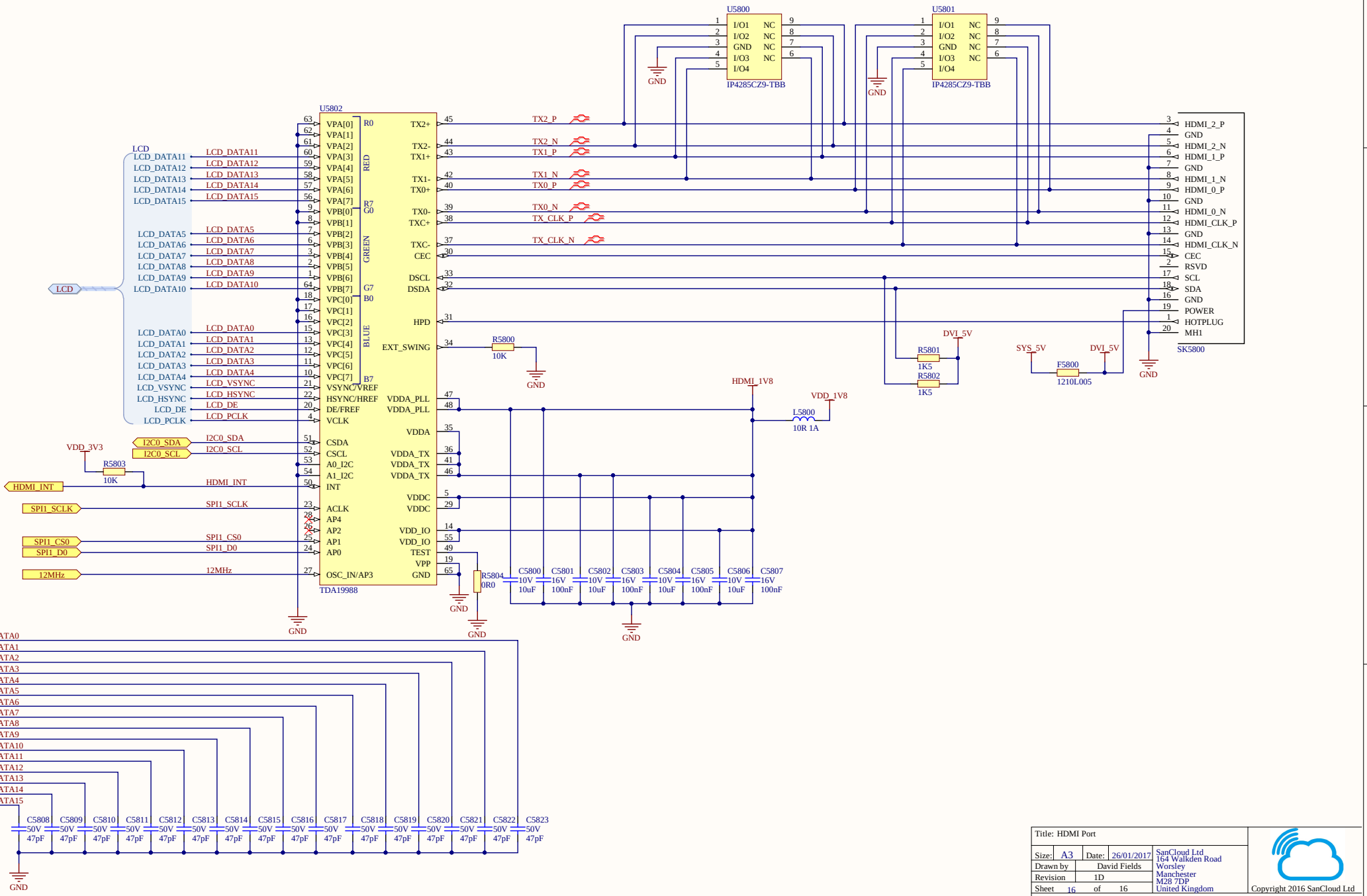

Title:	HDMI Port
Size:	A3
Date:	26/01/2017
Drawn by	David Fields
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