DIGITAL QUESTIONS

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ASIC WORLD Directory

Digital
Tutorial
Questions
Tools
Books
Links

Home
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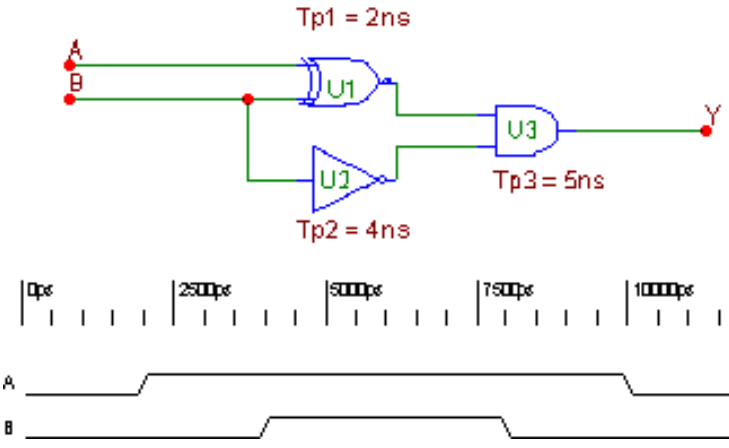
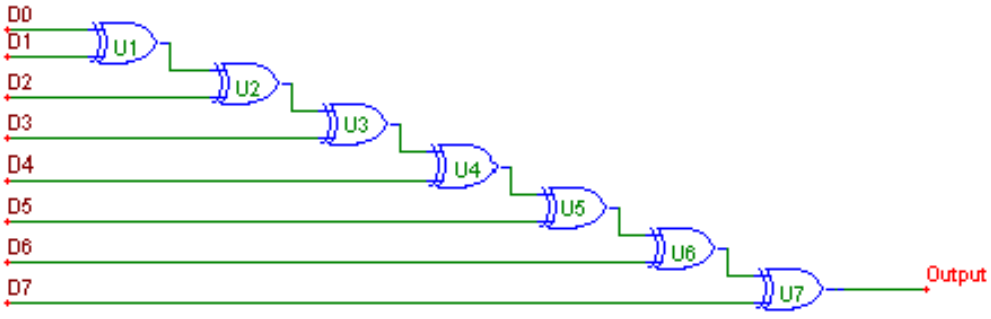
Sample Digital Questions Asked in Interviews

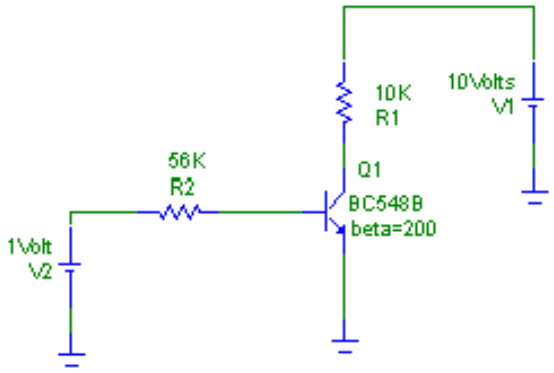
- What is the output of AND gate in the circuit below, when A and B are as in waveform? Where, Tp is gate delay of respective gate.



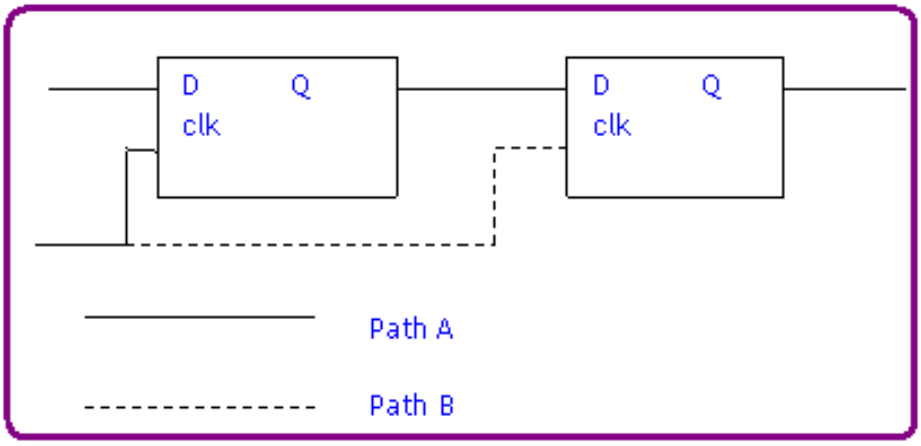
- Identify the below circuit, and its limitation ?



- What is the current though the resistor R1 (Ic) ?

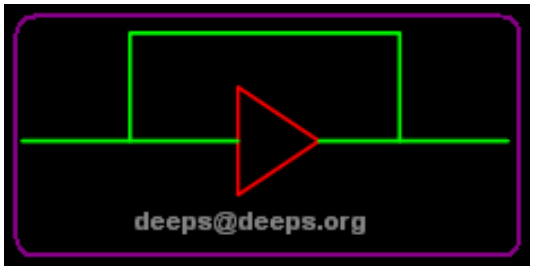


- Referring to the diagram below, briefly explain what will happen if the propagation delay of the clock signal in path B is much too high compare to path A. How do we solve this problem if the propagation delay of path B can not be reduced ?

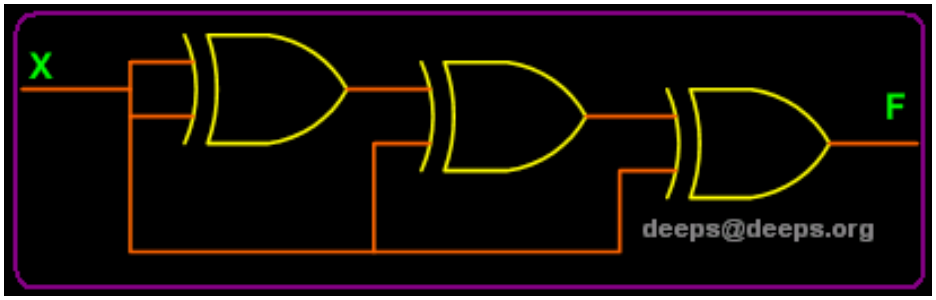


- What is the function of a D flip-flop, whose inverted output is connected to its input ?
- Design a circuit to divide input frequency by 2 ?
- Design a divide-by-3 sequential circuit with 50% duty cycle.?
- What are the different types of adder implementation ?
- Draw a Transmission Gate-based D-Latch ?
- Give the truth table for a Half Adder. Give a gate level implementation of the same.

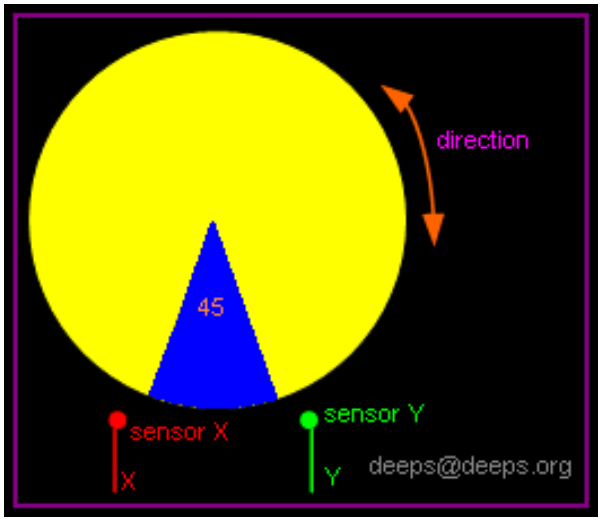
- What is the purpose of the buffer in below circuit, is it necessary/redundant to have buffer ?



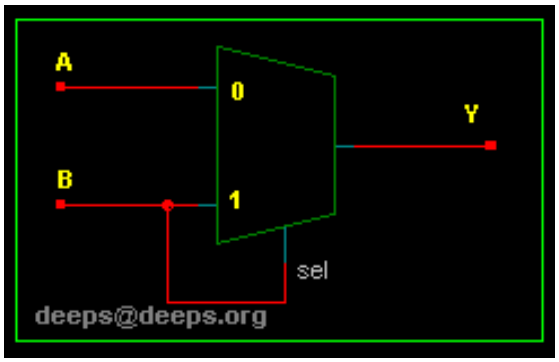
- What is output of the below circuit, assuming that value of 'X' is not known ?



- Consider a circular disk as shown in figure below with two sensors mounted X, Y and blue shade painted on the disk for a angle of 45 degree. Design a circuit with minimum number of gates to detect the direction of rotation.

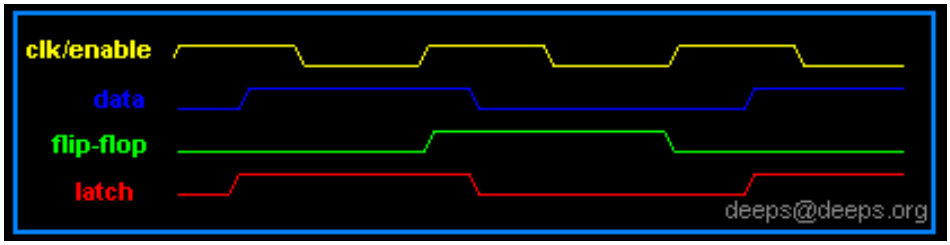


- Design a OR gate from 2:1 MUX.

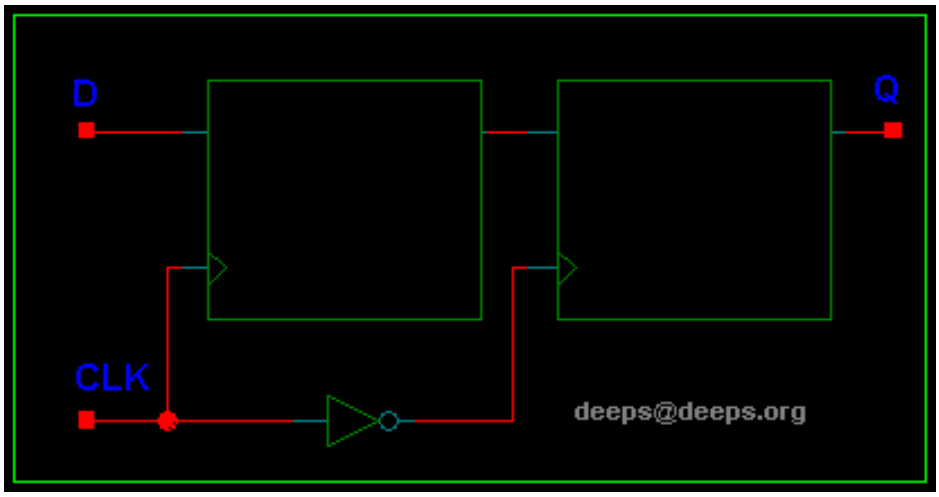


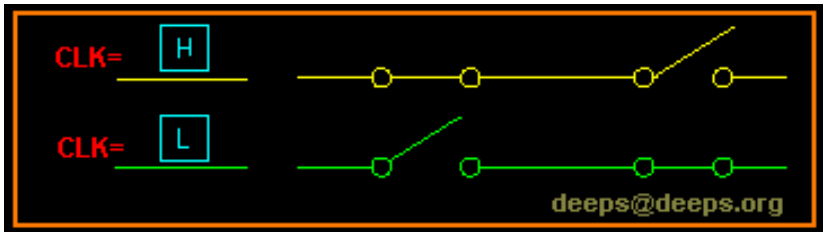
What is the difference between a LATCH and a FLIP-FLOP ?

- Latch is a level sensitive device and flip-flop is edge sensitive device
- Latch is sensitive to glitches on enable pin, where as flip-flop is immune to gltiches.
- Latches take less gates (also less power) to implement then flip-flops
- Latches are faster then flip-flops



Design a D Flip-Flop from two latches.





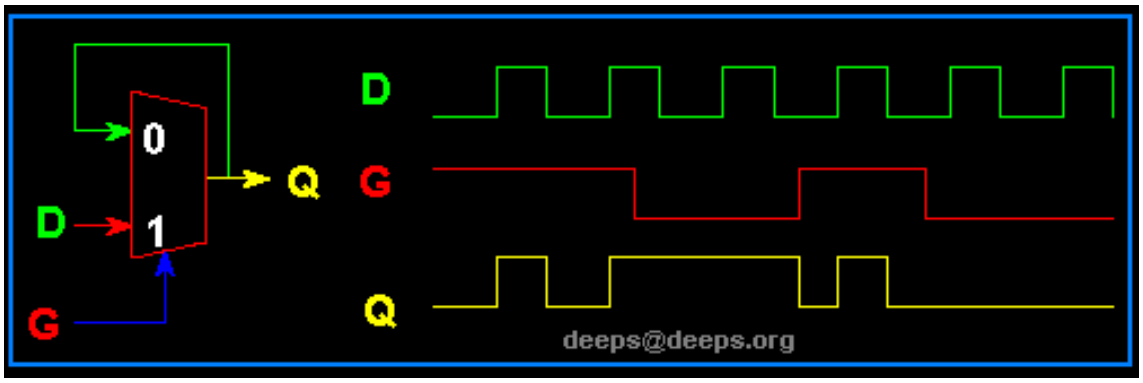
Design a 2 bit counter using D Flip-Flop.

Transition Table → Next State Transistion Table → K-map → circuit

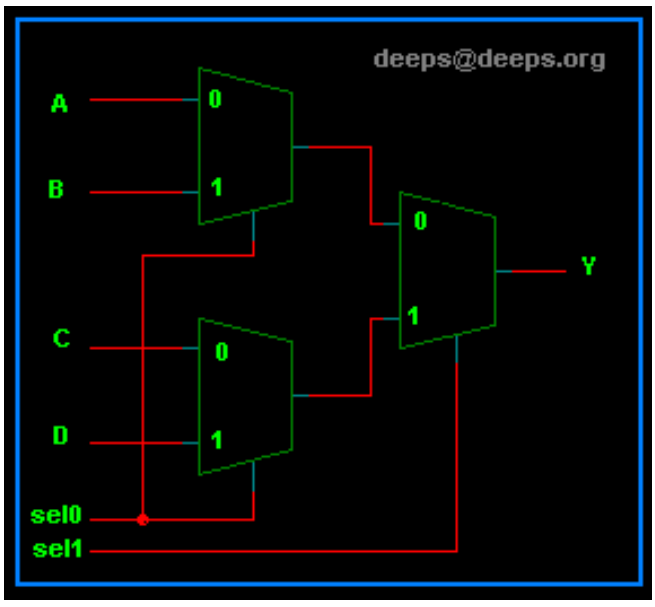
What are the two types of delays in any digital system ?

Wire Delay and Gate Delay

Design a Transparent Latch using a 2:1 Mux.



Design a 4:1 Mux using 2:1 Mux's and some combo logic.



What is metastable state ? How does it occur ?

Refer Tidbits section

What is metastablity ?

Refer Tidbits section

- Design a 3:8 decoder
- Design a FSM to detect sequence "101" in input sequence.
- Convert NAND gate into Inverter, in two different ways.
- Design a D and T flip flop using 2:1 mux, use of other components not allowed, just the mux.
- Design a divide by two counter using D-Latch.
- Design D Latch from SR flip-flop.
- Define Clock Skew , Negative Clock Skew, Positive Clock Skew ?
- What is Race Condition ?
- Design a 4 bit Gray Counter ?
- Design 4-bit Synchronous counter, Asynchronous counter ?
- Design a 16 byte Asynchronous FIFO?
- What is the difference between a EEPROM and FLASH ?
- What is the difference between a NAND-based Flash and NOR-based Flash ?
- You are given a 100 MHz clock , Design a 33.3 MHz clock with and without 50 % duty cycle?
- Design a Read on Reset System ?
- Which one is superior Asynchronous Reset or Synchronous Reset, Explain ?
- Design a State machine for Traffic Control at a Four point Junction ?

Do you have any Comments? mail me at: deepak@asic-world.com