CMOS interview questions.

1) What is latch up?

Latch-up pertains to a failure mechanism wherein a parasitic thyristor (such as a parasitic silicon controlled rectifier, or SCR) is inadvertently created within a circuit, causing a high amount of current to continuously flow through it once it is accidentally triggered or turned on. Depending on the circuits involved, the amount of current flow produced by this mechanism can be large enough to result in permanent destruction of the device due to electrical overstress (EOS) .

2)Why is NAND gate preferred over NOR gate for fabrication?

NAND is a better gate for design than NOR because at the transistor level the mobility of electrons is normally three times that of holes compared to NOR and thus the NAND is a faster gate. Additionally, the gate-leakage in NAND structures is much lower. If you consider t_phl and t_plh delays you will find that it is more symmetric in case of NAND (the delay profile), but for NOR, one delay is much higher than the other(obviously t_plh is higher since the higher resistance p mos's are in series connection which again increases the resistance).

3)What is Noise Margin? Explain the procedure to determine Noise Margin

The minimum amount of noise that can be allowed on the input stage for which the output will not be effected.

4)Explain sizing of the inverter?

In order to drive the desired load capacitance we have to increase the size (width) of the inverters to get an optimized performance.

5) How do you size NMOS and PMOS transistors to increase the threshold voltage?

6) What is Noise Margin? Explain the procedure to determine Noise Margin?

The minimum amount of noise that can be allowed on the input stage for which the output will not be effected.

7) What happens to delay if you increase load capacitance?

delay increases.

8)What happens to delay if we include a resistance at the output of a CMOS circuit?

Increases. (RC delay)

9)What are the limitations in increasing the power supply to reduce delay?

The delay can be reduced by increasing the power supply but if we do so the heating effect comes because of excessive power, to compensate this we have to increase the die size which is not practical.

10)How does Resistance of the metal lines vary with increasing thickness and increasing length?

R = (*l) / A.

11)For CMOS logic, give the various techniques you know to minimize power consumption?

Power dissipation=CV2f ,from this minimize the load capacitance, dc voltage and the operating frequency.

12) What is Charge Sharing? Explain the Charge Sharing problem while sampling data from a Bus?

In the serially connected NMOS logic the input capacitance of each gate shares the charge with the load capacitance by which the logical levels drastically mismatched than that of the desired once. To eliminate this load capacitance must be very high compared to the input capacitance of the gates (approximately 10 times).

13)Why do we gradually increase the size of inverters in buffer design? Why not give the output of a circuit to one large inverter?

Because it can not drive the output load straight away, so we gradually increase the size to get an optimized performance.

14)What is Latch Up? Explain Latch Up with cross section of a CMOS Inverter. How do you avoid Latch Up?

Latch-up is a condition in which the parasitic components give rise to the Establishment of low resistance conducting path between VDD and VSS with Disastrous results.

15) Give the expression for CMOS switching power dissipation?

CV2

16) What is Body Effect?

In general multiple MOS devices are made on a common substrate. As a result, the substrate voltage of all devices is normally equal. However while connecting the devices serially this may result in an increase in source-to-substrate voltage as we proceed vertically along the series chain (Vsb1=0, Vsb2 0).Which results Vth2>Vth1.

17) Why is the substrate in NMOS connected to Ground and in PMOS to VDD?

we try to reverse bias not the channel and the substrate but we try to maintain the drain,source junctions reverse biased with respect to the substrate so that we dont loose our current into the substrate.

18) What is the fundamental difference between a MOSFET and BJT ?

In MOSFET, current flow is either due to electrons(n-channel MOS) or due to holes(p-channel MOS) - In BJT, we see current due to both the carriers.. electrons and holes. BJT is a current controlled device and MOSFET is a voltage controlled device.

19)Which transistor has higher gain. BJT or MOS and why?

BJT has higher gain because it has higher transconductance.This is because the current in BJT is exponentially dependent on input where as in MOSFET it is square law.

20)Why do we gradually increase the size of inverters in buffer design when trying to drive a high capacitive load?
Why not give the output of a circuit to one large inverter?

We cannot use a big inverter to drive a large output capacitance because, who will drive the big inverter? The signal that has to drive the output cap will now see a larger gate capacitance of the BIG inverter.So this results in slow raise or fall times .A unit inverter can drive approximately an inverter thats 4 times bigger in size. So say we need to drive a cap of 64 unit inverter then we try to keep the sizing like say 1,4,16,64 so that each inverter sees a same ratio of output to input cap. This is the prime reason behind going for progressive sizing.

21)In CMOS technology, in digital design, why do we design the size of pmos to be higher than the nmos.What determines the size of pmos wrt nmos. Though this is a simple question try to list all the reasons possible?

In PMOS the carriers are holes whose mobility is less[aprrox half] than the electrons, the carriers in NMOS. That means PMOS is slower than an NMOS. In CMOS technology, nmos helps in pulling down the output to ground ann PMOS helps in pulling up the output to Vdd. If the sizes of PMOS and NMOS are the same, then PMOS takes long time to charge up the output node. If we have a larger PMOS than there will be more carriers to charge the node quickly and overcome the slow nature of PMOS . Basically we do all this to get equal rise and fall times for the output node.

22)Why PMOS and NMOS are sized equally in a Transmission Gates?

In Transmission Gate, PMOS and NMOS aid each other rather competing with each other. That's the reason why we need not size them like in CMOS. In CMOS design we have NMOS and PMOS competing which is the reason we try to size them proportional to their mobility.

23)All of us know how an inverter works. What happens when the PMOS and NMOS are interchanged with one another in an inverter?

I have seen similar Qs in some of the discussions. If the source & drain also connected properly...it acts as a buffer. But suppose input is logic 1 O/P will be degraded 1 Similarly degraded 0;

24)A good question on Layouts. Give 5 important Design techniques you would follow when doing a Layout for Digital Circuits?

a)In digital design, decide the height of standard cells you want to layout.It depends upon how big your transistors will be.Have reasonable width for VDD and GND metal paths.Maintaining uniform Height for all the cell is very important since this will help you use place route tool easily and also incase you want to do manual connection of all the blocks it saves on lot of area.
b)Use one metal in one direction only, This does not apply for metal

1. Say you are using metal 2 to do horizontal connections, then use metal 3 for vertical connections, metal4 for horizontal, metal 5 vertical etc...
c)Place as many substrate contact as possible in the empty spaces of the layout.
d)Do not use poly over long distances as it has huge resistances unless you have no other choice.
e)Use fingered transistors as and when you feel necessary.
f)Try maintaining symmetry in your design. Try to get the design in BIT Sliced manner.

25)What is metastability? When/why it will occur?Different ways to avoid this?

Metastable state: A un-known state in between the two logical known states.This will happen if the O/P cap is not allowed to charge/discharge fully to the required logical levels.
One of the cases is: If there is a setup time violation, metastability will occur,To avoid this, a series of FFs is used (normally 2 or 3) which will remove the intermediate states.

26)Let A and B be two inputs of the NAND gate. Say signal A arrives at the NAND gate later than signal B. To optimize delay of the two series NMOS inputs A and B which one would you place near to the output?

The late coming signals are to be placed closer to the output node ie A should go to the nmos that is closer to the output.