ASIC interview questions

1. what is the difference between mealy and moore state-machines

Both kinds of machines consist of flip-flop whose inputs are logical combinations of the input signals and the values of the flip-flop Q and Q' outputs.They differ in how the outputs of the machine are determined. For a Moore machine the outputs depend only on the Q and Q' flip-flop outputs. For a Mealy machine the outputs may depend on both the Q and Q' flip-flop outputs and the current inputs. Thus the outputs of a Mealy machine can change whenever the inputs change, even if this occurs "between clock pulses". In the figure, we see that the output of a Moore machine is associated with the state itself, whereas with a Mealy machine the output is associated with both the state the machine is now in and the current values of the inputs.

2. How to solve setup & Hold violations in the design

To solve setup violation

1. optimizing/restructuring combination logic between the flops.
2. Tweak flops to offer lesser setup delay [DFFX1 -> DFFXx]
3. Tweak launch-flop to have better slew at the clock pin, this will make CK->Q of launch flop to be fast there by helping fixing setup violations
4. Play with skew [tweak clock network delay, slow-down clock to capturing flop and fasten the clock to launch-flop](otherwise called as Useful-skews)

To solve Hold Violations

1. Adding delay/buffer[as buffer offers lesser delay, we go for spl Delay cells whose functionality Y=A, but with more delay]
2. Making the launch flop clock reaching delayed

3. Also, one can add lockup-latches [in cases where the hold time requirement is very huge, basically to avoid data slip]

3. What is antenna Violation & ways to prevent it

During the process of plasma etching, charges accumulate along the metal strips. The longer the strips are, the more charges are accumulated. IF a small transistor gate connected to these long metal strips, the gate oxide can be destroyed (large electric field over a very thin electric) , This is called as Antenna violation.

The ways to prevent is , by making jogging the metal line, which is atleast one metal above the layer to be protected. If we want to remove antenna violation in metal2 then need to jog it in metal3 not in metal1. The reason being while we are etching metal2, metal3 layer is not laid out. So the two
pieces of metal2 got disconnected. Only the piece of metal connected to gate have charge to gate. When we laydown metal3, the remaining portion of metal got charge added to metal3. This is called accumulative antenna effect.
Another way of preventing is adding reverse Diodes at the gates

4. how to estimate the width of the power-strap of the power-grid.

A good information :
http://www.vlsitechnology.org/html/irdrop_1.html

5. what is tie-high and tie-low cells and where it is used

Tie-high and Tie-Low cells are used to connect the gate of the transistor to either power or ground. In deep sub micron processes, if the gate is connected to power/ground the transistor might be turned on/off due to power or ground bounce. The suggestion from foundry is to use tie cells for this purpose. These cells are part of standard-cell library. The cells which require Vdd, comes and connect to Tie high...(so tie high is a power supply cell)...while the cells which wants Vss connects itself to Tie-low.

6. what is the difference between latches and flip-flops based designs

Latches are level-sensitive and flip-flops are edge sensitive. latch based design and flop based design is that latch allowes time borrowing which a tradition flop does not. That makes latch based design more efficient. But at the same time, latch based design is more complicated and has more
issues in min timing (races). Its STA with time borrowing in deep pipelining can be quite complex.

7. What is High-Vt and Low-Vt cells.

Hvt cells are MOS devices with less leakage due to high Vt but they have higher delay than low VT, where as the low Vt cells are devices which have less delay but leakage is high. The thereshold(t) vloltage dictates the transistor switching speed , it matters how much minimum threshold voltage applied can make the transistor switching to active state which results to how fast we can switch the trasistor. disadvantage is it needs to maintain the transistor in a minimum subthreshold voltage level to make ir switch fast so it leads to leakage of current inturn loss of power.

8. What is LEF mean?

LEF is an ASCII data format from Cadence Design inc, to describe a standard cell library. It includes the design rules for routing and the Abstract layout of the cells. LEF file contains the following,

Technology: layer, design rules, via-definitions, metal-capacitance

Site : Site extension

Macros : cell descriptions, cell dimensions, layout of pins and blockages, capacitances

To get further insight to the topic, please check this
http://www.csee.umbc.edu/~cpatel2/links/414/slides/lect03_LEF.pdf

9. what is DEF mean?

DEF is an ASCII data format from Cadence Design inc., to describe Design related information.

10. Steps involved in designing an optimal padring

1. Make sure you have corner-pads, across all the corners of the padring, This is mainly to have the power-continuity as well as the resistance is less .

2. Ensure that the Padring ful-fills the ESD requirement, Identifyh the power-domains, split the domains, Ensure common ground across all the domains.

3. Ensure the padring has ful-filled the SSN(Simultaneous Switching Noise) requirement.

4. Placing Transfer-cell Pads in the cross power-domains, for different height pads, to have rail connectivity.

5. Ensure that the design has sufficient core power-pads.

6. Choose the Drive-strenght of the pads based on the current requirements, timing.

7. Ensure that there is seperate analog ground and power pads.

8. A No-Connection Pad is used to fill out the pad-frame if there is no requirement for I/O's.Extra VDD/GND pads also could be used. Ensure that no Input/output pads are used with un-connected inputs, as they consume power if the inputs float.

9. Ensure that oscillator-pads are used for clock inputs.

10. In-case if the design requirement for source synchronous circuits, make sure that the clock and data pads are of same drive-strength.

11. Breaker-pads are used to break the power-ring, and to isolate the power-structure across the pads.

12. Ensure that the metal-wire connected to the pin can carry sufficient amount of the current, check if more than one metal-layer is necessary to carry the maximum current provided at the pin.

13. In case if required , place pads with capacitance.

11. What is metastability and steps to prevent it.

Metastability is an unknown state it is neither Zero nor One.Metastability happens for the design systems violating setup or hole time requirements. Setup time is a requirement , that the data has to be stable before the clock-edge and hold time is a requirement , that the data has to be stable after the clock-edge. The potential violation of the setup and hold violation can happen when the data is purely asynchronous and clocked synchronously.

Steps to prevent Metastability.

1. Using proper synchronizers(two-stage or three stage), as soon as the data is coming from the asynchronous domain. Using Synchronizers, recovers from the metastable event.

2. Use synchronizers between cross-clocking domains to reduce the possibility from metastability.

3. Using Faster flip-flops (which has narrower Metastable Window).

12. what is local-skew, global-skew,useful-skew mean?

Local skew : The difference between the clock reaching at the launching flop vs the clock reaching the destination flip-flop of a timing-path.

Global skew : The difference between the earliest reaching flip-flop and latest reaching flip-flop for a same clock-domain.

Useful skew: Useful skew is a concept of delaying the capturing flip-flop clock path, this approach helps in meeting setup requirement with in the launch and capture timing path. But the hold-requirement has to be met for the design.

13. What are the various timing-paths which i should take care in my STA runs?

1. Timing path starting from an input-port and ending at the output port(purely combinational path).

2. Timing path starting from an input-port and ending at the register.

3. Timing path starting from an Register and ending at the output-port.

4. Timing path starting from an register and ending at the register.

14. What are the various components of Leakage-power?

1. sub-threshold leakage

-courtesy Khondker

2. gate leakage

-courtesy Khondker

3. reverse biased drain substrate and drain substrate junction band-band tunnelling

-courtesy Khondker

15. What are the various yield-losses in the design?

The yield loss in the design is characterized by

1. Functional yield losses, mainly caused by spot defects , especially (shorts & opens)

2. Parametric yield losses, due to process variations.

16. what is meant by virtual clock definition and why do i need it?

Virtual clock is mainly used to model the I/O timing specification. Based on what clock the output/input pads are passing the data.

For Further Understanding of the concept.

17. What are the various Variations which impacts timing of the design?

18. What are the various Design constraints used while performing Synthesis for a design?

1. Create the clocks (frequency, duty-cycle).

2. Define the transition-time requirements for the input-ports.3

3. Specify the load values for the output ports

4. For the inputs and the output specify the delay values(input delay and ouput delay), which are

already consumed by the neighbour chip.

5. Specify the case-setting (in case of a mux) to report the timing to a specific paths.

6. Specify the false-paths in the design

7. Specify the multi-cycle paths in the design.

8. Specify the clock-uncertainity values(w.r.t jitter and the margin values for setup/hold).

19. Specify few verilog constructs which are not supported by the synthesis tool.

initial, delays, real, force and release, fork join.

20. what are the various capacitances with an MOSFET?

21.Vds-Ids curve for an MOSFET, with increasing Vgs.

22. Basic Operation of an MOSFET.

23. What is Channel length Modulation?

-courtesy Khondker

24. what is body effect?

Increase in Vt(threshold voltage) , due to increase in Vs(voltage at source), is called as

body effect.

-courtesy Khondker

25. What is latchup in CMOS design and ways to prevent it?

To best understand the concept behind the latchup, we need to understand the concept behind SCR(Silicon Controlled Rectifiers), and how to model the basic transistor in an SCR structure and on what conditions SCR structures are created in the CMOS design process and its effects and what are the ways used to prevent it in the design-phase.An SCR is an acronym for Silicon Controlled Rectifier. It works similar to a typical diode, but is controlled similar to a bipolar transistor as far as connections go. Connection points are Anode [A], Cathode [K], and Gate [G]. The SCR is made up of two "P-N" junctions with a "Gate" attachment between them. The gate is connected between the two P-N junctions with a current waiting in the forward bias direction [+ to -] and the voltage is above 1-volt. A momentary pulse to the gate will cause the SCR to conduct and current will flow across the device until the value changes.

-courtesy Kenneth R. Laker

For further Reading on the Concept