DTEK-V Processor Information

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Introduction

The DTEK-V board has a RISC-V compatible with the R32IMZICSR extensions. The board has been designed specifically with the IS1500 intended learning outcomes (ILOs) in mind and is used for the project and laboratory exercises in the course. It has been implemented using the Terasic DE10-Lite board on an Intel MAX 10 10M50DAF484C7G FPGA Device. The board is interfaced using the virtual JTAG interface through custom software for uploading-, downloading-, and running RISC-V binaries compiled by the GNU C Compiler.

Processor Information

Type	RISC-V
Extensions	I, M, ZICSR
Stages	Fetch/Dec., Exe., Mem/WB
Clock Freq.	30 Mhz
Throughput	1 IPC (peak)
Forwarding	From Exec and Mem/WB
L1 I-Cache	2 kB DM, 32B block size
L1 D-Cache	2 kB DM, 32B block size, Write-through policy

Exceptions

#0	Instruction address misalign
#2	Illegal instruction
#11	Environment call from M

Memory Mapped I/O

I/O Device	Memory Address	Type	IRQ #
SDRAM	0x0000000-0x3ffffff	Memory	-
LEDs	0x4000000-0x400000f	Output	
Switches	0x4000010-0x400001f	Input	17
Timer	0x4000020-0x400003f	Device	16
UART	0x4000040-0x4000047	Device	
Hex Displays (6 display)	0x4000050-0x400005f + (#display * 0x10)	Output	
Mutex	0x40000c0-0x40000c7	Device	
Button	0x40000d0-0x40000df	Input	18
GPIO (2x20)	0x40000e0-0x40000ef 0x40000f0-0x40000ff	Input/ Output	
VGA DMA	0x4000100-0x400010f	Device	
VGA Buffer	0x8000000-0x80257ff	Device	

Hardware Counters

mcycle	# CPU cycle counter
minstret	# Instruction executed
mhpmcounter3	# Memory instructions
mhpmcounter4	# I-cache misses
mhpmcounter5	# D-cache misses
mhpmcounter6	# I-cache stalls
mhpmcounter7	# D-cache stalls
mhpmcounter8	# Data-hazard stalls
mhpmcounter9	# ALU stalls

Resource Utilization

# LEs	39,168 (79%)
# Memory	1,322,322 (176 M9K, 97%)
# DSP blocks	24 (8%)