Evolution of CSMA Protocols for the IEEE 802.11 Standard

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Abstract—In this paper we present the requirements of candidate protocols to replace the pervasive CSMA/CA medium access control. We discuss the possibility of further preventing collisions and provide an overview of the related work. We specify protocols that are candidates of replacing CSMA/CA in pseudocode and use simulation to assess performance metrics such as throughput, fairness and collision probability.

I. Introduction

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A candidate to replace CSMA/CA should

- Provide performance advantages, either in the form of throughput or short term fairness.
- Be backward compatible with current implementation.
- Support a large number of simultaneous contenders.
- Be simple a simple evolution implementation to ease the transition and reduce time to market (Optional but desirable).

II. RELATED WORK

Since the popularization of IEEE 802.11, several papers have proposed modifications to the contention protocol that is used for sharing the medium. They can be categorized in three groups regarding the approach they use. The first one prevents that the contention window is reset to its minimum value after successful transmissions. Examples of this first group include [1], [2]. This solution improves throughput in saturation conditions at the price of lowering short term fairness.

The second groups involves the accurate estimation of the number of contenders to adjust the contention parameters. Two examples of this group are [3], [4]. This approach offers some throughput and fairness gains at the expense of increased implementation complexity. As the number of contenders is estimated relying on the number of collisions, the presence of channel errors further complicates the estimation. Furthermore, there is a fundamental trade-off between the accuracy and the reaction time of the estimation.

The aforementioned solutions are not able to fairly share the medium with legacy devices. In fact, these proposals are, generally speaking, less aggressive than the currently implemented protocol. Consequently, in a hypothetical mixed network in which the new and old protocols coexist, the new stations would receive a smaller share of the available bandwidth in a scenario.

A more important limitation of the solutions exposed so far is that the throughput is bounded by that of CSMA/CA with optimal configuration [3], [5]. In the present paper we focus on a third group of solutions that delivers throughput above the maximum attainable by CSMA/CA.

This third group of solutions uses a deterministic backoff after successful transmissions to further reduce the chances of collisions. Under certain conditions, collision-free operation is reached. It was introduced in [6] and a more detailed analysis that includes both saturated and non-saturated conditions is presented in [7]. A more in-depth study is carried out in [8], including realistic elements such as clear channel assessment errors. Different aspects of fairness are addressed in [8]–[10]. The performance in realistic channels taking into account the Auto Rate Fallback mechanism is evaluated [11], [12].

Even though initial research efforts where focused on the WLAN collision problem, more recent papers try to extend the idea to multi-hop networks. In [13], the multi-hop slotted case explored. The more realistic situation in multi-hop networks in which the time is not slotted is studied in [14].

The same principles that we exploit to prevent collisions in WLANs can be used in other areas of radio resource management in wireless area networks [15]–[18].

In all the previous work on collision-free operation in WLANs mentioned so far, there is the limitation that the number of contenders should not exceed the value of the deterministic backoff used after successful transmissions. If this value is exceeded, it is no longer possible to achieve collision-free operation. A first solution to solve this problem is presented in [19], but it requires the presence of a central entity (typically the access point) that instructs the other nodes to adjust the value of their deterministic backoff.

In the present paper, we study a completely distributed solution to accommodate a large number of contenders in a fair collision-free fashion.

III. ENHANCED CSMA

In this section we describe the CSMA/CA protocol as it is currently implemented in the IEEE 802.11 and an evolution of the standard that satisfies the four requirements specified in the introduction. Therefore, the presented protocol is a valid

```
1 while True do
         r \leftarrow 0;
                                                                                              1 while True do
 2
         s \leftarrow 0;
                                                                                                      r \leftarrow 0:
                                                                                              2
 3
         b \leftarrow \mathcal{U}[0, 2^s \text{CW}_{\text{min}} - 1];
                                                                                                       s \leftarrow 0;
 4
                                                                                              3
         while there is a packet to transmit do
                                                                                                       b \leftarrow \mathcal{U}[0, 2^s \text{CW}_{\text{min}} - 1];
 5
                                                                                              4
                                                                                                       while there is a packet to transmit do
               repeat
 6
                                                                                              5
                    while b > 0 do
                                                                                                            repeat
                                                                                              6
                          wait 1 slot;
                                                                                                                 while b > 0 do
                                                                                              7
 8
                          b \leftarrow b - 1;
                                                                                                                      wait 1 slot;
                                                                                              8
                                                                                                                       b \leftarrow b - 1;
                    Attempt transmission;
10
                                                                                                                 Attempt transmission;
                    if success then
                                                                                             10
11
                                                                                                                 if success then
                         r \leftarrow 0;
12
                                                                                             11
                          s \leftarrow 0;
                                                                                                                       r \leftarrow 0;
13
                                                                                             12
                          b \leftarrow \mathcal{U}[0, 2^s \text{CW}_{\text{min}} - 1];
                                                                                                                       b \leftarrow (2^s \text{CW}_{\text{min}})/2;
14
                                                                                             13
15
                    else
                                                                                             14
                                                                                                                 else
                         r \leftarrow r + 1;
                                                                                                                       r \leftarrow r + 1;
16
                                                                                             15
                          s \leftarrow \min r(s+1,S);
                                                                                                                       s \leftarrow \min r(s+1,S);
17
                                                                                             16
                         b \leftarrow \mathcal{U}[0, 2^s \text{CW}_{\text{min}} - 1];
                                                                                                                      b \leftarrow \mathcal{U}[0, 2^s \text{CW}_{\text{min}} - 1];
18
                                                                                             17
               until (r = R) or (success);
                                                                                                            until (r = R) or (success);
19
                                                                                             18
               if r=R then
                                                                                                            if r=R then
20
                                                                                             19
                    Discard packet;
                                                                                                                 Discard packet;
21
                                                                                             20
                    r \leftarrow 0;
                                                                                                                 r \leftarrow 0;
22
                                                                                             21
                                                                                                                 b \leftarrow \mathcal{U}[0, 2^s \text{CW}_{\min} - 1];
                    s \leftarrow 0;
23
                                                                                             22
                    b \leftarrow \mathcal{U}[0, 2^s \text{CW}_{\text{min}} - 1];
24
                                                                                                          Algorithm 3: CSMA/ECA with hysteresis
```

Algorithm 1: CSMA/CA

Algorithm 2: CSMA/ECA

```
1 while True do
                                                                                           1 while True do
 2
         r \leftarrow 0;
         s \leftarrow 0;
                                                                                                   r \leftarrow 0;
 3
         b \leftarrow \mathcal{U}[0, 2^s \text{CW}_{\text{min}} - 1];
                                                                                                   s \leftarrow 0;
                                                                                           3
 4
                                                                                                   b \leftarrow \mathcal{U}[0, 2^s \text{CW}_{\min} - 1];
         while there is a packet to transmit do
 5
                                                                                           4
                                                                                                   while there is a packet to transmit do
 6
              repeat
                                                                                           5
                    while b > 0 do
                                                                                           6
                                                                                                         repeat
                         wait 1 slot;
                                                                                           7
                                                                                                              while b > 0 do
 8
                        b \leftarrow b - 1;
                                                                                                                   wait 1 slot;
 9
                                                                                           8
                                                                                           9
                                                                                                                  b \leftarrow b - 1;
                    Attempt transmission;
10
                   if success then
                                                                                                              Attempt transmission of 2^s packets;
11
                                                                                          10
                        r \leftarrow 0;
                                                                                                              if success then
12
                                                                                          11
                         s \leftarrow 0;
                                                                                                                   r \leftarrow 0;
                                                                                          12
13
                        b \leftarrow (2^s \text{CW}_{\text{min}})/2;
                                                                                                                   b \leftarrow (2^s \text{CW}_{\text{min}})/2;
                                                                                          13
14
                                                                                                              else
                   else
15
                                                                                          14
                         r \leftarrow r + 1;
                                                                                          15
                                                                                                                   r \leftarrow r + 1;
16
                         s \leftarrow \min r(s+1,S);
                                                                                                                   s \leftarrow \min r(s+1,S);
17
                                                                                          16
                                                                                                                 b \leftarrow \mathcal{U}[0, 2^s \mathrm{CW}_{\min} - 1];
                        b \leftarrow \mathcal{U}[0, 2^s \text{CW}_{\text{min}} - 1];
                                                                                          17
18
              until (r = R) or (success);
                                                                                                         until (r = R) or (success);
19
                                                                                          18
              if r=R then
                                                                                                         if r=R then
20
                                                                                          19
                   Discard packet;
                                                                                                              Discard packet;
21
                                                                                          20
                   r \leftarrow 0;
22
                                                                                          21
                                                                                                              r \leftarrow 0;
                                                                                                              b \leftarrow \mathcal{U}[0, 2^s \text{CW}_{\min} - 1];
23
                    s \leftarrow 0;
                                                                                          22
                   b \leftarrow \mathcal{U}[0, 2^s \text{CW}_{\min} - 1];
24
                                                                                             Algorithm 4: CSMA/ECA with hysteresis and fair-share
```

candidate to replace CSMA/CA in the upcoming revisions of the standard.

There are three changes in the new protocol compared to the legacy one. Firstly, a deterministic backoff is used after successful transmissions. Secondly, the backoff stage is not reset after a packet is serviced. The backoff stage is reset only when the station leaves the contention because it has no packet to be transmitted. And thirdly, the number of packets transmitted in every transmission attempt is a function of the backoff stage. Note that current standards already support the transmission of multiple packets in a single slot.

In the following we describe the original protocol and then we describe each of the modifications that we propose, one by one.

Algorithm 1 describes the CSMA/CA algorithm that is used in current networks. When a station joins the contention it initializes the retry attempt counter r and the backoff stage s to zero. The backoff counter b is initialized using a uniform random distribution and a contention window. After each collision, the retry attempt counter and the backoff stage counter are incremented. As a consequence of the incremented backoff stage, a larger contention window is used. Note that there is maximum backoff stage S and a maximum retry limit S. When the maximum retry limit is reached the packet is discarded, S0 and S1 are reset and a new value for S1 is computed. Similarly, if the packet is successfully transmitted, the S2 and S3 recounters are reset and a new random backoff counter is computed.

Algorithm 2 describes CSMA/ECA in which a deterministic backoff is used after successful transmission. The only change with respect to CSMA/CA is in line 14, where the deterministic assignment takes place.

Hysteresis is included in 3. Adding hysteresis is as simple as removing lines 13 and 23 from Algorithm 2. Note that when hysteresis is used, the backoff stage is reset only when the node has no packet to serve.

Finally, fair-share is implemented in 4. Line 10 of 3 is modified to increase the number of transmitted packets from one to 2^s .

IV. PERFORMANCE EVALUATION

V. CONCLUSION

The conclusion goes here.

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