

Wireless MAC Processor technical Overview



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What is the Wireless MAC Processor

The WMP is a special-purpose processor devised to execute MAC programs. It permits a clear decoupling between protocol logic and the platform. The MAC logic is designed and implemented by the programmer using the MAC programming language. The instruction set and the MAC engine pre-developed by the vendor.

MAC Programming Language

eXtended Finite State Machine - XFSM
It is a convenient and compact way to represent the MAC protocol behavior.

Instruction set

ACTIONS - frame management, radio control, time scheduling
TX frame, set PHY params, RX frame, set timer, freeze counter, build header, forge frame, switch channel, etc
EVENTS - available HW/SW signals/interrupts
Busy channel signal, RX indication, inqueued frame, end timer, etc
CONDITIONS - boolean/arithmetic tests on available registers/info
Frame address == X, queue length > 0, ACK received, power level < P, etc

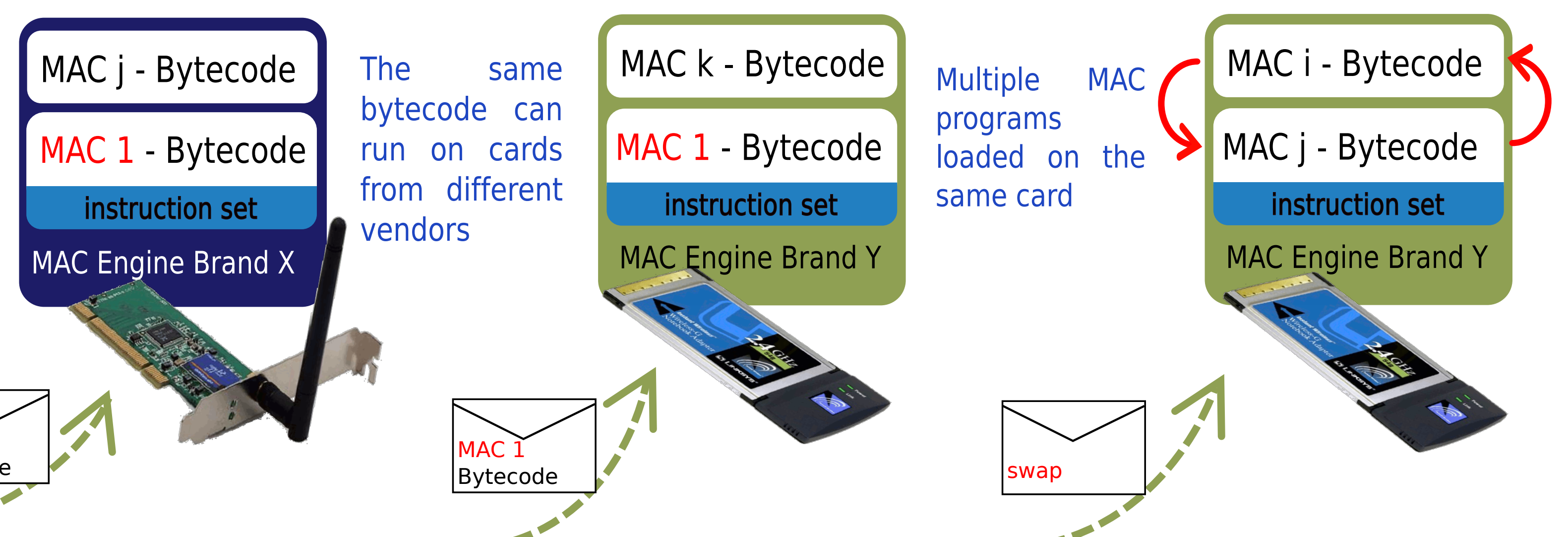
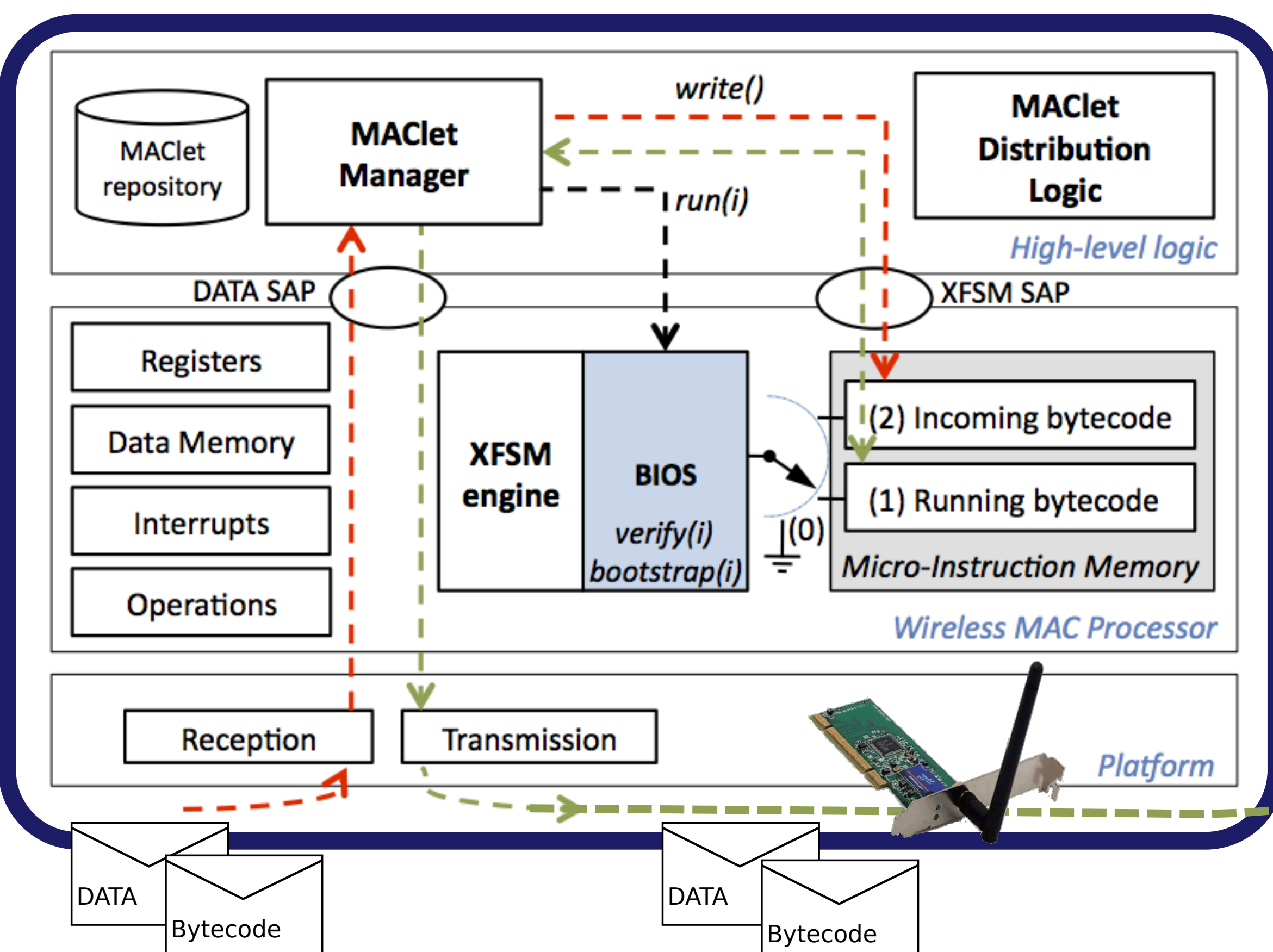
MAC Engine

The MAC Engine is a specialized XFSM executor.
It is integrated in the Wireless Card and handles NIC resources in real-time

closed implementation (manufacturer specific) - open API

WMP architecture and code mobility

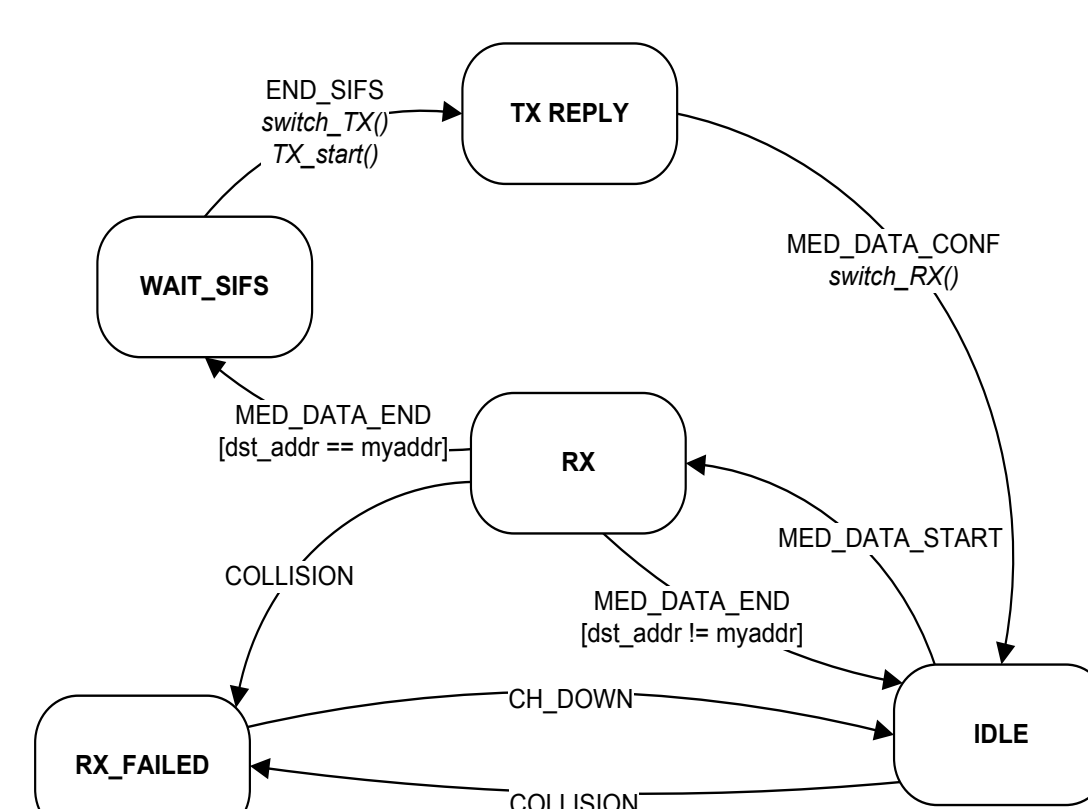
The WMP architecture permits the **design MAC once, run everywhere** paradigm and the decoupling between the platform and the MAC protocol logic.



Graphical XFSM and the bytecode: the two sides of a MAC program

Graphical XFSM

- human-readable and easy to develop;
- uses actions, conditions and events of the instruction set as basic building blocks;
- the WMP-compiler translates the XFSM in bytecode.



Bytecode

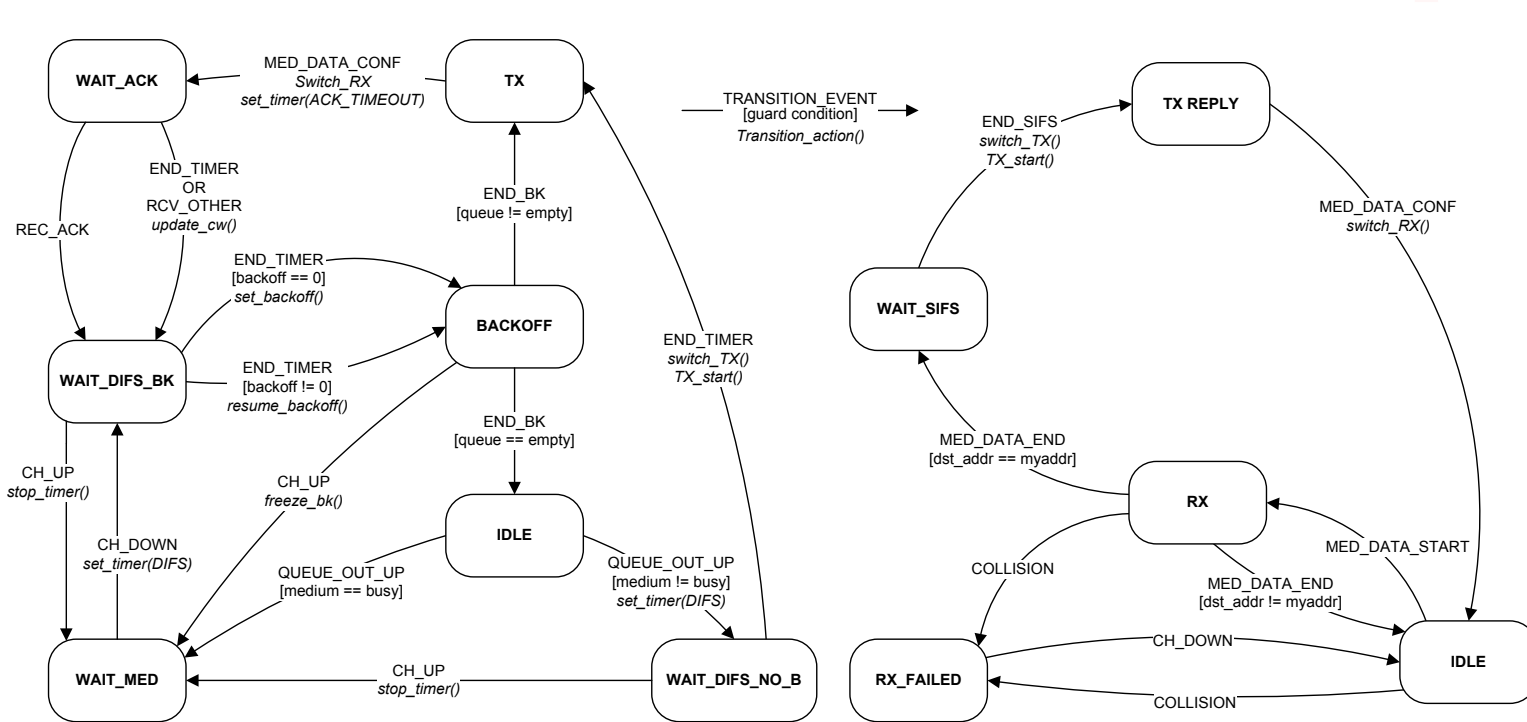
- very slim, only 544 bytes for DCF. It is sent via a regular wireless frame;
- can be dynamically loaded 'on the fly';
- is portable over different vendors' WMPs (as long as the instruction set is the same).
- can be periodically scheduled;
- can be injected locally or on a remote NIC sending it over the wireless link.

Memory address	Memory	Memory	Description
0000	FFFF FFFF FFFF FFFF	FFFF FFFF FFFF FFFF	Initial State Descriptor
0001	FFFF FFFF FFFF FFFF	FFFF FFFF FFFF FFFF	Initial State Descriptor
0002	FFFF FFFF FFFF FFFF	FFFF FFFF FFFF FFFF	Initial State Descriptor
0003	FFFF FFFF FFFF FFFF	FFFF FFFF FFFF FFFF	Initial State Descriptor
0004	FFFF FFFF FFFF FFFF	FFFF FFFF FFFF FFFF	Initial State Descriptor
0005	FFFF FFFF FFFF FFFF	FFFF FFFF FFFF FFFF	Initial State Descriptor
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0008	FFFF FFFF FFFF FFFF	FFFF FFFF FFFF FFFF	Initial State Descriptor
0009	FFFF FFFF FFFF FFFF	FFFF FFFF FFFF FFFF	Initial State Descriptor
0010	FFFF FFFF FFFF FFFF	FFFF FFFF FFFF FFFF	Initial State Descriptor
0011	FFFF FFFF FFFF FFFF	FFFF FFFF FFFF FFFF	Initial State Descriptor
0012	FFFF FFFF FFFF FFFF	FFFF FFFF FFFF FFFF	Initial State Descriptor
0013	FFFF FFFF FFFF FFFF	FFFF FFFF FFFF FFFF	Initial State Descriptor
0014	FFFF FFFF FFFF FFFF	FFFF FFFF FFFF FFFF	Initial State Descriptor
0015	FFFF FFFF FFFF FFFF	FFFF FFFF FFFF FFFF	Initial State Descriptor
0016	FFFF FFFF FFFF FFFF	FFFF FFFF FFFF FFFF	Initial State Descriptor
0017	FFFF FFFF FFFF FFFF	FFFF FFFF FFFF FFFF	Initial State Descriptor
0018	FFFF FFFF FFFF FFFF	FFFF FFFF FFFF FFFF	Initial State Descriptor
0019	FFFF FFFF FFFF FFFF	FFFF FFFF FFFF FFFF	Initial State Descriptor
0020	FFFF FFFF FFFF FFFF	FFFF FFFF FFFF FFFF	Initial State Descriptor
0021	FFFF FFFF FFFF FFFF	FFFF FFFF FFFF FFFF	Initial State Descriptor
0022	FFFF FFFF FFFF FFFF	FFFF FFFF FFFF FFFF	Initial State Descriptor
0023	FFFF FFFF FFFF FFFF	FFFF FFFF FFFF FFFF	Initial State Descriptor
0024	FFFF FFFF FFFF FFFF	FFFF FFFF FFFF FFFF	Initial State Descriptor
0025	FFFF FFFF FFFF FFFF	FFFF FFFF FFFF FFFF	Initial State Descriptor
0026	FFFF FFFF FFFF FFFF	FFFF FFFF FFFF FFFF	Initial State Descriptor
0027	FFFF FFFF FFFF FFFF	FFFF FFFF FFFF FFFF	Initial State Descriptor
0028	FFFF FFFF FFFF FFFF	FFFF FFFF FFFF FFFF	Initial State Descriptor
0029	FFFF FFFF FFFF FFFF	FFFF FFFF FFFF FFFF	Initial State Descriptor
0030	FFFF FFFF FFFF FFFF	FFFF FFFF FFFF FFFF	Initial State Descriptor
0031	FFFF FFFF FFFF FFFF	FFFF FFFF FFFF FFFF	Initial State Descriptor
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0035	FFFF FFFF FFFF FFFF	FFFF FFFF FFFF FFFF	Initial State Descriptor
0036	FFFF FFFF FFFF FFFF	FFFF FFFF FFFF FFFF	Initial State Descriptor
0037	FFFF FFFF FFFF FFFF	FFFF FFFF FFFF FFFF	Initial State Descriptor
0038	FFFF FFFF FFFF FFFF	FFFF FFFF FFFF FFFF	Initial State Descriptor
0039	FFFF FFFF FFFF FFFF	FFFF FFFF FFFF FFFF	Initial State Descriptor
0040	FFFF FFFF FFFF FFFF	FFFF FFFF FFFF FFFF	Initial State Descriptor
0041	FFFF FFFF FFFF FFFF	FFFF FFFF FFFF FFFF	Initial State Descriptor
0042	FFFF FFFF FFFF FFFF	FFFF FFFF FFFF FFFF	Initial State Descriptor
0043	FFFF FFFF FFFF FFFF	FFFF FFFF FFFF FFFF	Initial State Descriptor
0044	FFFF FFFF FFFF FFFF	FFFF FFFF FFFF FFFF	Initial State Descriptor
0045	FFFF FFFF FFFF FFFF	FFFF FFFF FFFF FFFF	Initial State Descriptor
0046	FFFF FFFF FFFF FFFF	FFFF FFFF FFFF FFFF	Initial State Descriptor
0047	FFFF FFFF FFFF FFFF	FFFF FFFF FFFF FFFF	Initial State Descriptor
0048	FFFF FFFF FFFF FFFF	FFFF FFFF FFFF FFFF	Initial State Descriptor
0049	FFFF FFFF FFFF FFFF	FFFF FFFF FFFF FFFF	Initial State Descriptor
0050	FFFF FFFF FFFF FFFF	FFFF FFFF FFFF FFFF	Initial State Descriptor
0051	FFFF FFFF FFFF FFFF	FFFF FFFF FFFF FFFF	Initial State Descriptor
0052	FFFF FFFF FFFF FFFF	FFFF FFFF FFFF FFFF	Initial State Descriptor
0053	FFFF FFFF FFFF FFFF	FFFF FFFF FFFF FFFF	Initial State Descriptor
0054	FFFF FFFF FFFF FFFF	FFFF FFFF FFFF FFFF	Initial State Descriptor
0055	FFFF FFFF FFFF FFFF	FFFF FFFF FFFF FFFF	Initial State Descriptor
0056	FFFF FFFF FFFF FFFF	FFFF FFFF FFFF FFFF	Initial State Descriptor
0057	FFFF FFFF FFFF FFFF	FFFF FFFF FFFF FFFF	Initial State Descriptor
0058	FFFF FFFF FFFF FFFF	FFFF FFFF FFFF FFFF	Initial State Descriptor
0059	FFFF FFFF FFFF FFFF	FFFF FFFF FFFF FFFF	Initial State Descriptor
0060	FFFF FFFF FFFF FFFF	FFFF FFFF FFFF FFFF	Initial State Descriptor
0061	FFFF FFFF FFFF FFFF	FFFF FFFF FFFF FFFF	Initial State Descriptor
0062	FFFF FFFF FFFF FFFF	FFFF FFFF FFFF FFFF	Initial State Descriptor
0063	FFFF FFFF FFFF FFFF	FFFF FFFF FFFF FFFF	Initial State Descriptor
0064	FFFF FFFF FFFF FFFF	FFFF FFFF FFFF FFFF	Initial State Descriptor
0065	FFFF FFFF FFFF FFFF	FFFF FFFF FFFF FFFF	Initial State Descriptor
0066	FFFF FFFF FFFF FFFF	FFFF FFFF FFFF FFFF	Initial State Descriptor
0067	FFFF FFFF FFFF FFFF	FFFF FFFF FFFF FFFF	Initial State Descriptor
0068	FFFF FFFF FFFF FFFF	FFFF FFFF FFFF FFFF	Initial State Descriptor
0069	FFFF FFFF FFFF FFFF	FFFF FFFF FFFF FFFF	Initial State Descriptor
0070	FFFF FFFF FFFF FFFF	FFFF FFFF FFFF FFFF	Initial State Descriptor
0071	FFFF FFFF FFFF FFFF	FFFF FFFF FFFF FFFF	Initial State Descriptor
0072	FFFF FFFF FFFF FFFF	FFFF FFFF FFFF FFFF	Initial State Descriptor
0073	FFFF FFFF FFFF FFFF	FFFF FFFF FFFF FFFF	Initial State Descriptor
0074	FFFF FFFF FFFF FFFF	FFFF FFFF FFFF FFFF	Initial State Descriptor
0075	FFFF FFFF FFFF FFFF	FFFF FFFF FFFF FFFF	Initial State Descriptor
0076	FFFF FFFF FFFF FFFF	FFFF FFFF FFFF FFFF	Initial State Descriptor
0077	FFFF FFFF FFFF FFFF	FFFF FFFF FFFF FFFF	Initial State Descriptor
0078	FFFF FFFF FFFF FFFF	FFFF FFFF FFFF FFFF	Initial State Descriptor
0079	FFFF FFFF FFFF FFFF	FFFF FFFF FFFF FFFF	Initial State Descriptor
0080	FFFF FFFF FFFF FFFF	FFFF FFFF FFFF FFFF	Initial State Descriptor
0081	FFFF FFFF FFFF FFFF	FFFF FFFF FFFF FFFF	Initial State Descriptor
0082	FFFF FFFF FFFF FFFF	FFFF FFFF FFFF FFFF	Initial State Descriptor
0083	FFFF FFFF FFFF FFFF	FFFF FFFF FFFF FFFF	Initial State Descriptor
0084	FFFF FFFF FFFF FFFF	FFFF FFFF FFFF FFFF	Initial State Descriptor
0085	FFFF FFFF FFFF FFFF	FFFF FFFF FFFF FFFF	Initial State Descriptor
0086	FFFF FFFF FFFF FFFF	FFFF FFFF FFFF FFFF	Initial State Descriptor
0087	FFFF FFFF FFFF FFFF	FFFF FFFF FFFF FFFF	Initial State Descriptor
0088	FFFF FFFF FFFF FFFF	FFFF FFFF FFFF FFFF	Initial State Descriptor
0089	FFFF FFFF FFFF FFFF	FFFF FFFF FFFF FFFF	Initial State Descriptor
0090	FFFF FFFF FFFF FFFF	FFFF FFFF FFFF FFFF	Initial State Descriptor
0091	FFFF FFFF FFFF FFFF	FFFF FFFF FFFF FFFF	Initial State Descriptor
0092	FFFF FFFF FFFF FFFF	FFFF FFFF FFFF FFFF	Initial State Descriptor
0093	FFFF FFFF FFFF FFFF	FFFF FFFF FFFF FFFF	Initial State Descriptor
0094	FFFF FFFF FFFF FFFF	FFFF FFFF FFFF FFFF	Initial State Descriptor
0095	FFFF FFFF FFFF FFFF	FFFF FFFF FFFF FFFF	Initial State Descriptor
0096	FFFF FFFF FFFF FFFF	FFFF FFFF FFFF FFFF	Initial State Descriptor
0097	FFFF FFFF FFFF FFFF	FFFF FFFF FFFF FFFF	Initial State Descriptor
0098	FFFF FFFF FFFF FFFF	FFFF FFFF FFFF FFFF	Initial State Descriptor
0099	FFFF FFFF FFFF FFFF	FFFF FFFF FFFF FFFF	Initial State Descriptor
0100	FFFF FFFF FFFF FFFF	FFFF FFFF FFFF FFFF	Initial State Descriptor

MAC program examples

DCF

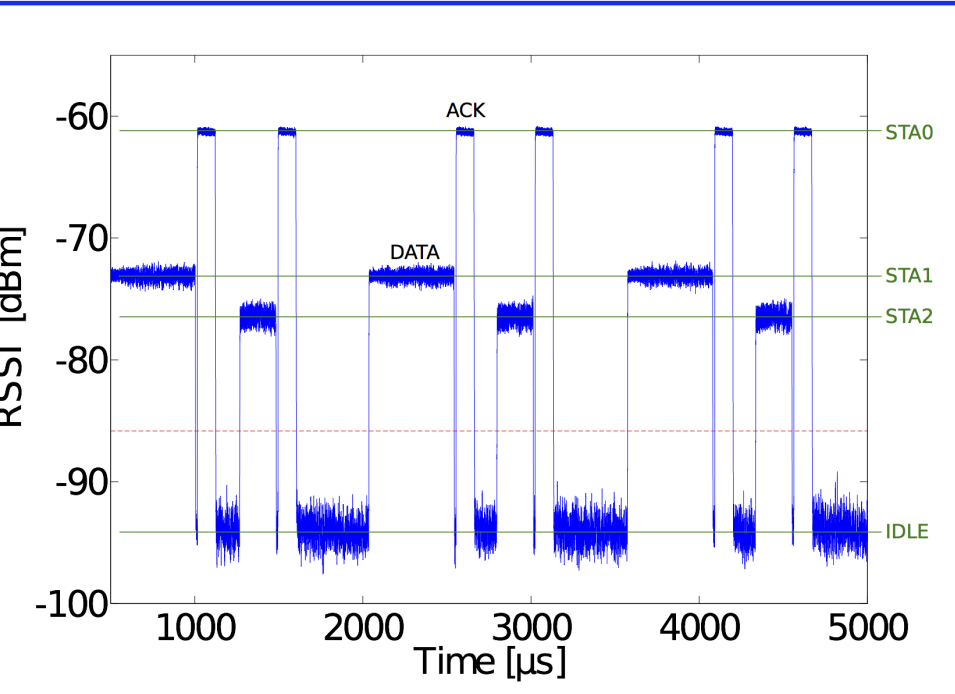
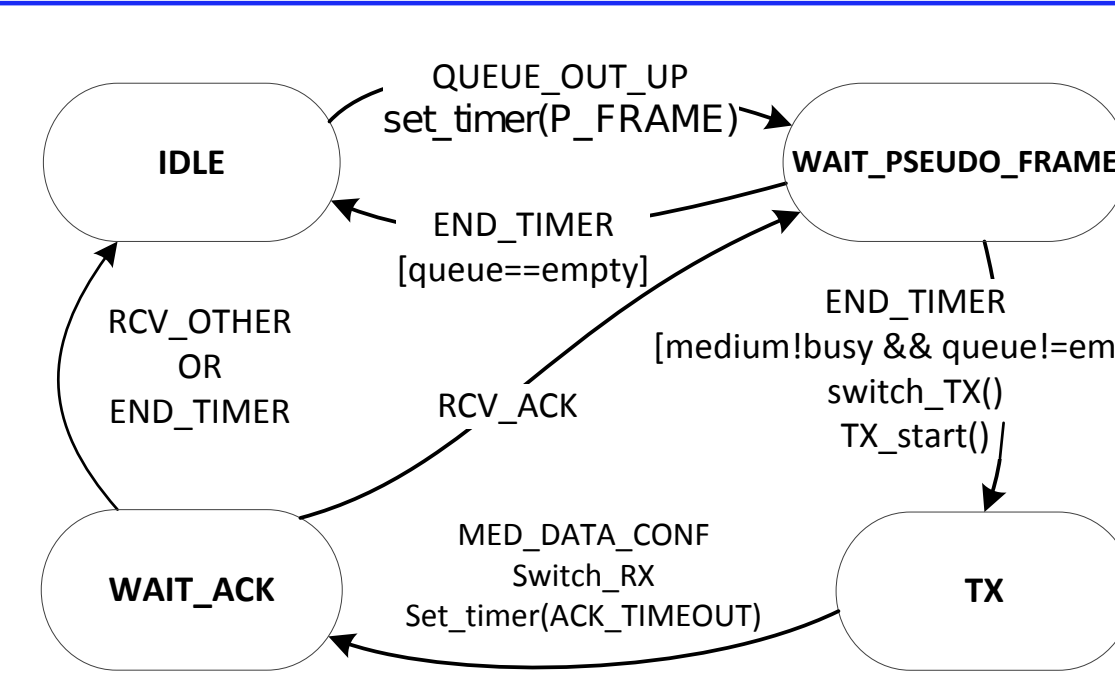
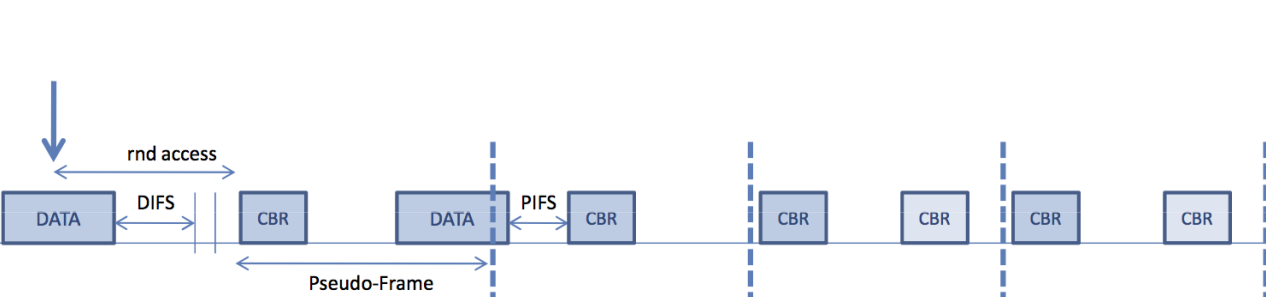
Even standard DCF can be defined on the top of our API.



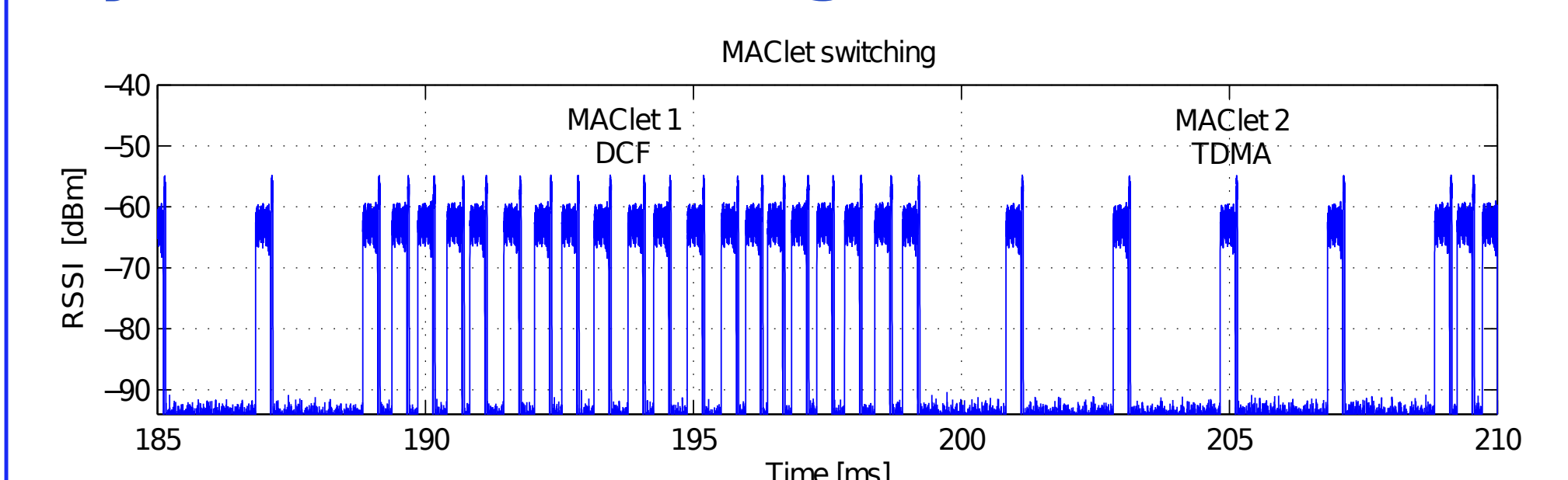
DCF running on the WMP has the same performances than the hard-coded firmware implementation. DCF timing parameters can be finely tuned.

Pseudo-TDMA

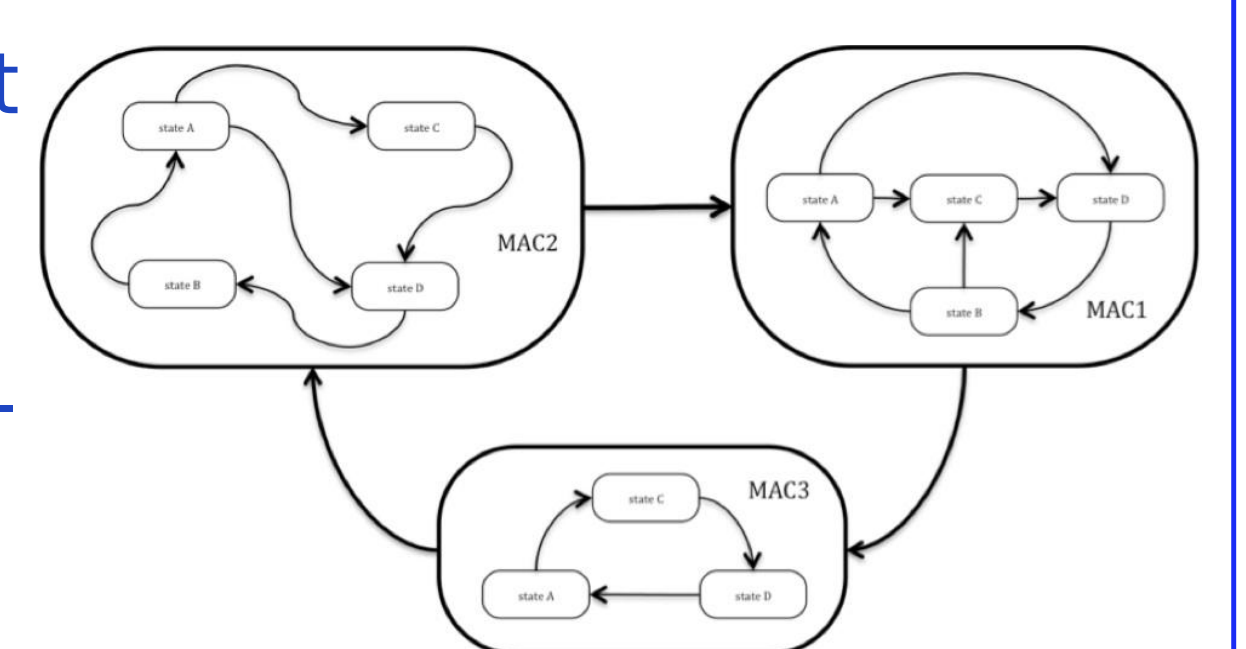
A simple pseudo-TDMA is performed after a random access.



Bytecode switching

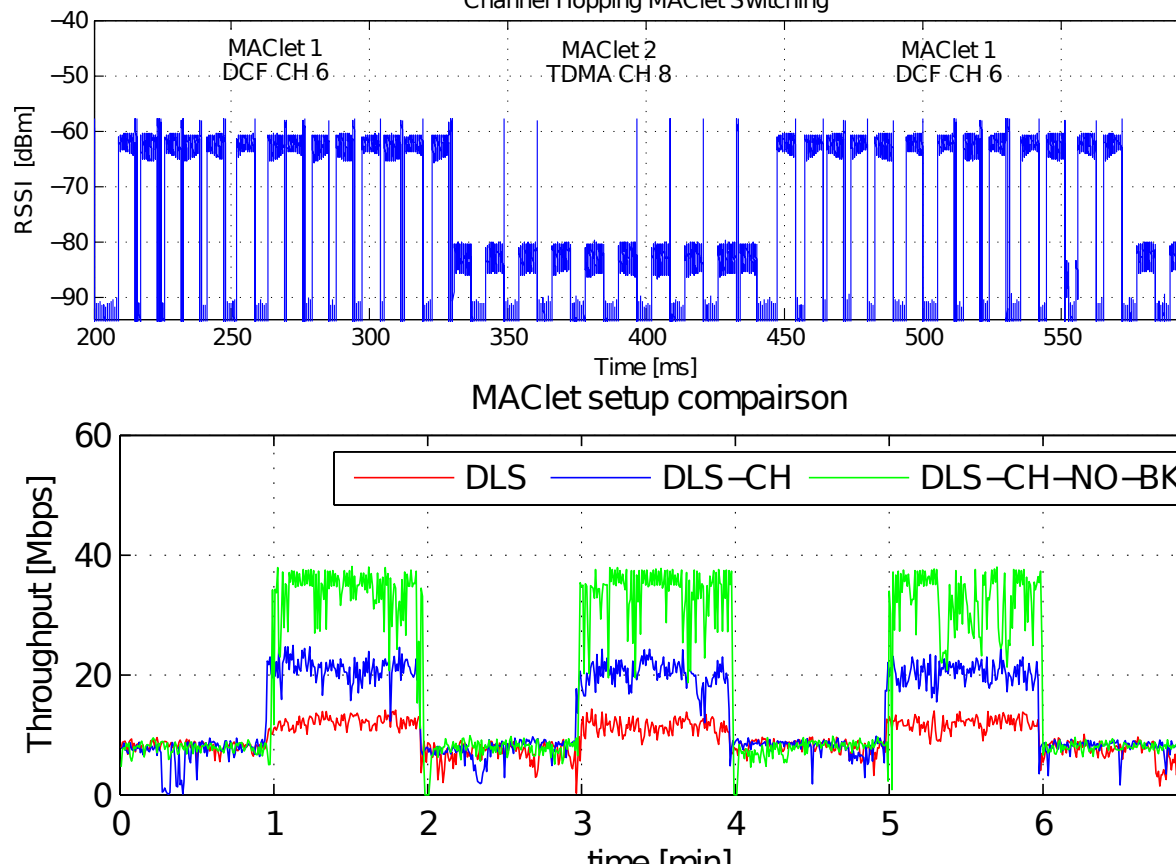
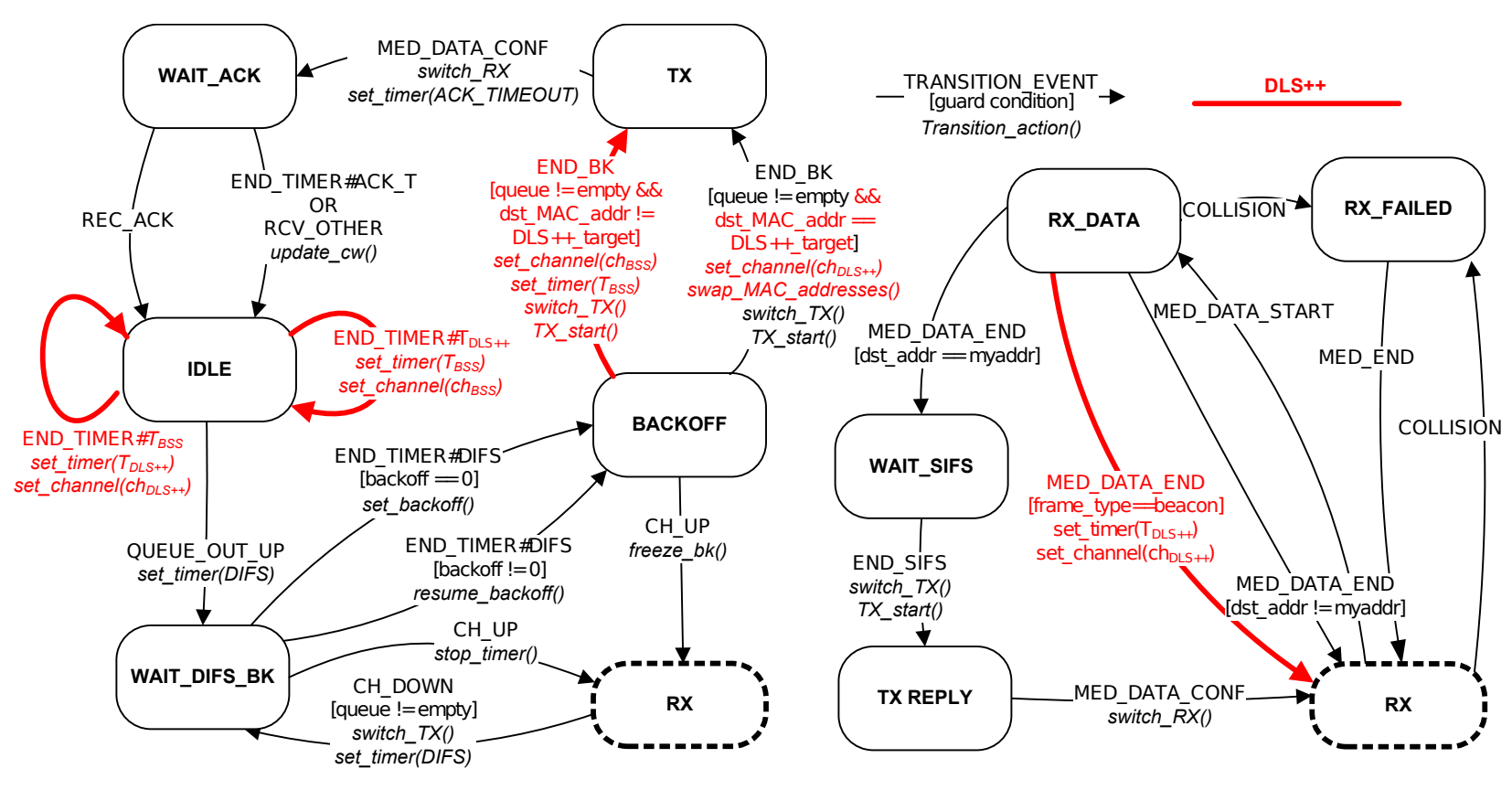


A MAC switch is just a state transition. Bytecode switching is performed at per-packet time resolution.



DLS++

Direct Link Setup with multi-channel capabilities. Use legacy DCF towards the AP and TDMA on a different channel while communicating on a direct link.



Links

I. Tinnirello, G. Bianchi, P. Gallo, D. Garlisi, F. Giuliano, F. Gringoli, "Wireless MAC Processors: Programming MAC Protocols on Commodity Hardware" IEEE INFOCOM, March 2012.

<http://wmp.tti.unipa.it>

<http://www.ict-flavia.eu/>

